

# Altera Device Guide Line

(NOTE: This document is "Altera Device Guide Line)

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by  
Altera Korea

Author:	Sung-Chan Oh
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**Revision History**

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1.0	S.C. Oh	1, Jan, 04	Initial version

# Table of Contents:

<b>1.</b>	<b>OVERVIEW .....</b>	<b>4</b>
<b>2.</b>	<b>DEVICE I/O.....</b>	<b>4</b>
2.1	Voltage.....	4
2.1.1	Core Voltage	
2.1.2	I/O Voltage	
2.1.3	PLL Voltage	
2.2	Dual Purpose I/O .....	5
2.3	Unused I/O.....	7
<b>3.</b>	<b>CONFIGURATION .....</b>	<b>10</b>
3.1	Passive Serial .....	11
3.1.1	Passive Serial with Configuration Device	
3.1.2	Passive Serial with Download Cable	
3.2	JTAG .....	14
<b>4.</b>	<b>DEBUGGING CONFIGURATION PROBLEM .....</b>	<b>15</b>
4.1	Configuration Reliability .....	15
4.2	Board Layout Tips .....	16
4.3	Debugging Suggestions .....	17
4.3.1	All Configuration Schemes	
4.3.2	Multi-Device Configuration Chains	
4.3.3	Using an External Host (e.g., Microprocessor or CPLD)	
4.3.4	Using a Configuration Device	
4.3.5	Using JTAG Configuration	
4.4	Error detection Circuitry .....	20
4.5	Combination of Configuration Device and JTAG .....	21
<b>5.</b>	<b>POWER SEQUENCE .....</b>	<b>22</b>

# 1. Overview

Altera FPGA data spec      FPGA I/O PCB layout      CPLD I/O configuration      I/O 가      가      가

## 2. Device I/O

### 2.1 Voltage

#### 2.1.1 Core Voltage

Core I/O pad PLL logic element memory cell core

	Process	Core Voltage
Stratix / GX	0.13um	1.5v
Cyclone	0.13um	1.5v
APEX20KE	0.18um	1.8v

#### 2.1.2 I/O Voltage

PLD I/O Core 가

	I/O Voltage
Stratix / GX	1.5v / 1.8v / 2.5v / 3.3v
Cyclone	1.5v / 1.8v / 2.5v / 3.3v
APEX20KE	1.8v / 2.5v / 3.3v

#### 2.1.3 PLL Voltage

PLL clock noise  
 VCC\_int VCC\_io (GND )

	VCC_CKCLK#	VCC_CKOUT#	GND_CKCLK#	GND_CKOUT#
Stratix / GX	1.5v	1.5v / 2.5v / 3.3v		
Cyclone	1.5v	1.5v / 2.5v / 3.3v	GND	GND
APEX20KE	1.8v	1.8v / 2.5v / 3.3v		

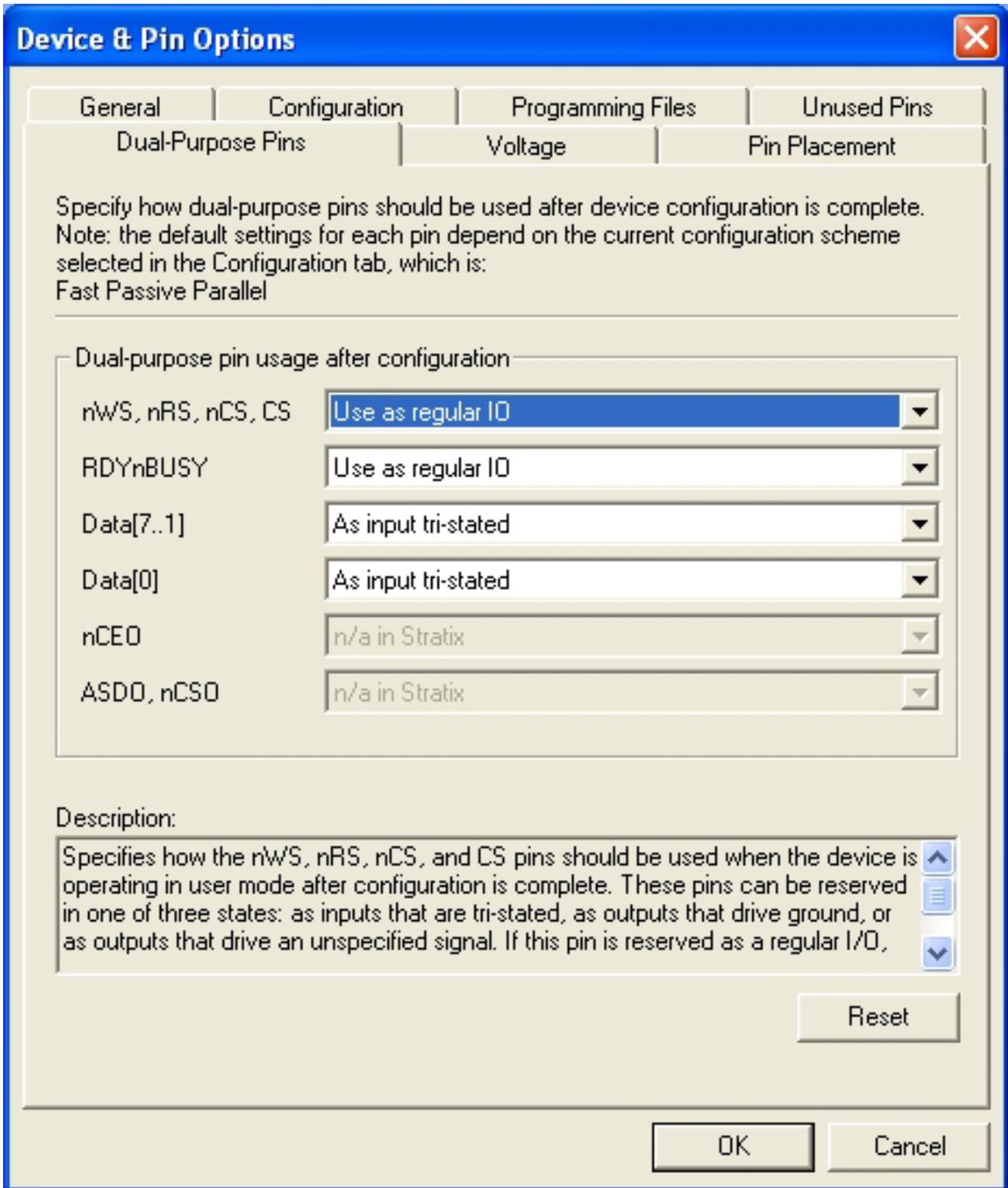
Clock	pin	P	N	Positive	Negative
LVDS	differential		pair	P/N	
LVTTL	P				

## 2.2 Dual Purpose I/O

Quartus Assignments -> Device -> Device & Pin Options -> Dual-Purpose Pins configuration user I/O 가

가

) " Configuration" configuration



### 2.3 Unused I/O

	Dedicated clk and input pins	Unused JTAG pins (NOT using JTAG)	PLL-related pins	General IOs
<b>MAX 7000A, 7000S, 7000E, 7000</b>				GND
	GND - dedicated floating , 가	IO 가		IO 가 unknown low high switching
<b>MAX 7000AE, 7000B</b>	GND - dedicated floating , 가	IO 가		GND
		가		
<b>ACEX &amp; FLEX</b>			VCC_CLKLK GND_CLKLK PLL	
			ground	
	GND - dedicated floating , 가		PLL VCC_CLKLK VCCINT GND_CLKLK GNDINT	GND IO 가 unknown
		AN 39		

**APEX &  
Cyclone  
& Stratix**

CLKLK\_FB1p  
CLKLK\_FB2p  
GND

CLKLK\_OUT1p  
CLKLK\_OUT2p

CLKLK\_ENA  
VCCINT

GND  
가  
VCC\_CLKLK  
GND\_CLKLK  
PLL  
GND

PLL

VCC\_CLKLK  
VCCINT  
GND\_CLKLK  
GNDINT

VCC\_CLKOUT  
GND\_CLKOUT  
PLL

GND  
PLL PLL

GND - dedicated  
floating ,  
가

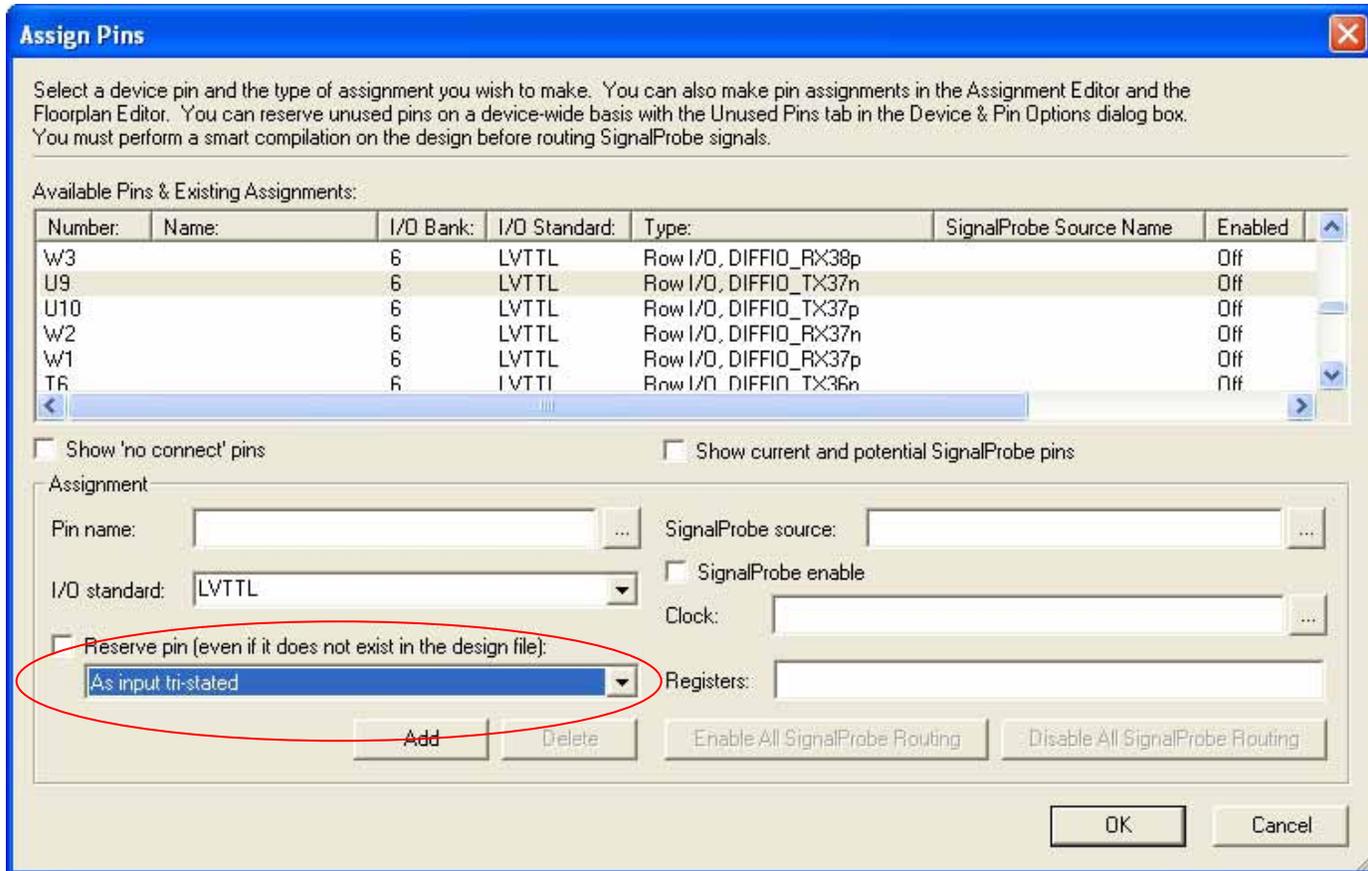
VCC\_CLKOUT  
GND\_CLKOUT

VCCIO 가  
GNDIO

AN 39

user I/O  
Reserve Pin

Quartus II Assignment -> Assign Pins



### 3. Configuration

PLD configuration

	. Configuration	ISP(In System Program)	ICR(In Circuit
Reconfiguration)		ByteBlaster	ISP 가 EPC

	ICR		
가	Altera	PS(Passive Serial)	JTAG
	가 configuration		

**Table 1-1. Configuration Scheme Device Family Support**

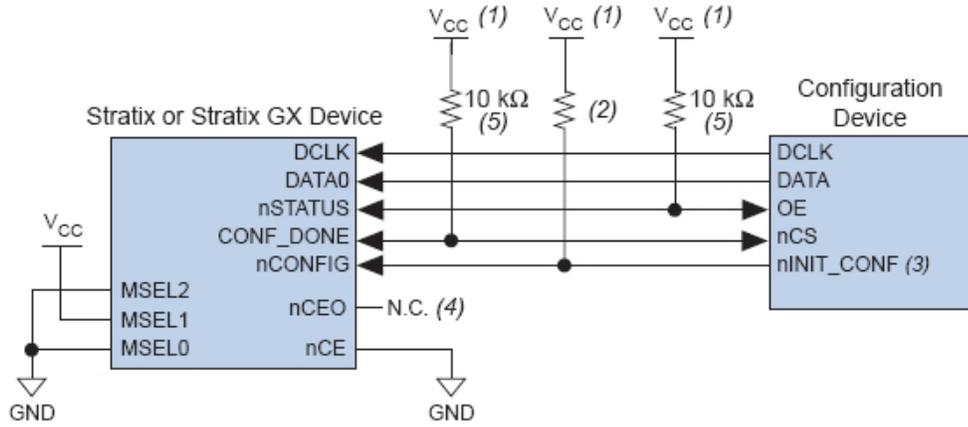
Configuration Scheme	Device Family							
	Stratix, Stratix GX	Cyclone	APEX II	APEX 20K, APEX 20KE, APEX 20KC	Mercury	ACEX 1K	FLEX 10K, FLEX 10KE, FLEX 10KA	FLEX 6000
Passive Serial (PS)	✓	✓	✓	✓	✓	✓	✓	✓
Active Serial (AS)		✓						
Fast Passive Parallel (FPP)	✓		✓					
Passive Parallel Synchronous (PPS)				✓	✓	✓	✓	
Passive Parallel Asynchronous (PPA)	✓		✓	✓	✓	✓	✓	
Passive Serial Asynchronous (PSA)								✓
Joint Test Action Group (JTAG)	✓	✓	✓	✓	✓	✓	✓	(1)

### 3.1 Passive Serial

가 Passive Serial DCLK / DATA0 / nSTATUS / nCONFIG / CONF\_DONE nSTATUS / nCONFIG / CONF\_DONE Pull-up PS 가 configuration , Stratix / GX EPC , Stratix / GX ByteBlaster . Stratix 가 device Configuration Handbook

[http://www.altera.com/literature/hb/cfg/config\\_handbook.pdf](http://www.altera.com/literature/hb/cfg/config_handbook.pdf)

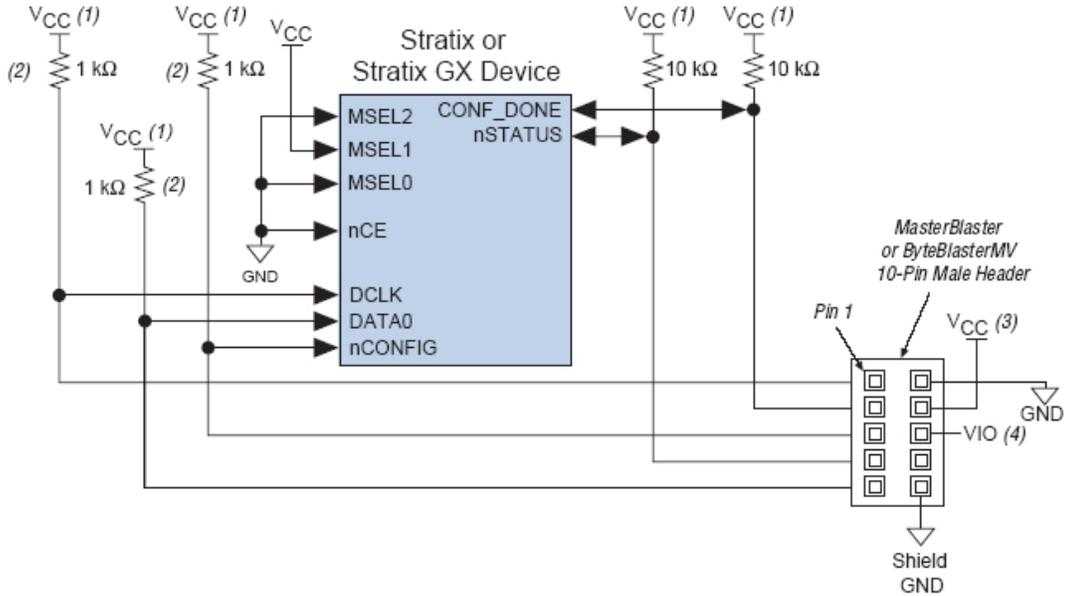
### 3.1.1 Passive Serial with Configuration Device



**Note**

- (1) Pull-up configuration device
- (2) 10k ohm Pull-up EPC16/8/4/2 OE nCS  
pull-up 가 , pull-up  
pull-up
- (3) nINIT\_CONF EPC16 / 8 / 4 / 2 , nINIT\_CONF  
nCONFIG pull-up
- (4) FPGA chain 가 FPGA nCEO
- (5) CONF\_DONE nSTATUS pull-up 10k ohm  
, CONF\_DONE nSTATUS 가 3.3v 2.5v pull-up  
pull-up

### 3.1.2 Passive Serial with Download Cable



- (1) Pull-up
- (2) DATA0 DCLK , configuration pull-up pull-up

- (3) MasterBlaster ByteBlasterMV 3.3v 5.0v Vcc
  - (4) 6 MasterBlaster driver Vio
- Vccio . ByteBlasterMV

) Configuration Configuration Handbook

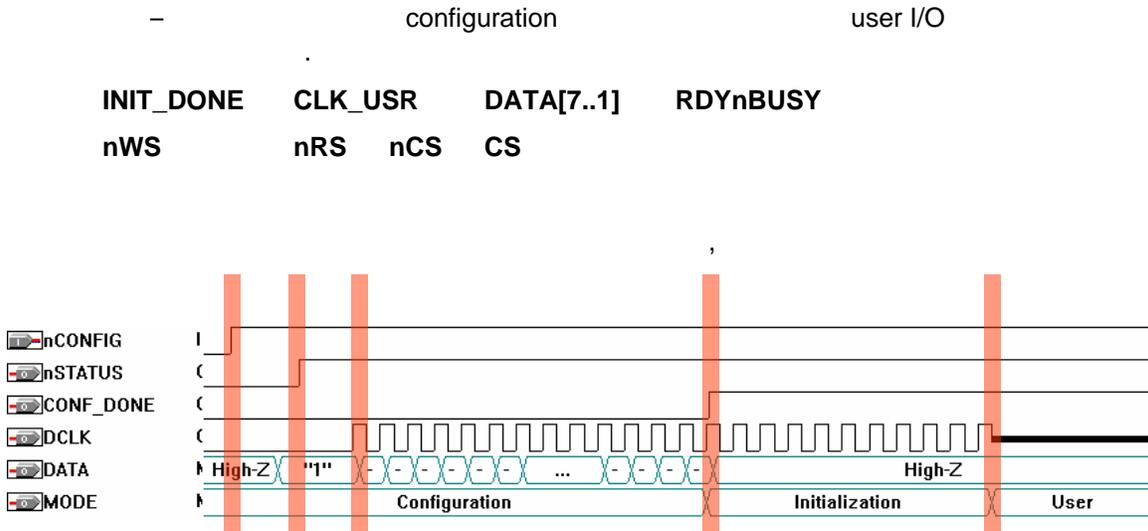
[http://www.altera.com/literature/hb/cfg/config\\_handbook.pdf](http://www.altera.com/literature/hb/cfg/config_handbook.pdf)

■ Configuration

- configuration
- 가 I/O 가

**nSTATUS CONF\_DONE MSEL DCLK**  
**nCONFIG nCE nCEO DATA0**  
**TDI TDO TCK TMS TRST**

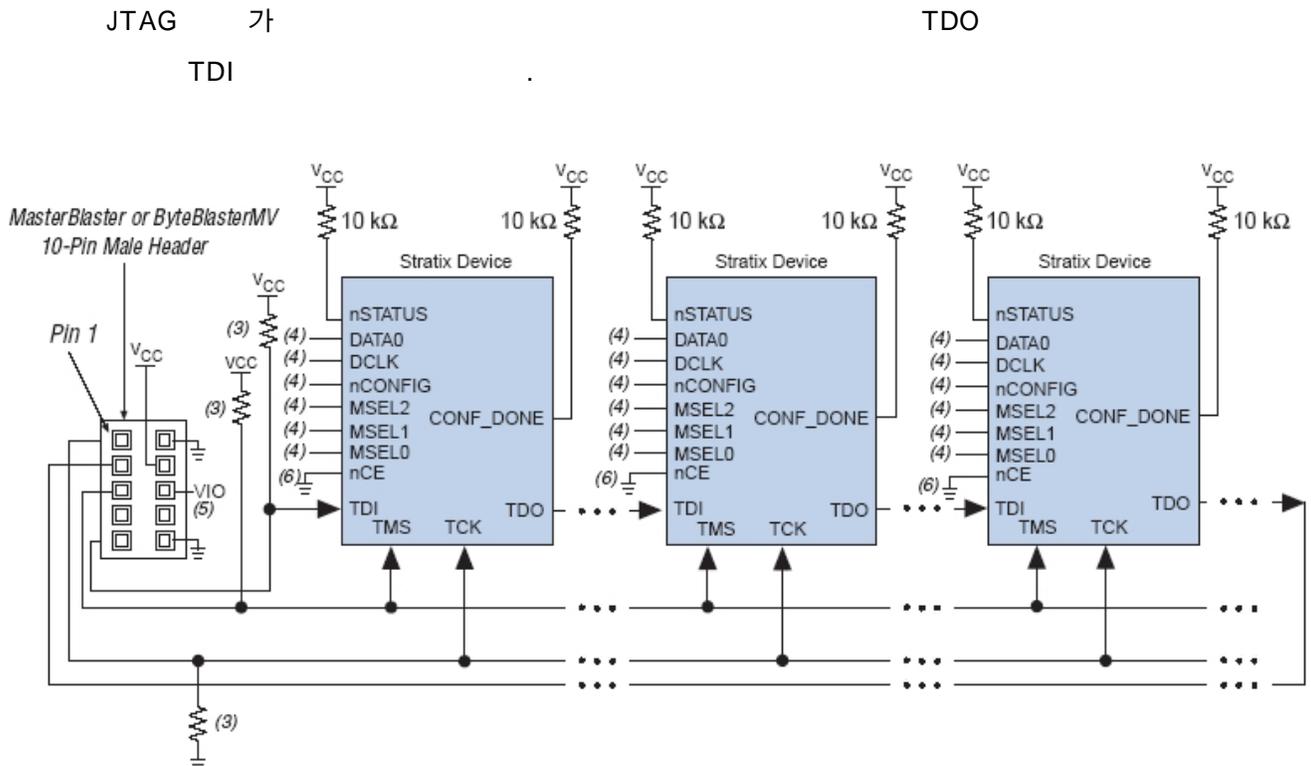
■ Dual-Purpose Configuration Pins



- ① nCONFIG 가 Low High , Configuration
  - MSEL Configuration
- ② Pull-up nSTATUS High
- ③ Configuration DCLK rising edge
  - DATA0 (Serial)
  - DATA[7..0] (Parallel)
- configuration 가 nSTATUS 가 low
- ④ Configuration CONF\_DONE 가 High
- ⑤ clock 가
  - Registers
  - User I/O
  - Operation
- ⑥ 가 User Mode
- Reconfigure , nCONFIG Low High
  - I/O Tri-State 가
  -
- INIT\_DONE
  - 가 off
  - Configuration
    - Configuration low

### 3.2 JTAG

JTAG 4 (TDI, TDO, TCK, TMS)가 pull-up  
pull-down



- (3) Pull-up / Pull-down 10k ohm
- (4) JTAG configuration nCONFIG Vcc, MSEL0 / 1 / 2  
GND , DATA0 DCLK "high" "low" pull-up down
- (5) Vio MasterBlaster Vccio
- (6) JTAG configuration nCE GND "low"



configuration

DCLK JTAG TCK 가

DATA set-up hold DCLK 가 , DATA DCLK

, Altera DCLK, DATA0,  
(DATA[7..0]), nCONFIG, nSTATUS, CONF\_DONE  
가 configuration

가 nSTATUS low ,  
configuration  
nSTATUS CONF\_DONE Vcc  
pull-up  
nSTATUS 가 CONF\_DONE  
, configuration 가

가 configuration , configuration signal integrity  
, DCLK DATA

JTAG TCK, TDI, TMS

Configuration , configuration 가  
nCS (FPGA CONF\_DOEN ) high  
Enhanced configuration bit CONF\_DONE  
high 64 DCLK  
EPC2 16DLCK  
configuration 가 nCS high  
, OE (FPGA nSTATUS ) low 가  
, nCS CONF\_DONE  
, configuration , capacitance  
가 CONF\_DONE

### 4.3 Debugging Sugesstions

Altera FPGA ,  
가  
configuration

#### 4.3.1 All Configuration Scheme

1. configuration target
2. Configuration JTAG I/O Bank FPGA Vccint
3. Configuration
4. JTAG , FPGA JTAG floating  
 , configuration  
 JTAG configuration configuration  
 가 , JTAG configuration floating toggling
5. 가  
 ,  
 가 , 가  
 , configuration  
 가
6. DCLK 가  
 DCLK 가 configuration , CRC  
 . FPGA DCLK 가  
 가
7. FPGA 가 configuration , INIT\_DONE  
 . INIT\_DONE Quartus II "Enable INIT\_DONE output option"  
 . INIT\_DONE open-drain Vcc pull-up  
 , nCONFIG 가 low configuration

high 가 . INIT\_DONE option FPGA  
 (configuration ), INIT\_DONE low 가 .  
 INIT\_DONE high , FPGA configuration

- configuration 가 configuration  
 CONF\_DONE high 가 , CONF\_DONE Vcc pull-up  
 GND low .

### 4.3.2 Multi-Device Configuration Chains

- SOF configuration Quartus II  
 “Convert Programming File” .
- Configuration , configuration 가 .

### 4.3.3 Using an External Host (e.g., Microprocessor or CPLD)

- Altera FPGA RBF (Raw Binary File)  
 byte LSB(Least Significant Bit)가 .  
 가 , configuration 가 .
- 가  
 DATA / DCLK nWS scope .
- PPA (Passive Parallel Asynchronous) , nRS floating  
 high ,  
 configuration 가 .

### 4.3.4 Using a Configuration Device

- Quartus II Programmer “ Verify” configuration 가  
 configuration 가  
 FPGA .
- configuration configuration 가 DLCK DATA  
 configuration idle ,  
 Configuration FPGA Vccint configuration

가 POR (Power On Reset)

3. Configuration , configuration CRC FPGA 가  
 nSTATUS low configuration 가 OE low  
 configuration CONF\_DONE high

4. enhanced configuration (EPC4 / 8 / 16)

PGM floating configuration  
 WP# boot  
 Vcc  
 BYTE# (100 ) Vcc ,  
 configuration  
 100  
 F-A0 C-A0, F-A1 C-A1, F-A15 C-A15, F-A16 C-A16

5. enhanced configuration  
 In-system programming FPGA configuration floating  
 tri-state

**4.3.5 Using JTAG Configuration**

1. JTAG Altera ,  
 TRST ( ) Vcc TCK pull-down

2. configuration  
 , nCE GND JTAG low  
 , nCONFIG Vcc high  
 , CONF\_DONE 가 low  
 가

3. TDO 가 TDI V<sub>IH</sub>  
 TDO 3.3v Vccio I/O , TDO  
 3.3v

4. , TCK  
 JTAG configuration

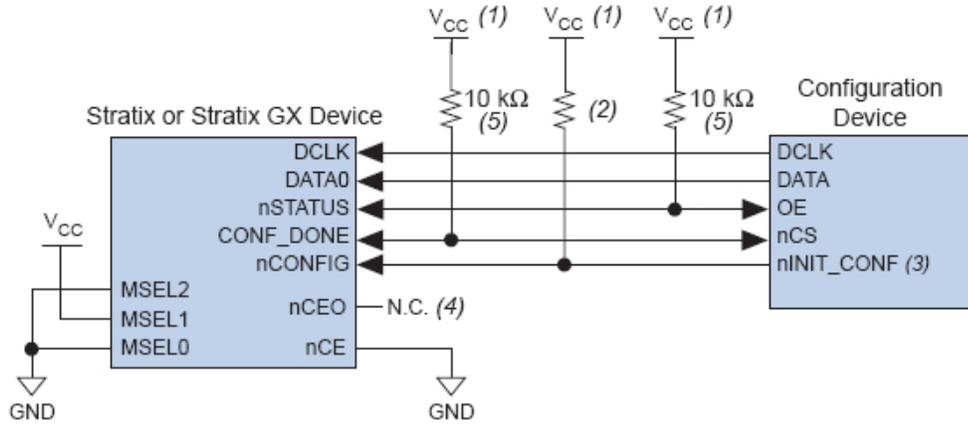
5. TCK 가 .  
 TCK 가 가  
 . DCLK 가 configuration ,  
 CRC

**4.4 Error Detection Circuitry**

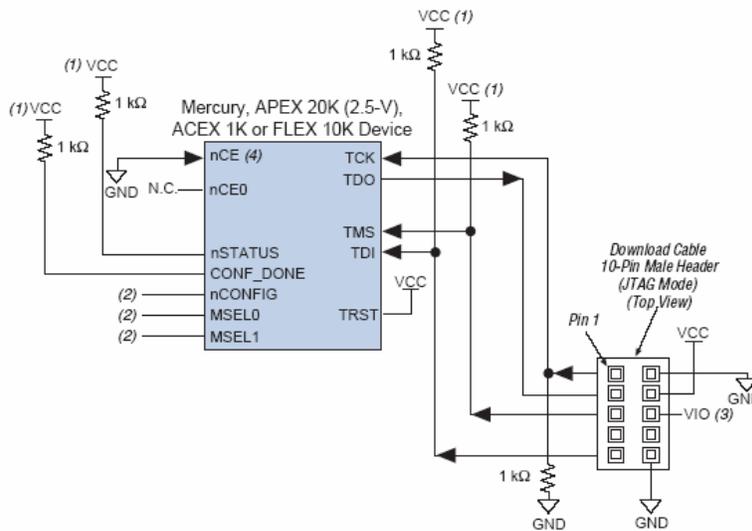
EPC1/2/1441 가 FPGA  
 configuration configuration  
 Configuration device nCS .  
 nCS configuration 가 FPGA high  
 configuration 가 OE( nSTATUS of FPGA) pin  
 low .  
 configuration 가 configuration CONF\_DONE (nCS of  
 EPC)가 high 가 (configuration ) EPC 16  
 OE low nSTATUS pin(FPGA) low  
 configuration . auto restart configuration on error option  
 enable configuration .  
 FPGA error detection scheme configuration  
 . FPGA CRC(Cyclic Redundancy Code) 가  
 CRC CRC 가 nSTATUS pin low  
 .  
 CRC checking FPGA .

**4.5 Combination of Configuration Device and JTAG**

Configuration 가 가  
 가 . Configuration device  
 Passive Serial JTAG Programming .



6-1 PS with Configuration device



6-2 JTAG programming

6-1 6-2 JTAG Programming CONF\_DONE,  
nSTATUS pull-up 1k ohm VCC  
configuration device Passive Serial Programming  
configuration scheme 가  
Jumper setting .

## 5. Power Sequence

Altera EPC4 / 8 / 16 Enhanced Configuration ( EEPC) Power On  
 Reset ( POR) FPGA Vccint .  
 CONF\_DONE 가 low configuration device OE 가 high 가 power  
 up  
 FPGA power EEPC 가 POR pull-up  
 high high CONF\_DONE high .  
 EEPC 가 POR OE 가 , pull-up EEPC  
 가 OE rising edge nCS 가 가  
 DATA DCLK toggle configuration .  
 power-down power-up EEPC 가  
 .  
 ) EEPC 가 configuration  
 EEPC 가 POR FPGA power up  
 .

Power-up EEPC POR time  
 .  
 EEPC 가 POR 가 PORSEL "high" 2ms  
 "low" 100ms 가 . Timing margin , 100ms POR timing  
 .