

(Technical)

Document No.: MJL-LD-AN-7

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Date: 2000 8 8

Subject: **LPM_FUNCTION** **ModelSim** **Simulation**

1. lpm_function 256x8 DPRAM

MAX+plus II Quartus Component MegaWizard Plug-in
Manager . Dual-Port RAM

ModelSim Functional Simulation Timing Simulation .

MAX+plus II File → Megawizard Plug-in Manger .

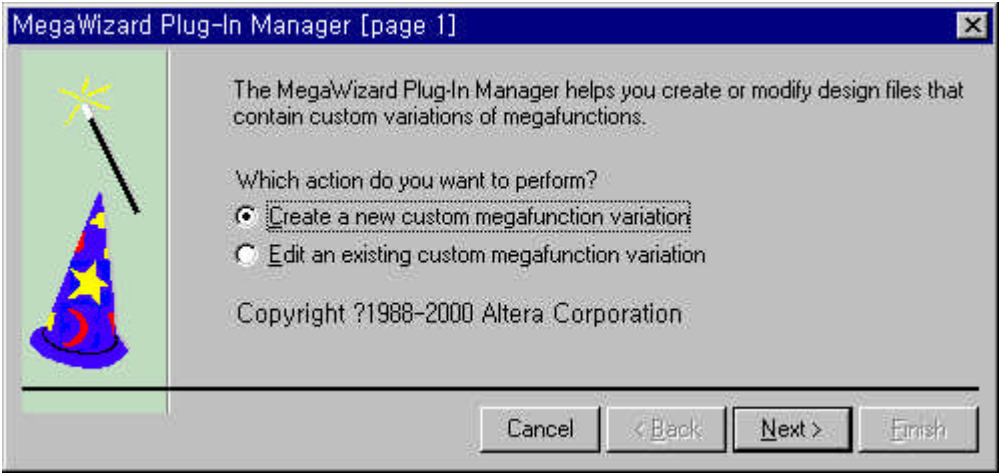


Figure 1 MegaWizard Plug-In Manager Window

Component	1	"Create a new custom megafunction
variation"		
Next Button	.	
2	lpm_ram_dp	VHDL
test	.	C: \ mywork \ modelsim \ dp_ram
		가
Next Button		On

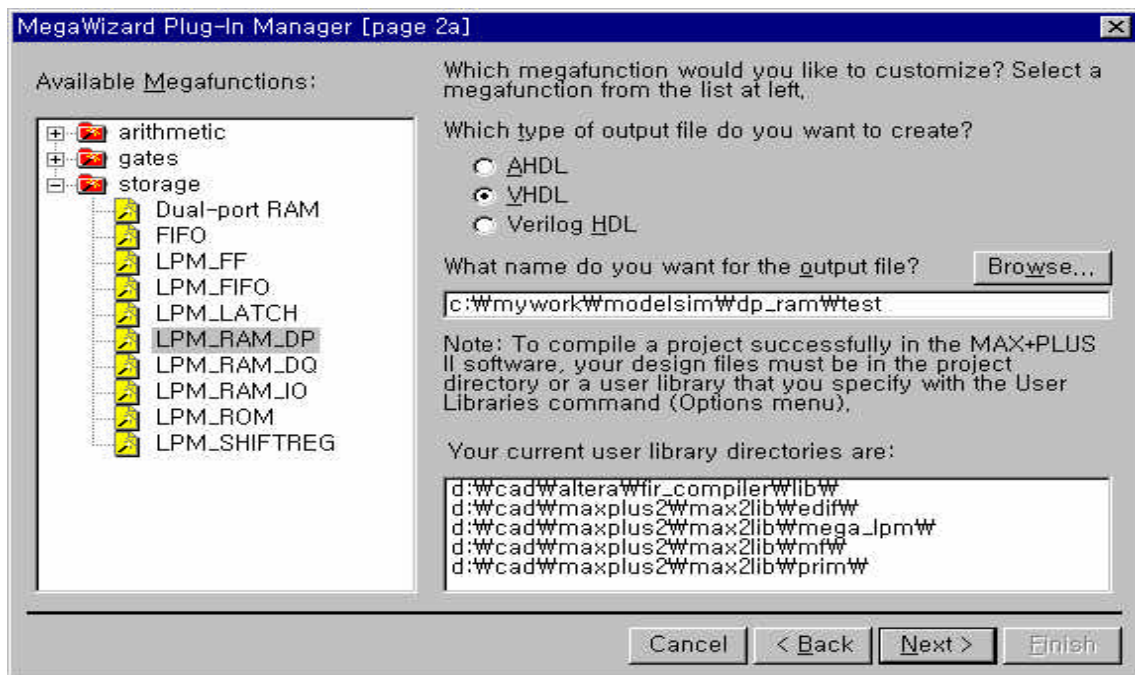


Figure 2 Select Megafunction Window

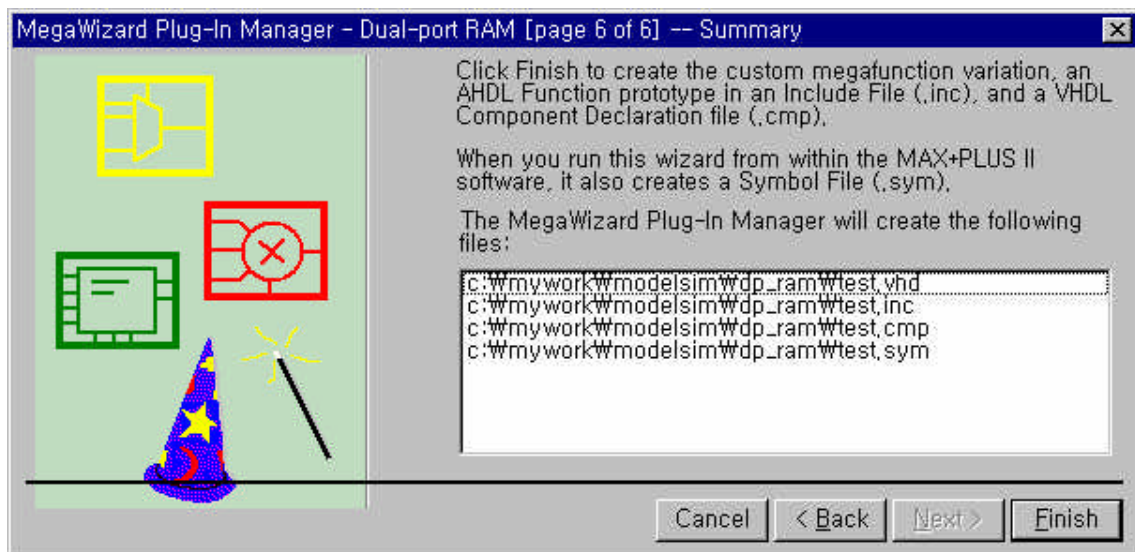


Figure 3 MegaWizard Summary Window

Default Option

Finish Button

C: \ MYWORK \ MODELSIM \ DP_RAM

3

2. ModelSim 256x8 DPRAM Function Simulation

ModelSim . Top Menu File → Change Directory... test.vhd
c: \ mywork \ modelsim \ dp_ram directory

Top Menu Design → Create a New Library... 4

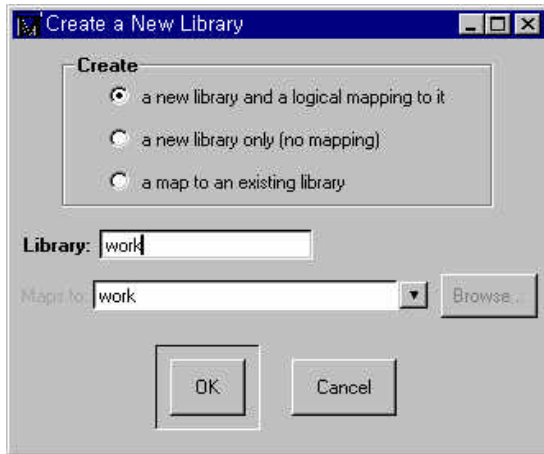


Figure 4 Create a New Library Window

modelsim.ini

가 ,

modelsim.ini

```

Compile . 5
Compile Window
c: \ mywork \ modelsim \ dp_ram \ test.vhd

```

Top Menu Design → Compile...
test.vhd File

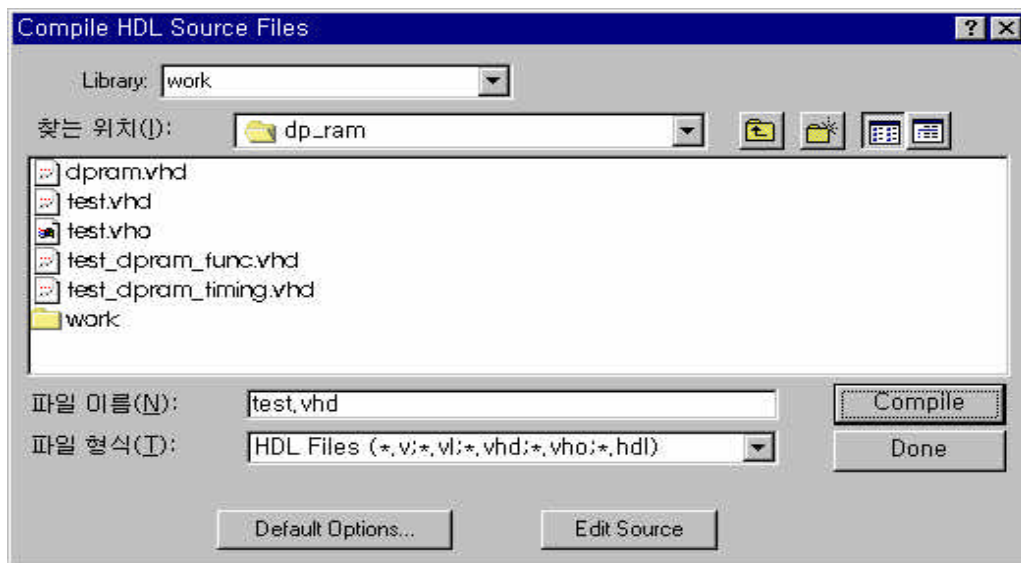


Figure 5 Compile HDL Source Files Window

Compile Button test.vhd File Compile .
가 6 Error 가 **LPM LIBRARY**

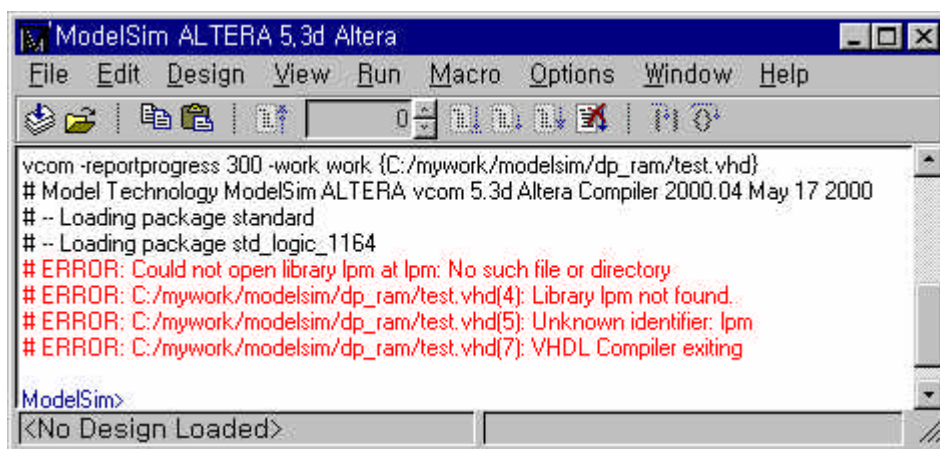
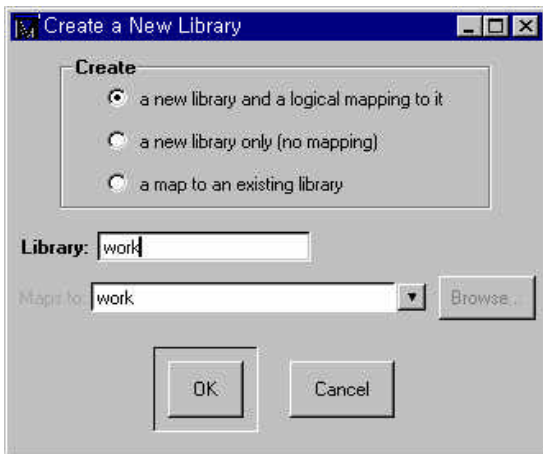


Figure 6 LPM Library 가 Error Message

ModelSim LPM Library LPM Library test.vhd Compile
ERROR Compile 가 가 .



- a new library and a logical mapping to it

ModelSim	work	modelsim.ini
work library가	work directory	.
c: \ mywork \ modelsim \ dp_ram directory	work Sub-directory	.

- a new library only [no mapping]

ModelSim	work	.
----------	------	---

- a map to an existing library

Library

LPM Library		ModelSim
Directory	"a map to an existing library"	
ModelSim Top Menu	File → Change Directory...	ModelSim
	d: \ cad \ modeltech_ae \ altera \ vhdl	Directory
ModelSim 5.3d Altera Edition Version	Altera	
Library Compile Altera Directory	VHDL Verilog Sub-directory	

Top Menu	Design → Create a New Library...	7
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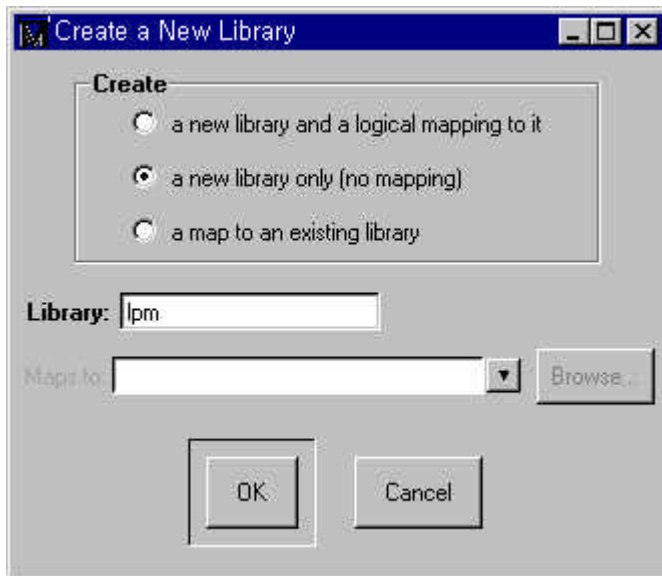


Figure 7 a new library only (no mapping) Window

LPM Directory	lpm_component	Source VHDL File	lpm_component
Modeling	Source VHDL File	ModelSim	Compile
.			
MAX+plus II	<MAX+plus II 가	> \ Ipmsim Directory	220pack.vhd,
220model.vhd	lpm_component	Source Code	.
.			
Quartus	<Quartus 가	> \ eda \ sim_lib Directory	Source
Code 가	.		
.			
ModelSim Top Menu	Design → Compile...	220pack.vhd, 220model.vhd	Compile
.	220pack.vhd	Compile	.
.			
8	.	8	Compile Button
VHDL Version	Coding	Default Option...	Button
			Source Code 가 1987
			9

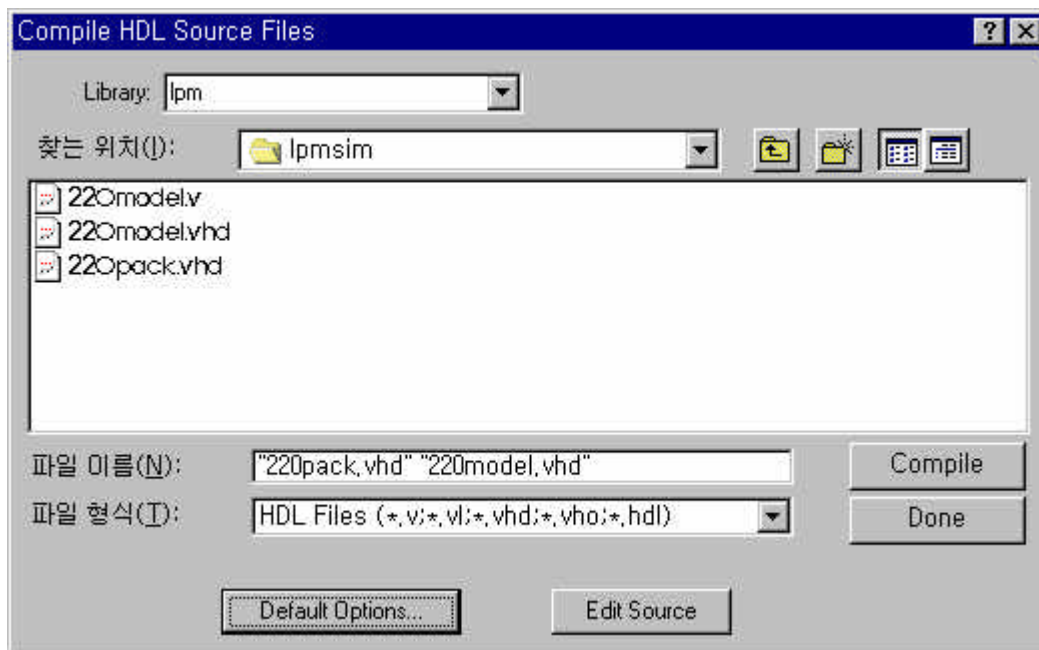


Figure 8 Compile HDL Source Files Window

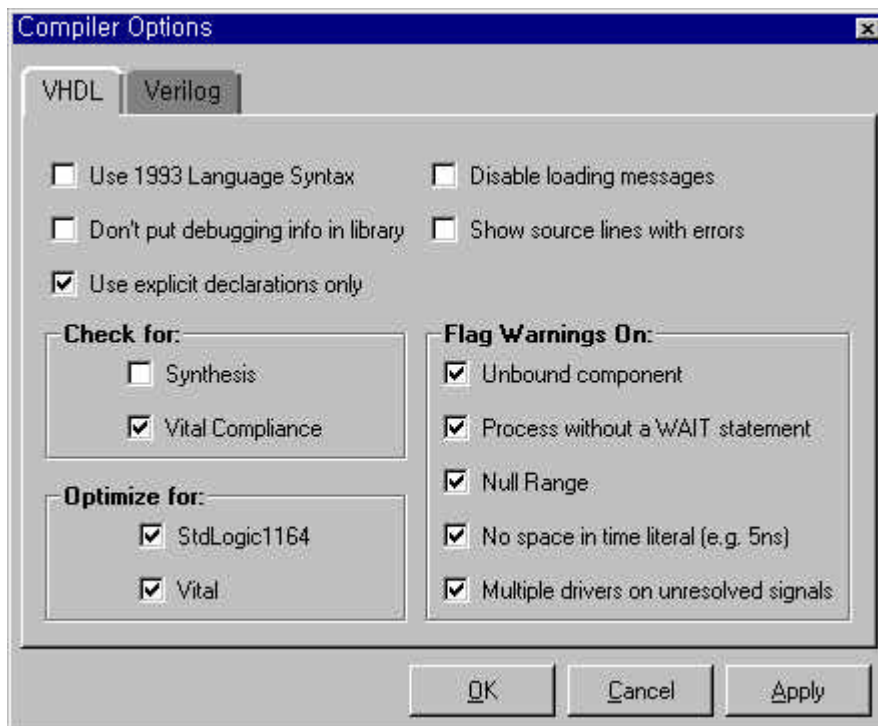


Figure 9 Compiler Options Window

8 Compile Button Source File Compile .

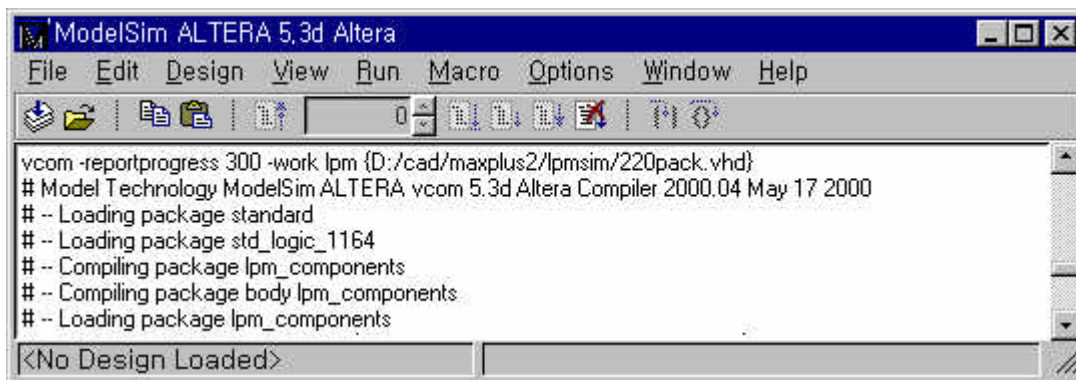


Figure 10 220PACK.VHD File Compile Result Window

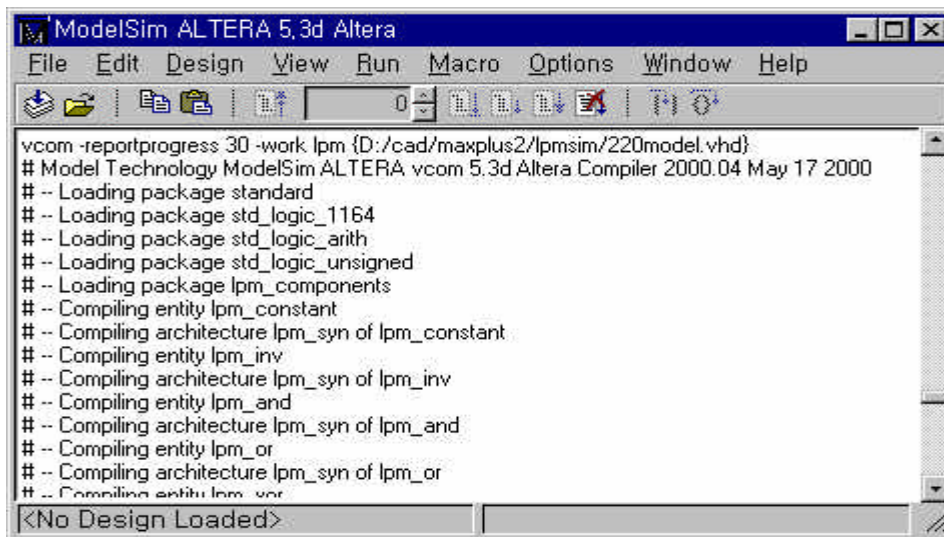


Figure 11 220MODEL.VHD File Compile Result Window

12 LPM LIBRARY 가 ModelSim Top Menu
File → Change Directory...

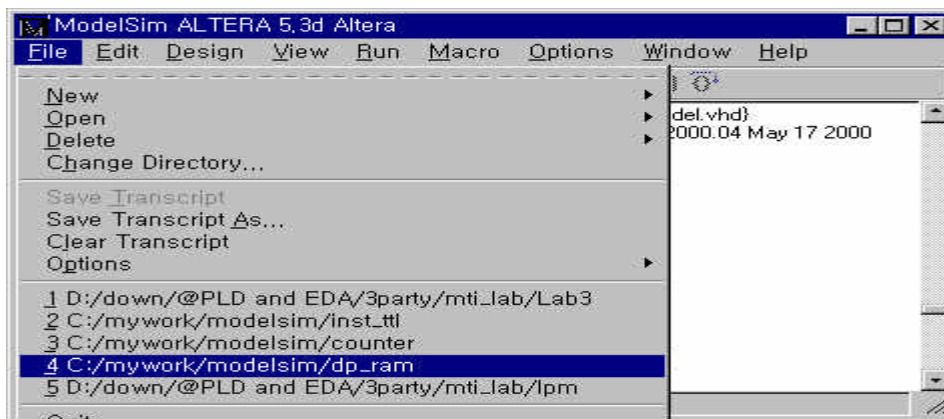


Figure 12 Change Directory... Window

ModelSim Top Down Menu Design → Browse Libraries... 13 LPM
 Library 가 LPM Library 가 가 Add Button
 14 LPM Library

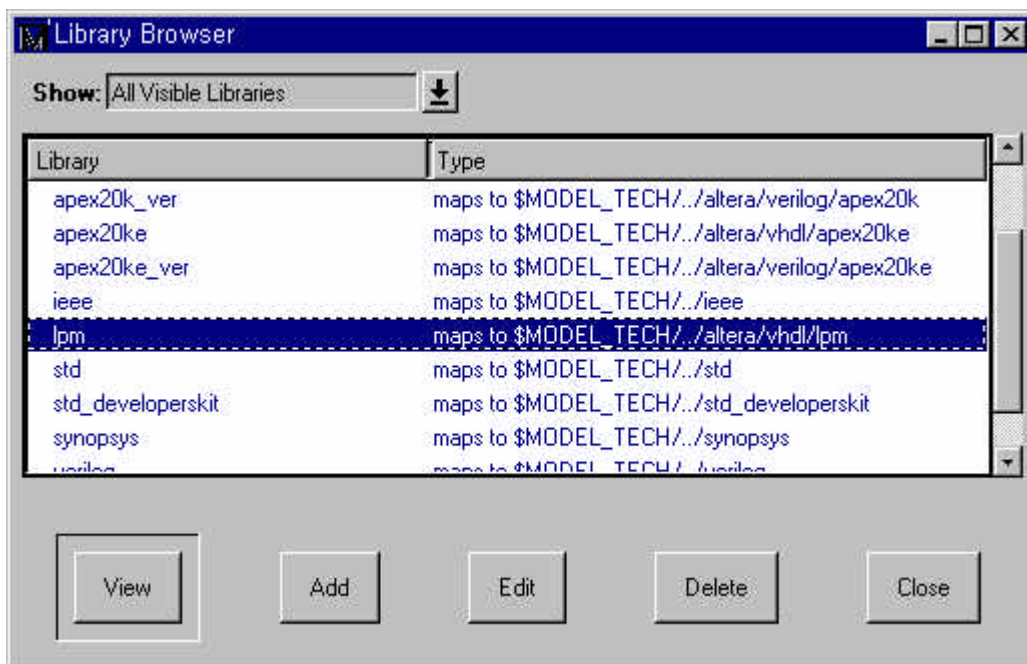


Figure 13 Library Browser Window

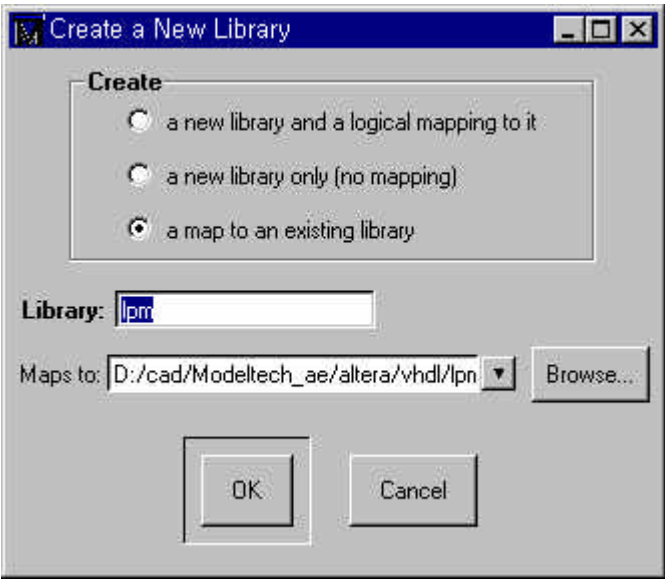


Figure 14 Create a New Library Window

a map to an existing library	Browse Button	LPM Library
Directory Path	13	
Design → Compile... Menu	test.vhd Compile	

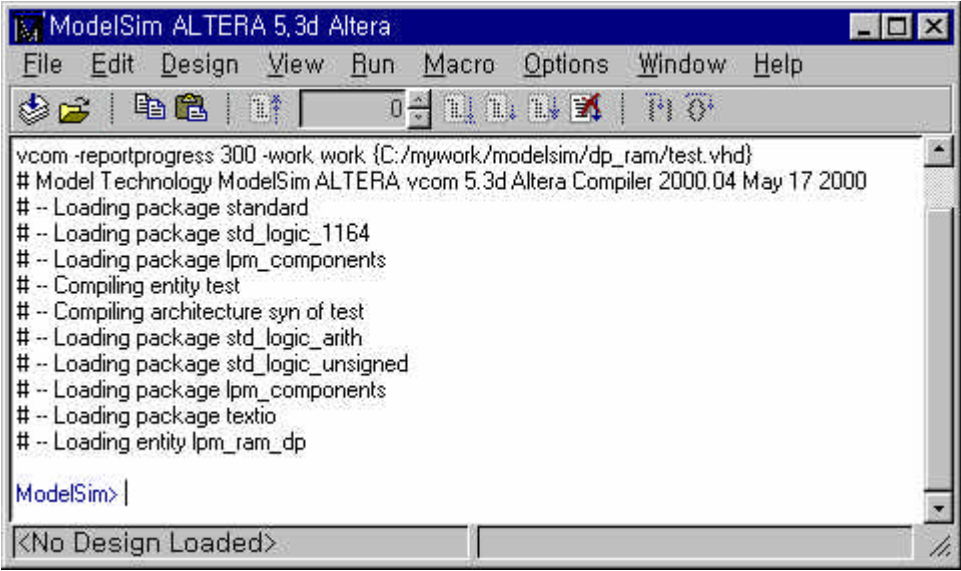


Figure 15 test.vhd Compile

15	test.vhd	Functional Simulation
Testbench	VHDL Code	Testbench File

test_dpram_func.vhd .

ModelSim Top Down Menu Design → Compile... test_dpram_func.vhd
File Compile . Compile Compile HDL Source Files Window
Done Button Compile Menu .

* Test_dpram_func.vhd Source Code

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

--use std.TEXTIO.all;
use ieee.std_logic_TEXTIO.all;

entity test_dpram is
-- port (
-- );
end test_dpram;

architecture arch of test_dpram is

constant CYC_TIME : TIME := 50 ns;

component test
port ( data : IN STD_LOGIC_VECTOR (7 DOWN 0);
      wraddress : IN STD_LOGIC_VECTOR (7 DOWN 0);
      rdaddress : IN STD_LOGIC_VECTOR (7 DOWN 0);
      wren : IN STD_LOGIC := '1';
      clock : IN STD_LOGIC ;
      q : OUT STD_LOGIC_VECTOR (7 DOWN 0));
end component;

signal clock, wren : std_logic;
signal datain : std_logic_vector(7 downto 0);
signal waddr, raddr, q : std_logic_vector(7 downto 0);

signal main_clk, reset : std_logic;
signal rd_clk : std_logic;
signal wr_clk : std_logic;
signal cnt_data : std_logic_vector(7 downto 0);

begin
U1: test port map ( data => datain,
                  wraddress => waddr,
                  rdaddress => raddr,
                  wren => wren,
                  clock => clock,
                  q => q);

wren <= '1';
clock <= main_clk;

main_clk_gen: process
begin
  main_clk <= '0';
  wr_clk <= '0';
  wait for CYC_TIME/2;
  main_clk <= '1';
  wr_clk <= '1';
  wait for CYC_TIME/2;
end process;

rd_clk_gen: process
begin
  rd_clk <= '0';
  wait for CYC_TIME;
  rd_clk <= '1';

  wait for CYC_TIME;
end process;

Reset_Gen: process
begin
  if NOW = 0 ns then
    reset <= '0', '1' after 100 ns;
    wait for CYC_TIME * 2;
  else
    wait;
  end if;
end process;

CNTDATA_GEN: process(reset, main_clk)
begin
  if reset = '0' then
    cnt_data <= (others=>'0');
  elsif main_clk'event and main_clk='1' then
    cnt_data <= cnt_data + '1';
  end if;
end process;

-- Data input from the counter value
Din_Gen: process(wr_clk,reset)
begin
  if reset = '0' then
    datain <= (others=>'0');
  elsif wr_clk'event and wr_clk='0' then
    datain <= cnt_data;
  end if;
end process;

-- Write Address Generation
WADDR_GEN: process(reset,wr_clk)
begin
  if reset = '0' then
    waddr <= (others=>'0');
  elsif wr_clk'event and wr_clk='0' then
    waddr <= waddr + '1';
  end if;
end process;

-- Read Address Generation
RADDR_GEN: process(reset,rd_clk)
begin
  if reset = '0' then
    raddr <= (others=>'0');
  elsif rd_clk'event and rd_clk='0' then
    raddr <= raddr + '1';
  end if;
end process;

end arch;

configuration CONF_TEST_DP_RAM of TEST_DPRAM is
  for ARCH
    for U1:TEST use entity work.TEST(SYN);
    end for;
  end for;
end CONF_TEST_DP_RAM;

```

ModelSim Simulation Design Loading

ModelSim Top Menu Design → Load New Design... 16

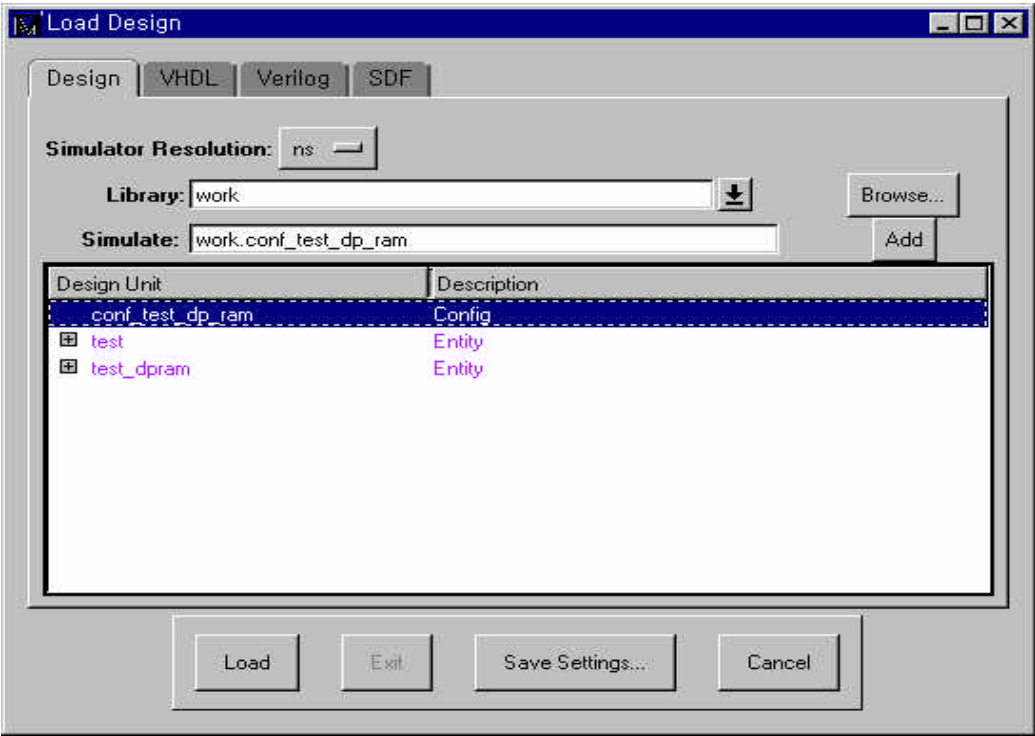


Figure 16 Load New Design Window

Load Button Loading 17

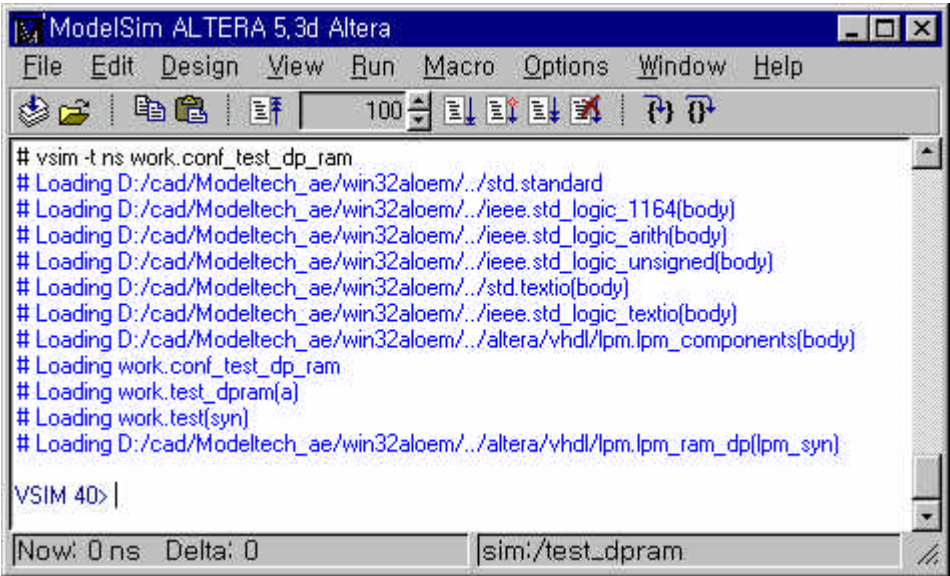


Figure 17 Design Loading Window

18 Transcripts Window View Signals <enter>, View Wave <enter>
 Waveform Window Signals Window .

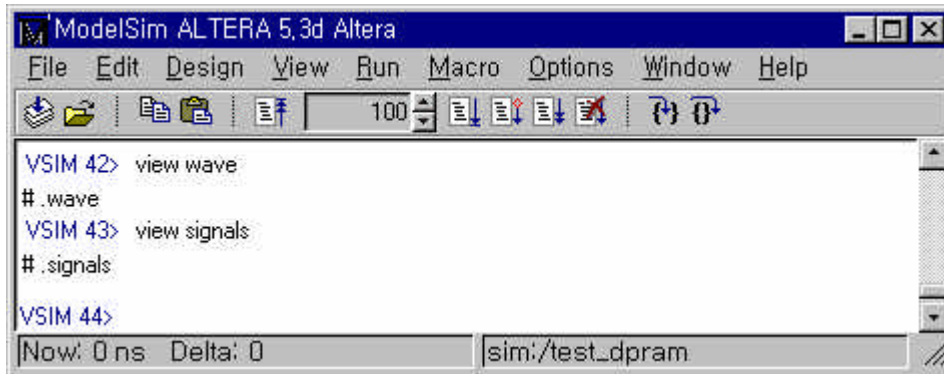


Figure 18 wave signal window

Signal Window 19 View → Wave → Signals in Region
 Waveform Window .

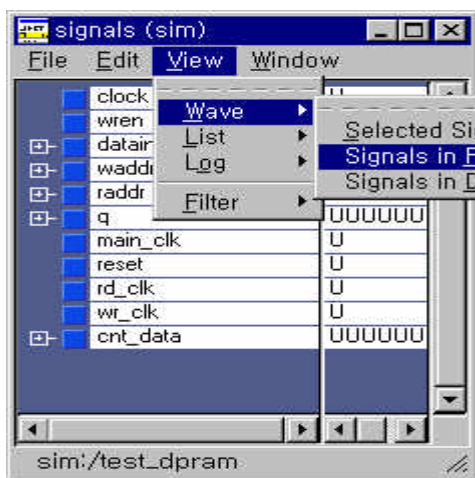


Figure 19 Signal Window

20 Loading 1000ns Simulation .



Figure 20 1000ns Simulation Window

Wave Window

가

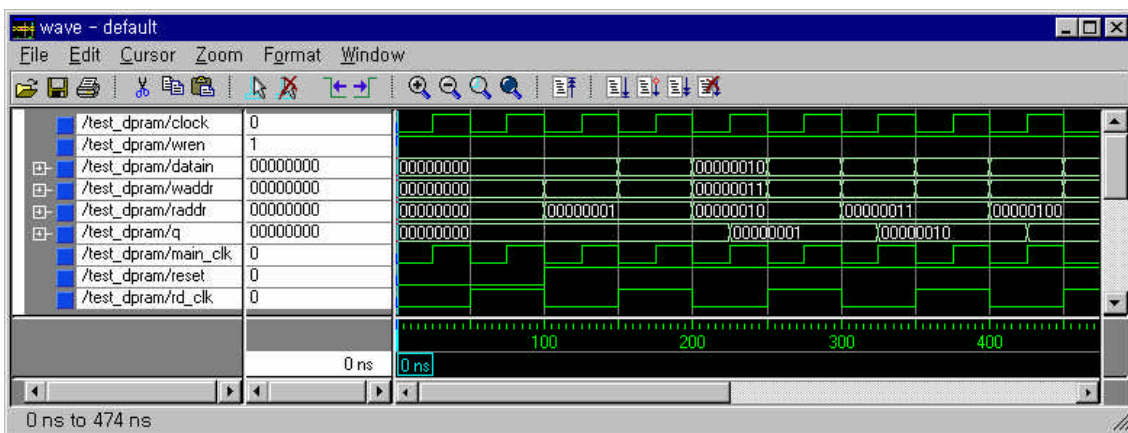


Figure 21 Functional Simulation Result Window

3. Timing Simulation

Timing Simulation Testbench File

Function Simulation Testbench File Configuration 가
 U1 Instance 가 Architecture \ EPF10K30ETC144-3 \ .

```
configuration CONF_TEST_DP_RAM of TEST_DPRAM is
  for ARCH
    for U1:TEST use entity work.TEST(\EPF10K30ETC144-3\);
    end for;
  end for;
end CONF_TEST_DP_RAM;
```

File Name test_dpram_timing.vhd .

MAX+plus II Gate-level VHDL Output Delay Output .

MAX+plus II test.vhd Project Assign → Device...
 EPF10K30ETC144-3 .

Compile Process Interfaces → VHDL Netlist Writer On Interfacs →
 VHDL Netlist Writer Settings... 22 .

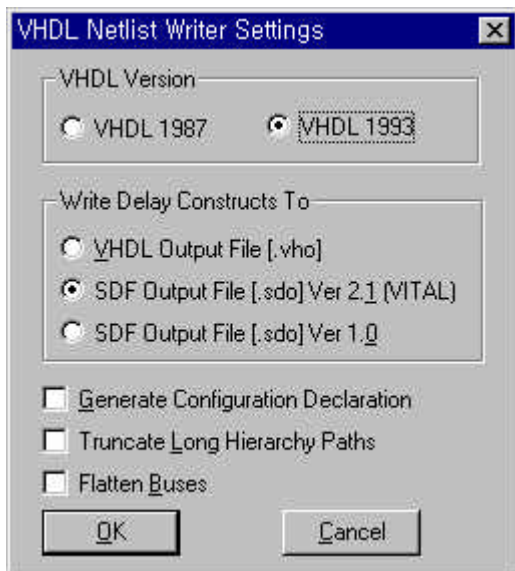


Figure 22 VHDL Netlist Writer Setting Window

Compile . test.vho test.sdo .
 test.vho test.vhd Synthesis () 가 EPF10K30E Device
 Place & Route Gate-level VHDL File
 test.sdo Standard Delay Format Net Logic Delay .
 File Timing Simulation 가 .
 ModelSim Design → Compile ... test.vho Compile .
 work library test.vho 가 . 가 test_dpram_timing.vhd Compile
 .
 Design → Load New Design... 23, 24 .

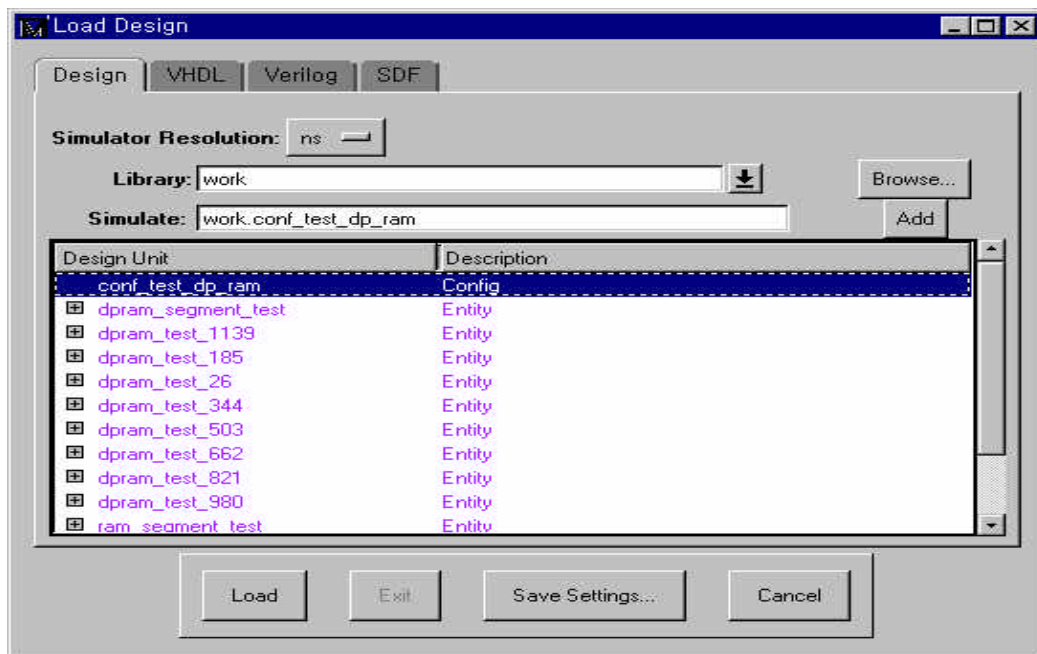


Figure 23 Load Design Window

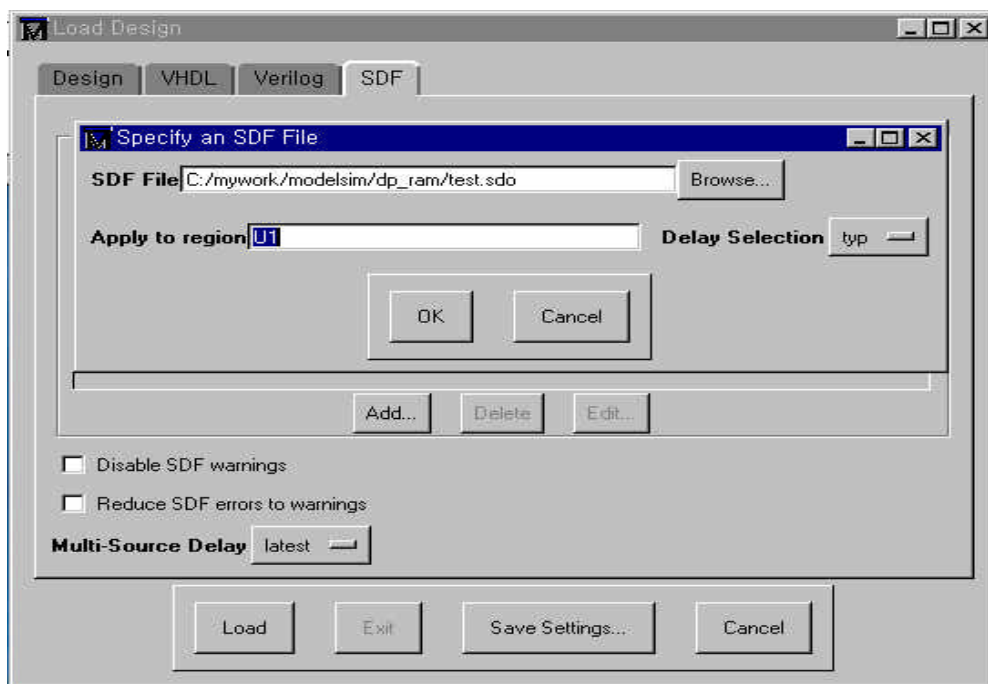


Figure 24 SDF Definition Window

Add... Button SDF File Testbench File

Instance Name Apply to Region Field . OK button Load

Button Loading .

Functional Simulation

25 Timing Simulation 가 Waveform .

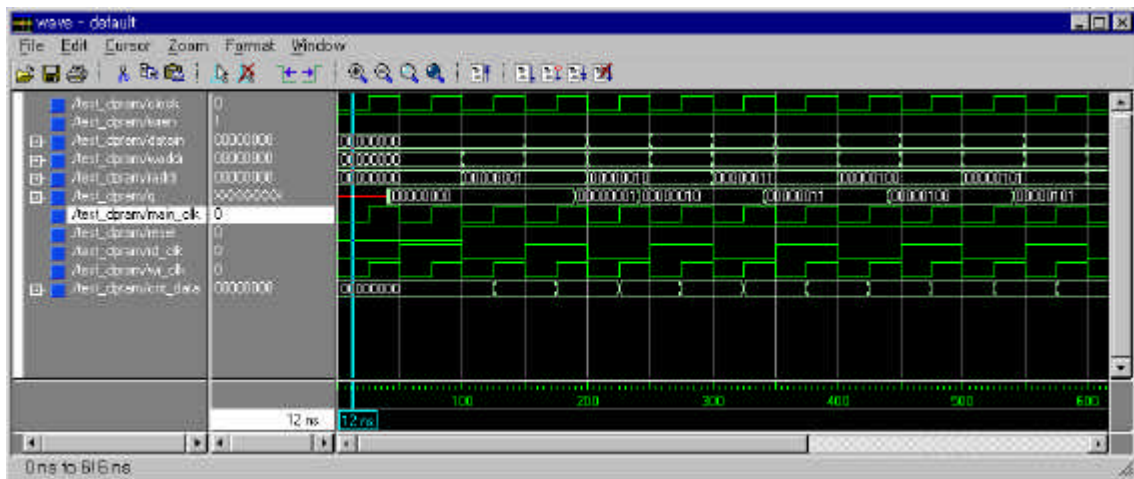


Figure 25 Result Waveform Window

Revision History

- 2000-7-13 - Ver 1.0: Initialize Release...
- 2000-8-8 - Ver 1.1: Text Modified by C.W.Yang...