System-On-a-Programmable-Chip Solutions

PLD **World Korea 2001**

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SOPC Design Using ARM-Based Excalibur Devices

Outline

- **ARM-based Devices Overview**
- **Embedded Stripe**
- **Excalibur MegaWizard**
- **Verification Tools**
  - **Bus Functional Model**
  - **Full Stripe Model**
- **Configurations**
- **Software Tools**
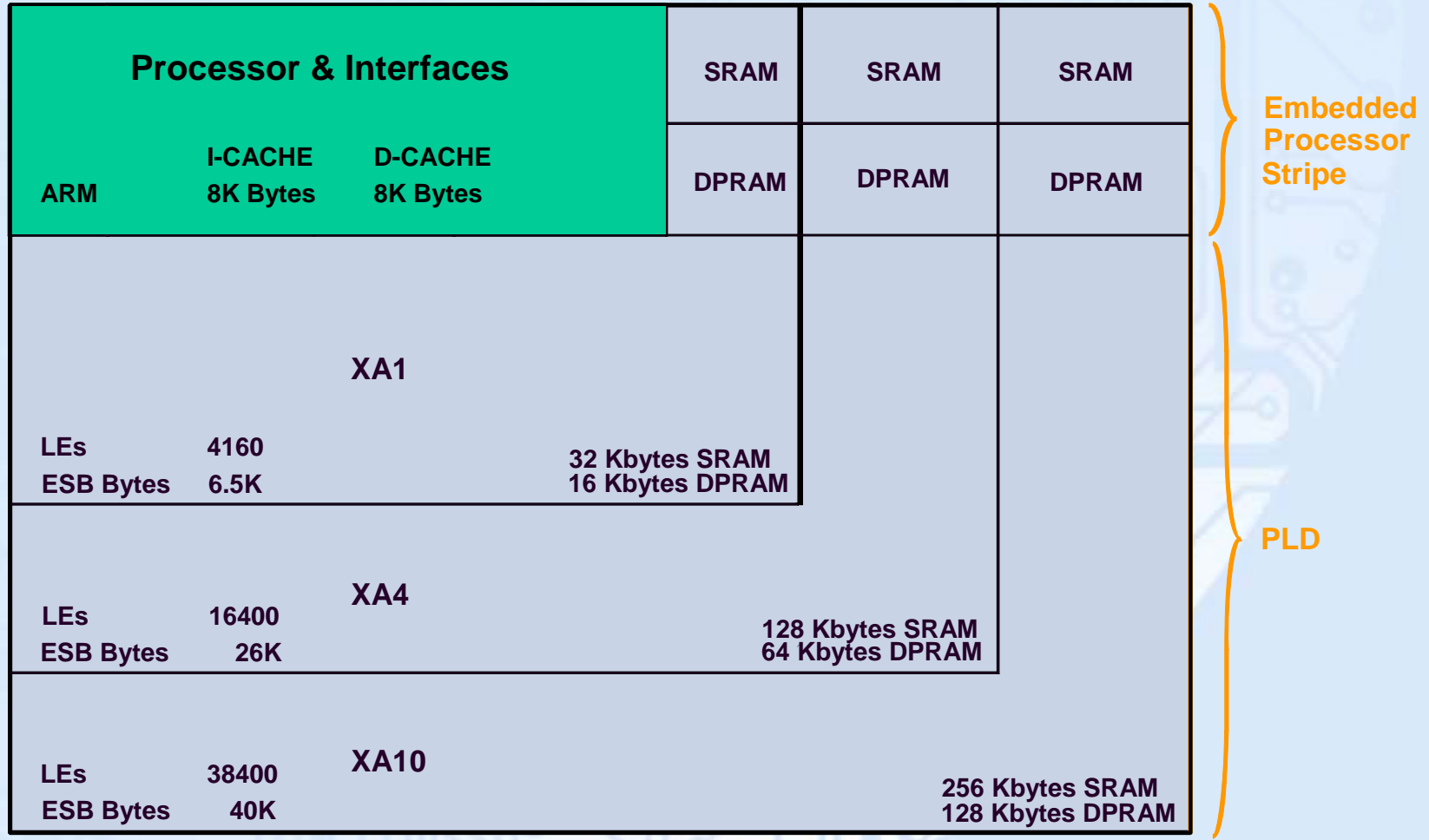- **Applications Examples**
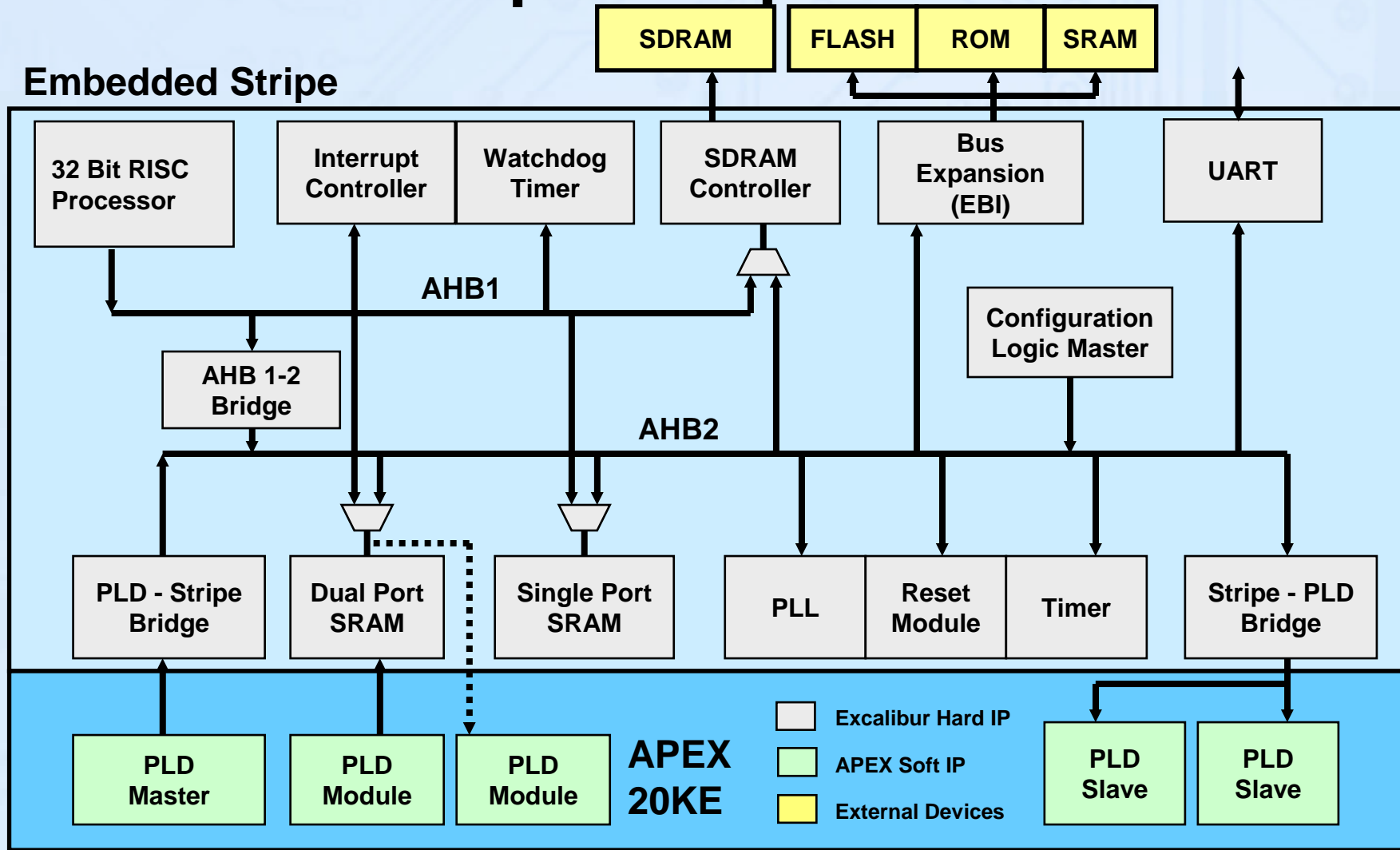- **Summary**

ARM-Based Devices Overview

Features

■ **32 Bit RISC Processor**
  – **200 MHz ARM922T™**
■ **High Performance .18 μm 8LM TSMC Process**
■ **AMBA™ Bus Architecture**
  – **Industry Standard Bus Architecture**
■ **Stripe Memory**
  – **Single Port and Dual Port**
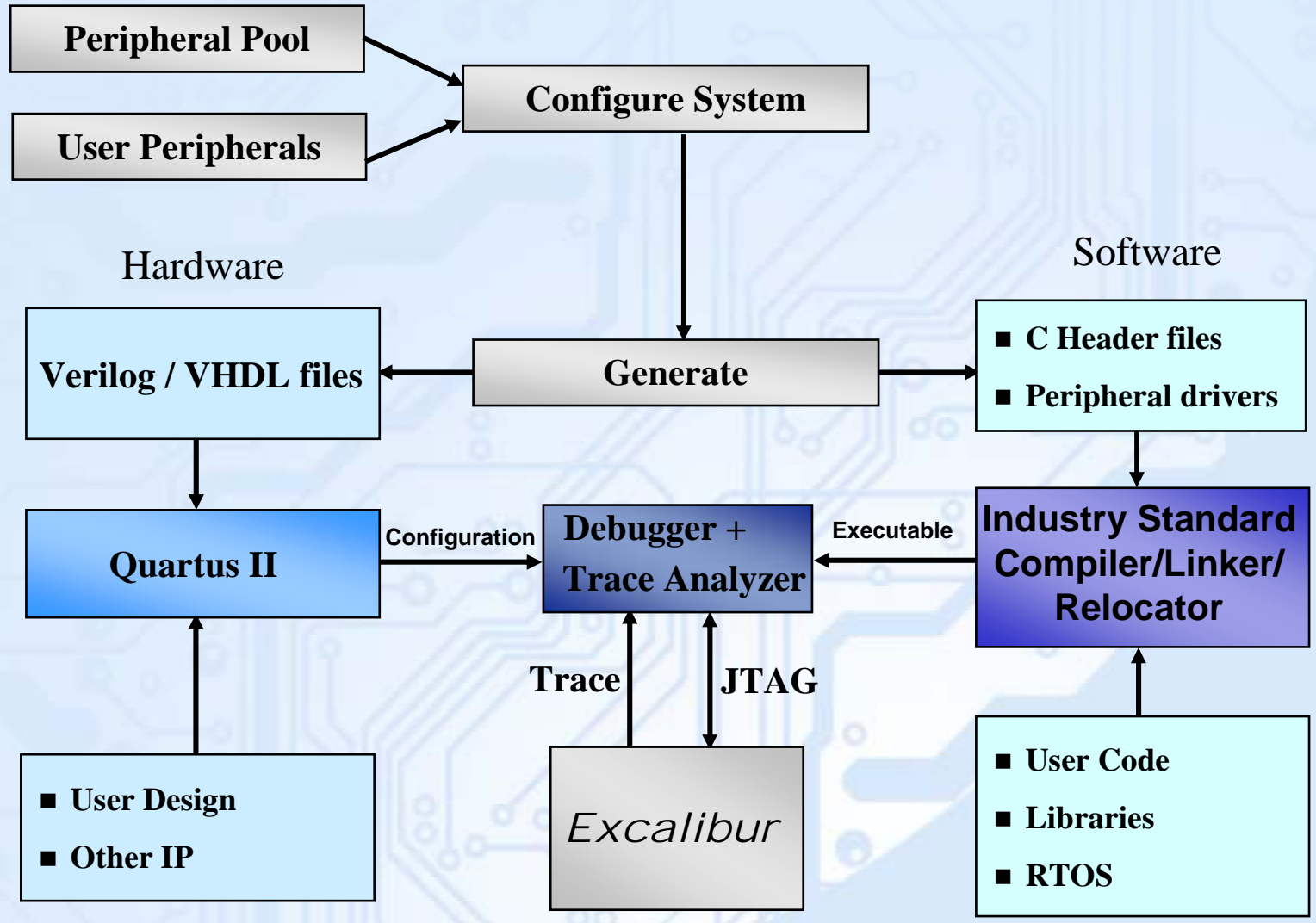■ **External Memory**
  – **SDRAM, DDRSRAM, FLASH, SRAM**

Hard Processor PLD Architecture

Processor & Interfaces		SRAM	SRAM	SRAM
	I-CACHE D-CACHE	DPRAM	DPRAM	DPRAM
ARM	8K Bytes 8K Bytes			

XA1

LEs   4160
ESB Bytes   6.5K

32 Kbytes SRAM
16 Kbytes DPRAM

XA4

LEs   16400
ESB Bytes   26K

128 Kbytes SRAM
64 Kbytes DPRAM

XA10

LEs   38400
ESB Bytes   40K

256 Kbytes SRAM
128 Kbytes DPRAM

Embedded Processor Stripe

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Excalibur Stripe Components

Excalibur Work Flow

Peripheral Pool

User Peripherals

Configure System

Hardware

Software

Verilog / VHDL files

Generate

- C Header files
- Peripheral drivers

Quartus II

Configuration

Debugger +
Trace Analyzer

Executable

Industry Standard
Compiler/Linker/
Relocator

Trace

JTAG

- User Design
- Other IP

Excalibur

- User Code
- Libraries
- RTOS

Embedded Stripe

ARM922T Processor

■ **Based on the ARM922™ (ARM920™ Derivative) and Incorporating the ARM9TDMI™**

■ **High Speed Cache (8KB Instruction + 8KB Data)**

■ **Single Cycle Repeat-rate SRAM and DPRAM**

■ **MMU Facilitates the Implementation of Real-time Operating Systems (RTOS)**

■ **200MHz on Altera® 1P/8M, 0.18u Process at TSMC**

■ **Advanced Built-in System Debug Features**

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ARM922TDMI

- **Based on ARM9TDMI core**
  - **Five stage pipeline**
  - **Harvard bus architecture**
  - **CPI of 1.5**

ARM9 -

T - **Thumb Architecture Extension**

D - **Core has Debug Extensions**

M - **Core has an enhanced Multiplier**

**I** - **Core has EmbeddedICE Logic Extension**

AMBA High Performance Bus (AHB)

- **AMBA - Advanced Micro-controller Bus Architecture**
- **Connects Embedded Stripe and PLD Devices**
- **200MHz Maximum Clock Rate**
- **32 Bit Wide Pipelined Bus**
  - **Burst transfers - one cycle per data word**
  - **Non-tristate implementation**
- **Multi-master With Distributed Address Decoding**
  - **Single-cycle bus master handover**
- **Split Transactions Extensions**
  - **Needed to fully exploit bus bandwidth in a multi-master bus**

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Stripe PLL's

- **Stripe PLL's Provide Clock Boost Multiplication Only**
  - **Default power-up operation is bypass**
  - **Program control registers through configuration logic or the embedded processor**
  - **State machine control to put PLL in bypass mode if lock is lost**
  - **Can change PLL frequency with proper software control**
- **PLL1**
  - **Clock for processor and peripheral bus**
  - **Up to 400 Mhz operation divided by 2 or 4**
- **PLL2**
  - **Clock for the SDRAM controller**
  - **Up to 266 Mhz operation**

Stripe PLL's

■ **Stripe Contains 2 PLL's**
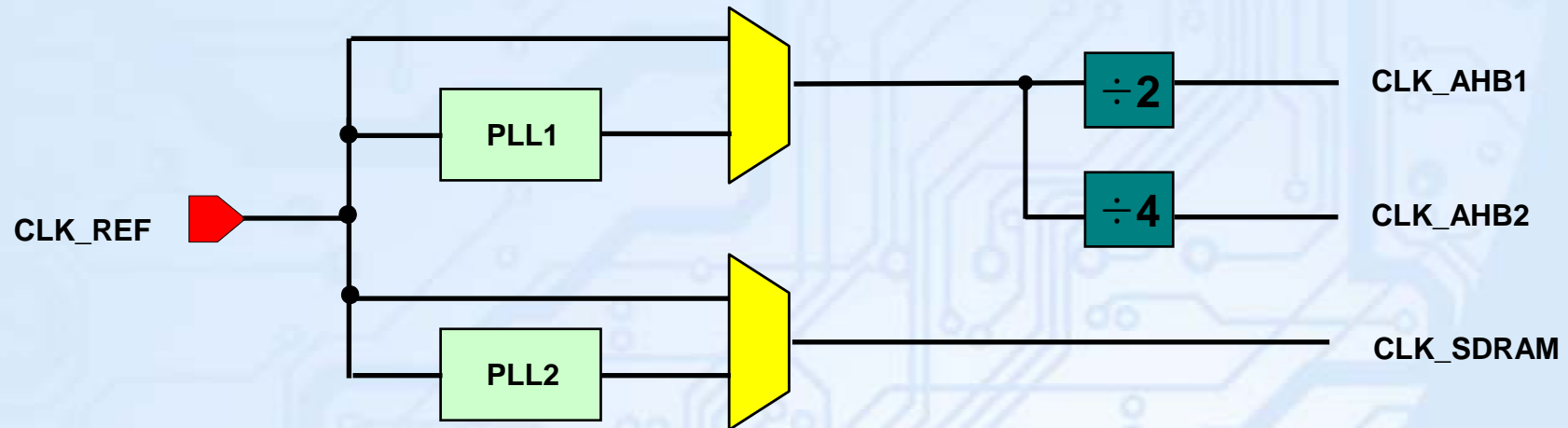
■ **PLL 1 & PLL 2 are similar to APEX PLLs**

– **Fout = CLK_REF (MHz) * M/ (N *K) where M, N, K are integers**

– **PLLs can be bypassed**

Excalibur Memory Hierarchy
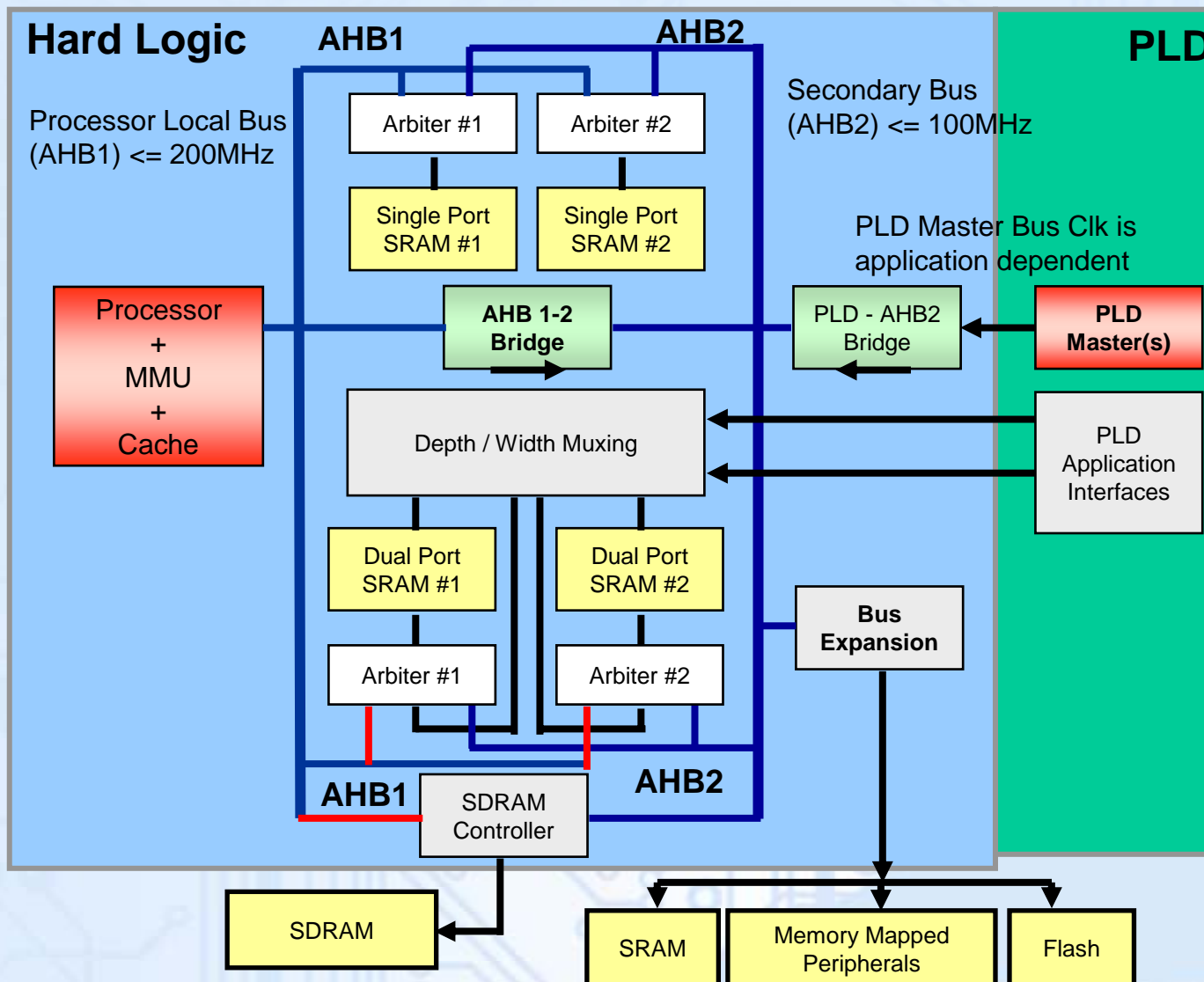
Single Port SRAM

- **Stripe Memory**
  - **2 blocks of independent addressable memory available on AHB1 or AHB2 bus**
  - **32, 128, or 256 Kbytes total depending on device size**
- **Arbiter Resolves Competition Between AHB1 and AHB2 Interfaces for Access to the SRAM**
  - **Defaults to fixed round-robin scheme with fairness**
  - **Supports locked transfers**
- **Each SRAM Block Is Byte Addressable**
- **Supports Big or Little Endian Transfers**

Dual Port SRAM

- **Stripe Memory**
  - **2 blocks available on AHB1 or AHB2 bus**
  - **16, 64, or 128 Kbytes depending on device size**
  - **Each block can itself be configured as 2 blocks for a total of 4 indpendent addressable DPRAM**
- **Available From AHB1, AHB2, or PLD**
  - **Arbiter controls access**
- **Each Block Is Byte Addressable**
- **Supports Various Widths and Depths**

Dual Port SRAM Configurations

Processor | **PLD**

Depth / Width Muxing

| DPRAM Block #1 32K x 16 | DPRAM Block #2 32K x 16 |
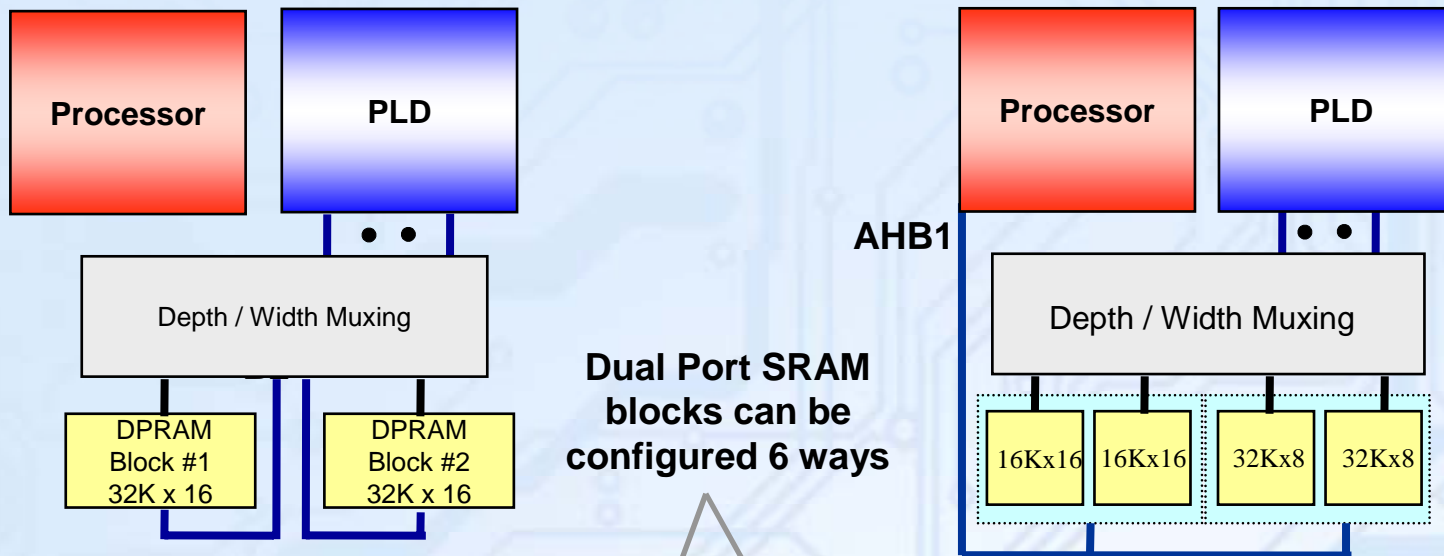
Dual Port SRAM blocks can be configured 6 ways

AHB1

Processor | **PLD**

Depth / Width Muxing

| 16Kx16 | 16Kx16 | 32Kx8 | 32Kx8 |

	Dual Port SRAM Block Configurations (Excalibur1000)
AHB Interface	-
PLD Interface	1 x 16k x 32 1 x 32k x 16 2 x 16k x 16 1 x 64k x 8 2 x 32k x 8 32k x 16 Dual Port (*)

(*) - Configuration shown here

	Dual Port SRAM Block Configurations (Excalibur1000)
AHB Interface	128 Kbytes (16Kx16) 256 Kbytes (32Kx8)
PLD Interface	1 x 16k x 32 1 x 32k x 16 2 x 16k x 16 (*) 1 x 64k x 8 2 x 32k x 8 (*) 32k x 16 Dual Port

(*) - Configurations shown here

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SDRAM Controller

- **Stripe Contains a Controller for SDRAM or DDR SDRAM External Memory**
  - **Either 16 or 32 bit SDRAM or DDR SDRAM can be connected but not both**
- **Runs Asynchronously to AHB1 or AHB2**
- **Supports Byte, Half-word, and Word Transfers**
- **Addressing**
  - **AHB buses are byte addressed, DRAM is bit addressed**
  - **DRAMS have row, column, and bank address**
  - **Number of row and column bits depends on memory used**
- **Supports 2 Blocks and up to 512 Mbytes Total of External DRAM**
- **Supports PC100/133 SDR SDRAMs and PC200/266 DDR SDRAMs**
- **SDRAM must be initialized through software control**

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Expansion Bus Interface (EBI)

- **Provides Capability to Interface to External Memory Mapped Devices**
- **Different Sizes and Types Available**
- **Rate-Adaptation Between Flash Memories or Memory Mapped Peripherals and AHB2 Bus Masters**

- **Four Chip Select Outputs**

  - **Each Address Space Can Be Configured to Operate in an 8- or 16-Bit Mode.**

  - **Bus Timing and Interface Signals Can be Configured by a Bus Master**

- **Supports Split Bus Transactions**

  - **Prevents Stalling of Other AHB2 Bus Masters**

- **Support both synchronous & asynchronous mode**

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UART

- **5 to 8 data bits**
- **1 or 2 stop bits**
- **Even, odd, stick, or no parity**
- **75 to 230,400 baud rate**
- **16-byte transmit FIFO**
- **16-byte receive FIFO.**
- **Programmable baud generator**
- **Internal diagnostic capabilities**
- **Modem communication support**

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Interrupt Controller

- **User Configurable to Three System Modes**

  – **Interrupt Sources Can Arise From Stripe and PLD**

- **Priority and Enabling Scheme**

  – **All Interrupts Disabled on Power-up**

  – **Sets Priority on Interrupt Sources**

  – **Enables or Disables Individual Interrupt Sources**

Block Diagram
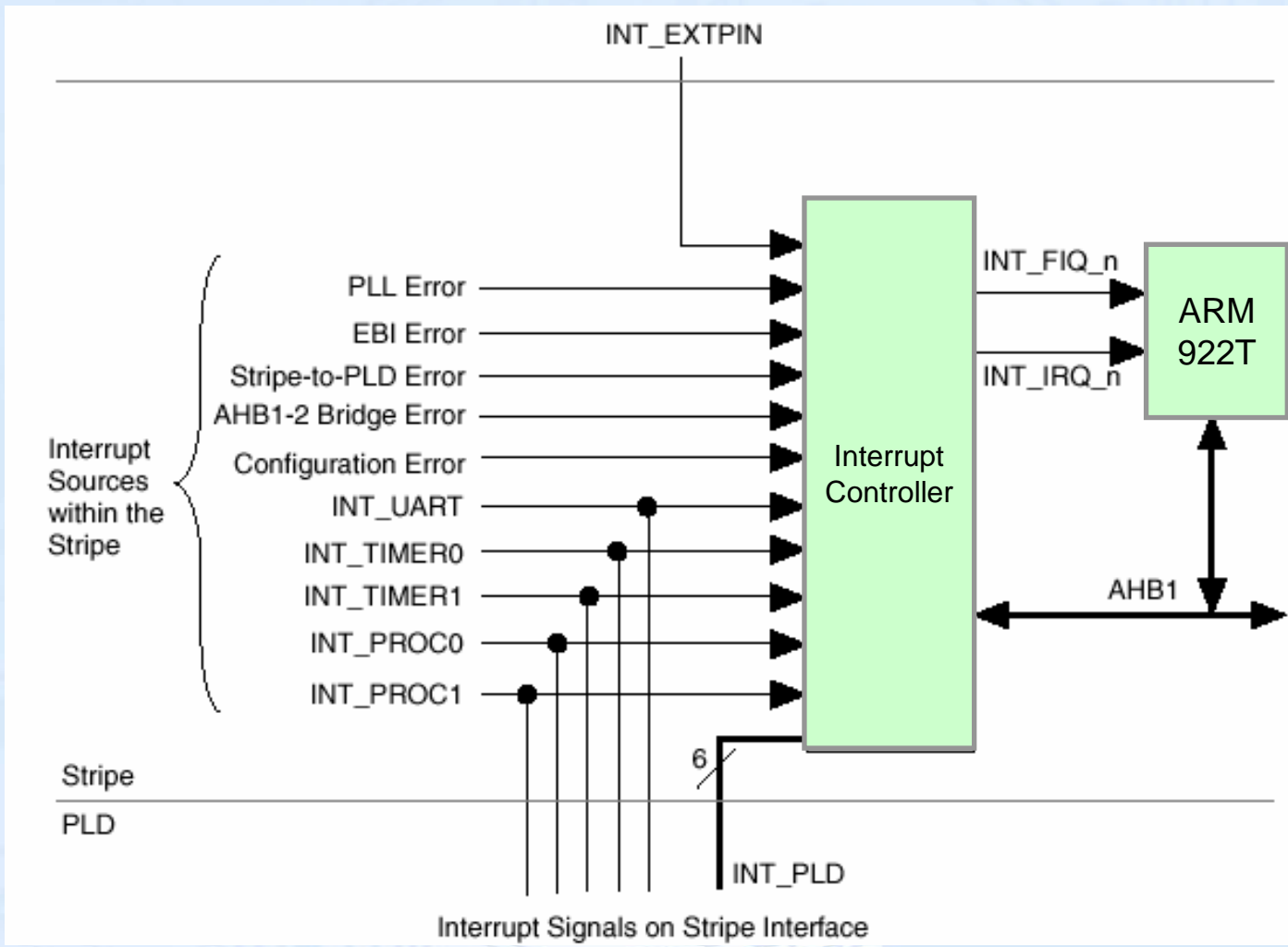
Watchdog Timer

- **Protects the System against Software / Hardware Failures**

- **One-shot Timer Resets Entire Chip When It Expires**

- **32-bit Register Interface Provides User-selected Timeouts**

  - **Up to 30s With a 33MHz Clock**

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Timer

- **Dual-Channel Timer**
- **32 Bit Prescaler**
- **32 Bit Timer Register**
- **Three Operating Modes**
  - Free running interrupt (heartbeat)
  - Software controlled start/stop (interval timer) with interrupt on limit
  - One-shot interrupt after programmable delay

Reset & Mode Control

- **PLD power-on reset**
- **Resets from external sources**
  - **Configuration pin nCONFIG**
  - **External reset pin (bi-directional open drain pin, supplying reset output to flash devices)**
  - **External power-on reset**
- **Resets from internal sources**
  - **Software watchdog timer reset**
  - **JTAG module**
  - **Configuration error**

Excalibur ARM MegaWizard

Excalibur MegaWizard

- **Select ARM®-Based™ Excalibur™**
  - – **Easily create the desired stripe configuration**
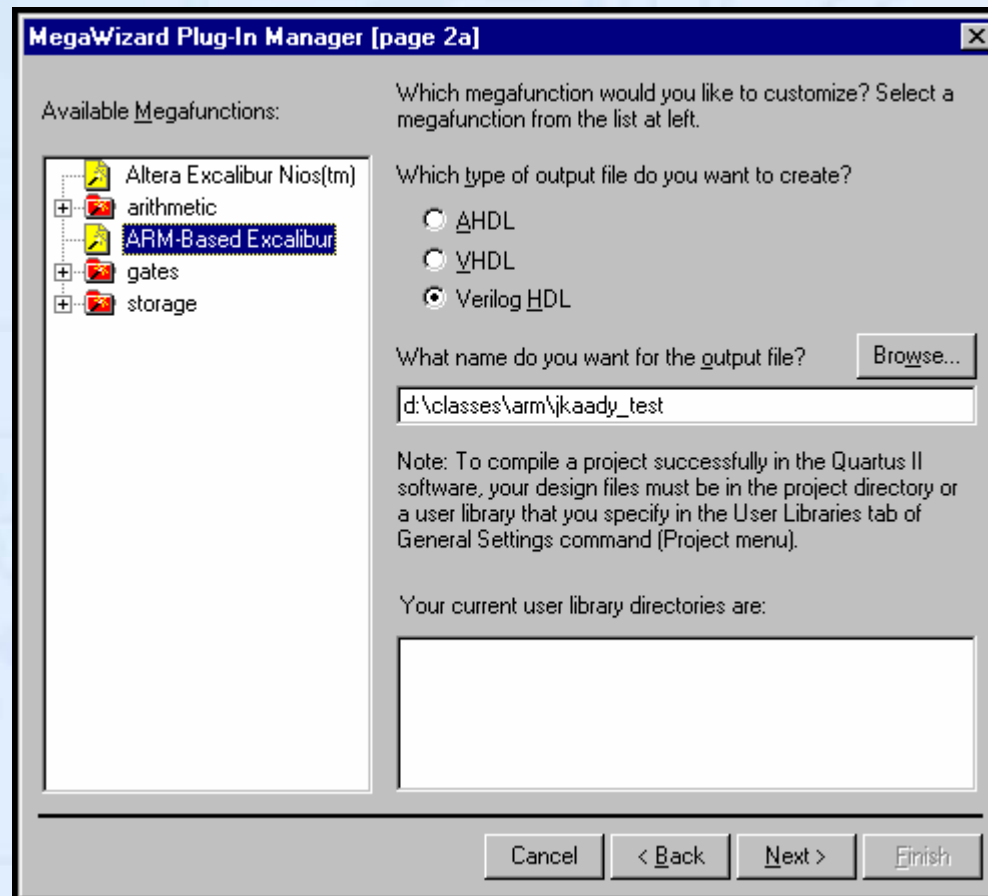
MegaWizard

Select family and device

Hold processor in reset?

Boot from FLASH?

Endianess

Reserve pins

Megawizard Plug-In Manager - Excalibur [Page 3 of 7]

This page allows you to select and configure the Excalibur device to suite your particular application. It also allows you to enable or disable those 'stripe' modules that require external access and therefore pins to be reserved on the Excalibur device.

Select Excalibur family   Excalibur_ARM

Select available device   EPXA10

Reset operation

If the processor is held in reset, it can only be released by a write to the 'stripe' Boot control register by one of its two remaining bus masters.

☐ Do you want the processor to be held in reset?

☑ Do you want to Boot from FLASH?

Byte order

⦿ Little endian   ◯ Big endian

Reserve pins

Do you want to reserve pins for any of the following 'stripe' modules?

☑ EBI (FLASH)   Outputs Slow slew rate   Inputs 3.3V LVTTL
☑ SDRAM   Outputs Fast slew rate   Inputs SSTL 2
☑ UART   Outputs Slow slew rate   Inputs 3.3V LVTTL
☐ Trace   Outputs Fast slew rate   No Inputs

Cancel   ◁ Prev   Next ▷   Finish

MegaWizard

Select the AHB2 to PLD bridges

Select the Interrupts

Megawizard Plug-In Manager - Excalibur [Page 4 of 7]

This page allows you to configure the interface between the 'stripe' and the PLD.

Bridges

Note: The PLD-TO-STRIPE bridge allows a master or masters in the PLD to access resources in the 'stripe'. Similarly the STRIPE-TO-PLD bridge allows masters in the 'stripe' access to resources in the PLD.

☑ Do you want to use the STRIPE-TO-PLD bridge (Master Port)?

☑ Do you want to use the PLD-TO-STRIPE bridge (Slave Port)?

Interrupts

Note: If you choose to implement an interrupt controller within the PLD then you must also select the mode of operation for the main interrupt controller (in the 'stripe'), which will determine how these PLD interrupt request signals are treated.

If you select Mode 3 you will also need to configure the PLD_MS register in the 'stripe'. Please see the Excalibur data sheet for more details.

☑ Do you want to use the STRIPE-TO-PLD interrupt sources?

☐ Do you want to use the PLD-TO-STRIPE interrupt sources?

Select PLD interrupt mode   Mode 3 - Six individual requests

Trace / Debug

☑ Do you want to use processor debug extensions?

☐ Do you want to use processor trace extensions?

Cancel   ◁ Prev   Next ▷   Finish

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MegaWizard

External clock reference

AHB1 / AHB2 clock settings

SDRAM clock setting

MegaWizard

Enter the base address & size

Automatic checking for overlapping regions or incorrect base address

MegaWizard

SRAM0,SRAM1 DPRAM0, DPRAM1 Memory Map

Combine dual port?

DPRAM0 setting DPRAM1 setting

MegaWizard

Memory Type

Timing Parameter

Address bits

Megawizard Plug-In Manager - Excalibur [Page 6 of 7]

This page allows you to configure all of the memory regions of the Excalibur device. You can adjust the base address and size of any region, together with the region parameters (if any), by editing or selecting the controls within the 'Memory map' area.

SDRAM0, SDRAM1
Memory map

Select device and port width

Click on the Show details button

Memory map

Registers	7FFFC000	16K
SRAM0	00020000	16K
SRAM1	00040000	16K
DPRAM0		OFF
DPRAM1	00080000	128K
SDRAM0	00800000	8M	>
SDRAM1		OFF
EBI0 (FLASH)	0000000	32K
EBI1		OFF
EBI2		OFF
EBI3		OFF
PLD0		OFF
PLD1		OFF
PLD2		OFF
PLD3		OFF

No errors detected.

You have the choice of selecting one of four reference SDRAM devices, or a user custom device.

Note: The reference SDRAM parameters assume a 133MHz speedgrade for all the x16 devices, and a 166MHz speedgrade for the x32 device.

SDRAM settings

Device Micron MT48LC4M16A2

SDRAM port width

◉ 32-bits   ○ 16-bits

Show details >>

Cancel | Prev | Next | Fin

Custom

SDRAM memory type

◉ SDR   ○ DDR

SDRAM timing

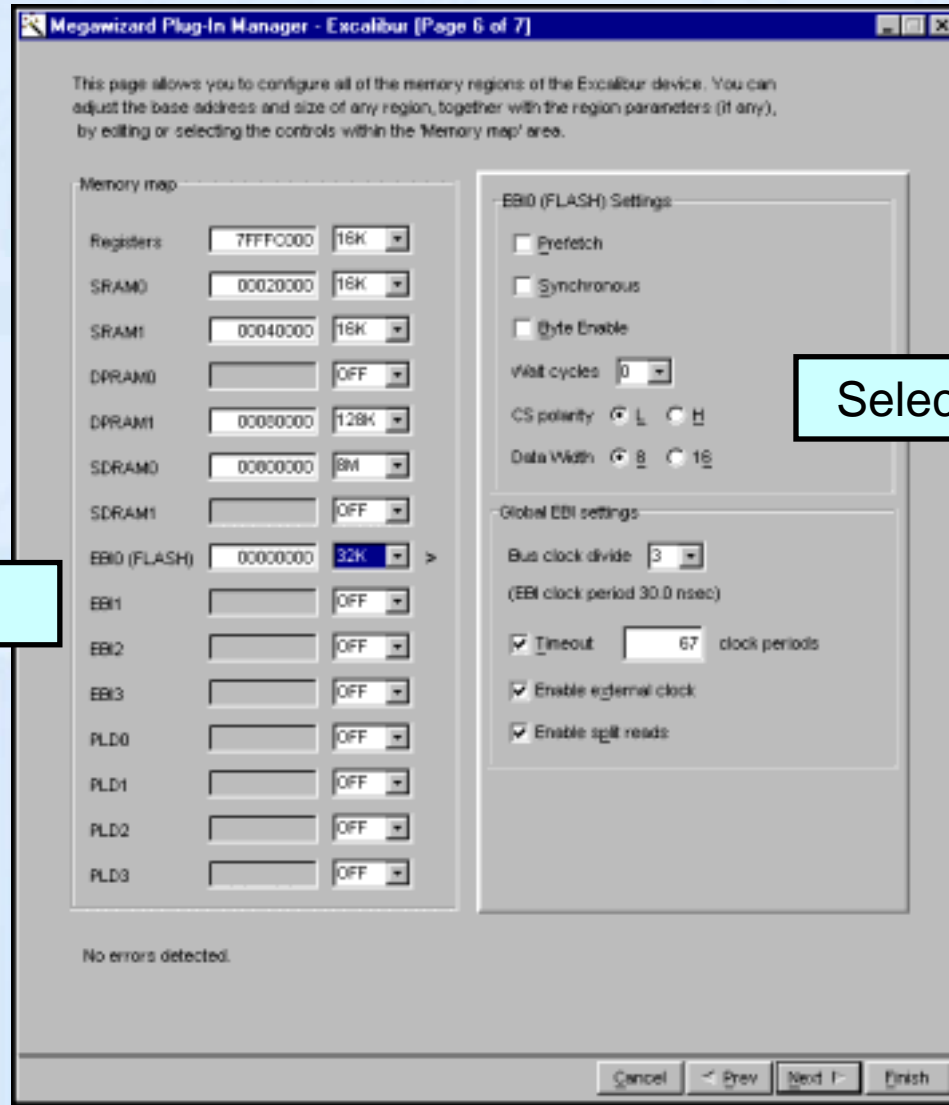|		
Active to Read or Write delay (RCD)	20	ns
Active to Precharge command (RAS)	45	ns
Active bank A to Active bank B command (RRD)	15	ns
Precharge command period (RP)	20	ns
Write recovery time (WR)	15	ns
Active to Active command period (RC)	65	ns
Auto Refresh period (RFC)	75	ns
Auto Refresh interval (RFSH)	15625	ns
CAS latency (CL)	2	
Burst Length (BL)	4	

SDRAM size

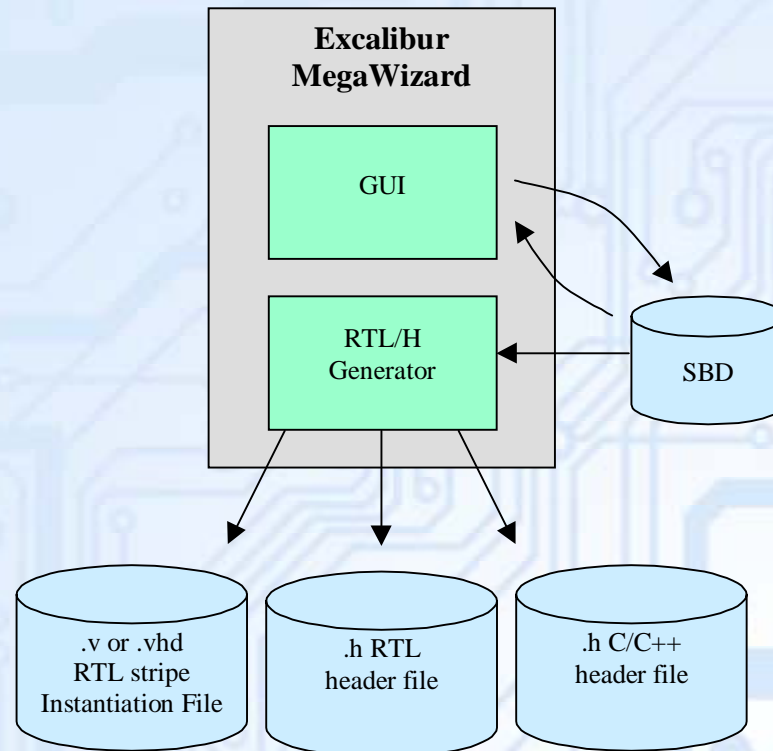|	
Number of row address bits (ROW)	12
Number of column address bits (COL)	8
Number of bank address bits (BA)	2

Cancel | OK

MegaWizard

Excalibur Megawizard

■ **A Megawizard in Quartus II will assist the customer to define the Memory Map, etc**

Verification Tools

Bus Functional Model

■ **Verifies the ability of PLD Peripherals to AHB Protocol**

– **AMBA AHB Masters and Slaves**

■ **Models AHB Transactions**

– **Includes Master Port and Slave Port Bus Transactors**

– **Models AHB Master and AHB Slave - Accepts and Transmits AHB Protocol Signals**

– **Does** Not **Model**

● **Excalibur ARM Stripe**

● **Stripe-PLD Bridge**

● **PLD-Stripe Bridge**
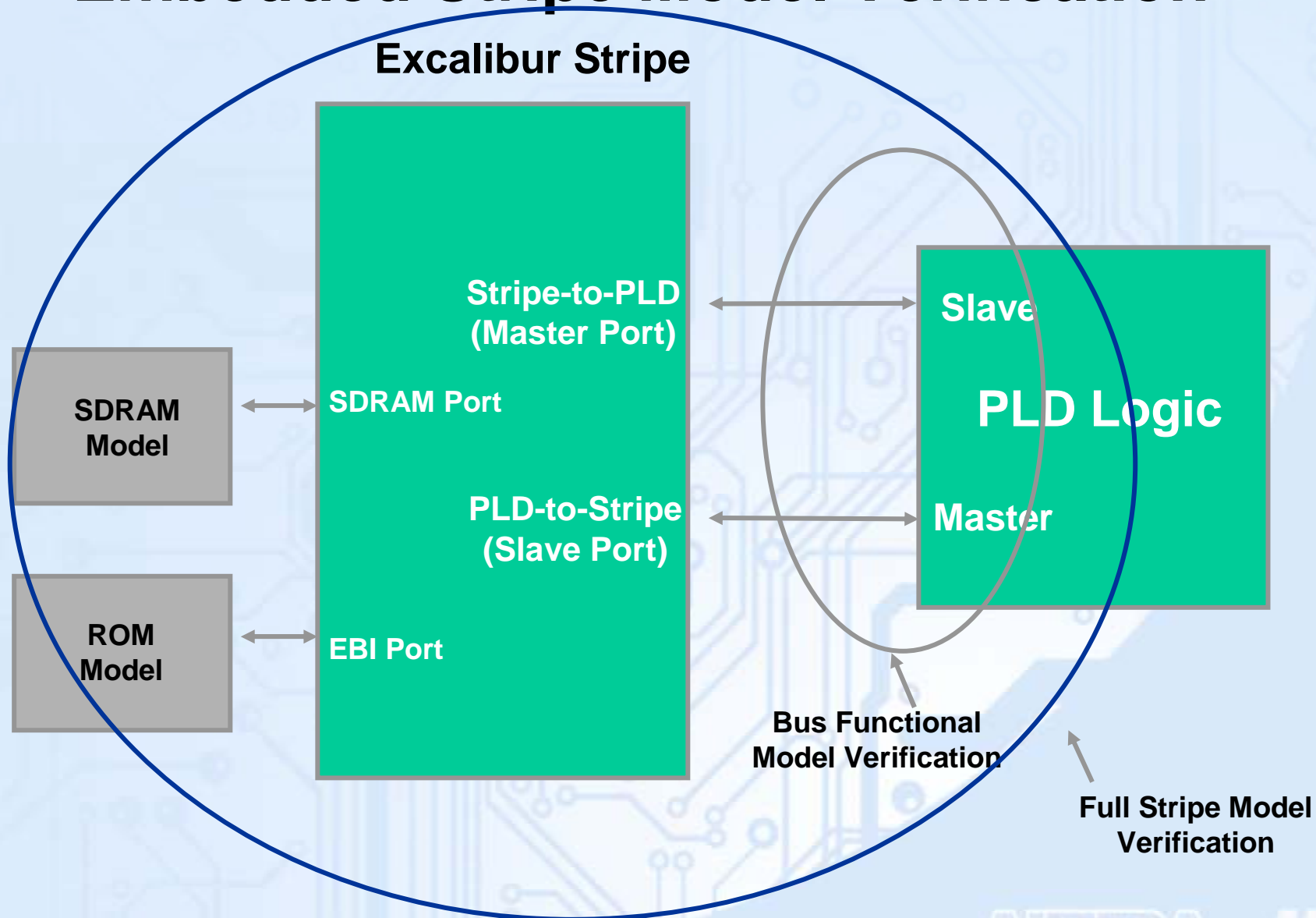
Cycle Accurate Stripe Model

- **Processor**
- **Timer**
- **Interrupt Controller**
- **UART**
- **EBI**
- **DPRAM, SRAM**

- SDRAM Controller
- AHB1-2 Bridge
- Stripe-to-PLD Bridge
- PLD-to-Stripe Bridge
- PLLs (limited model of behavior)
- PLD Configuration Not Modeled
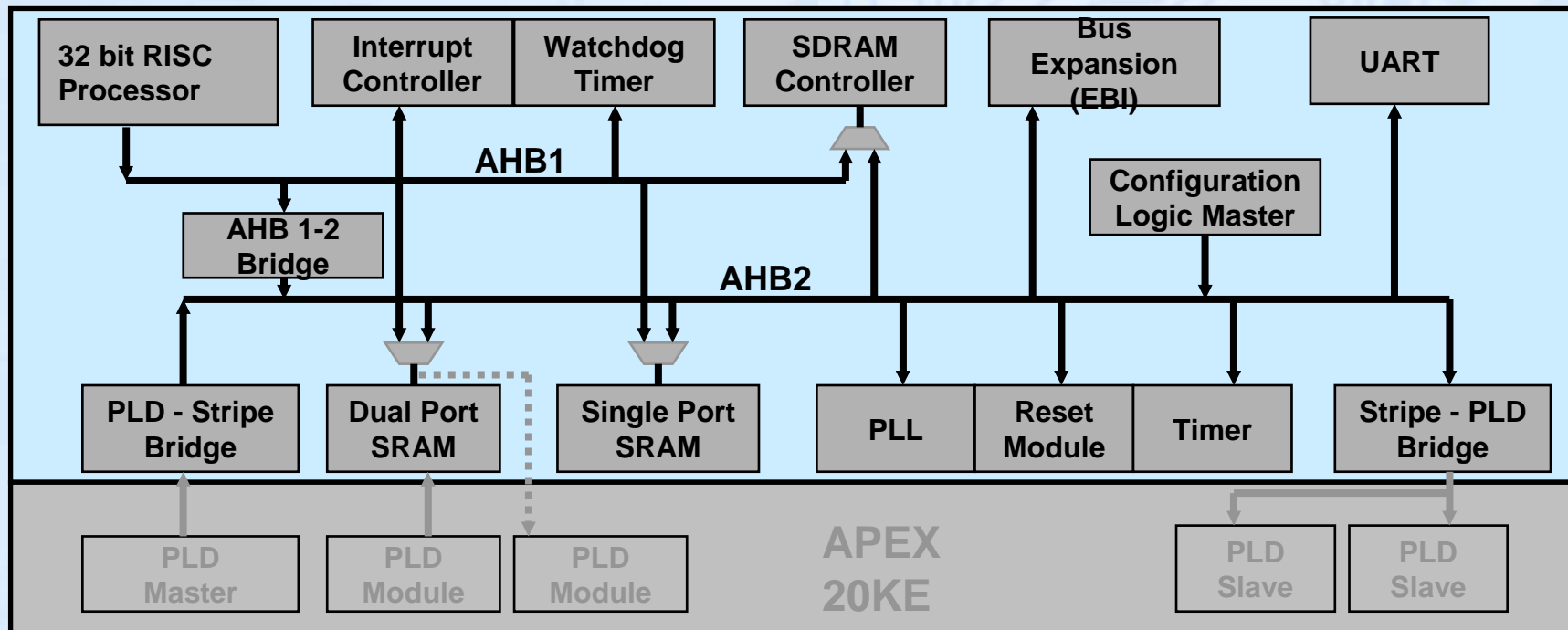
ALTERA MJL

Verification Tool Flow
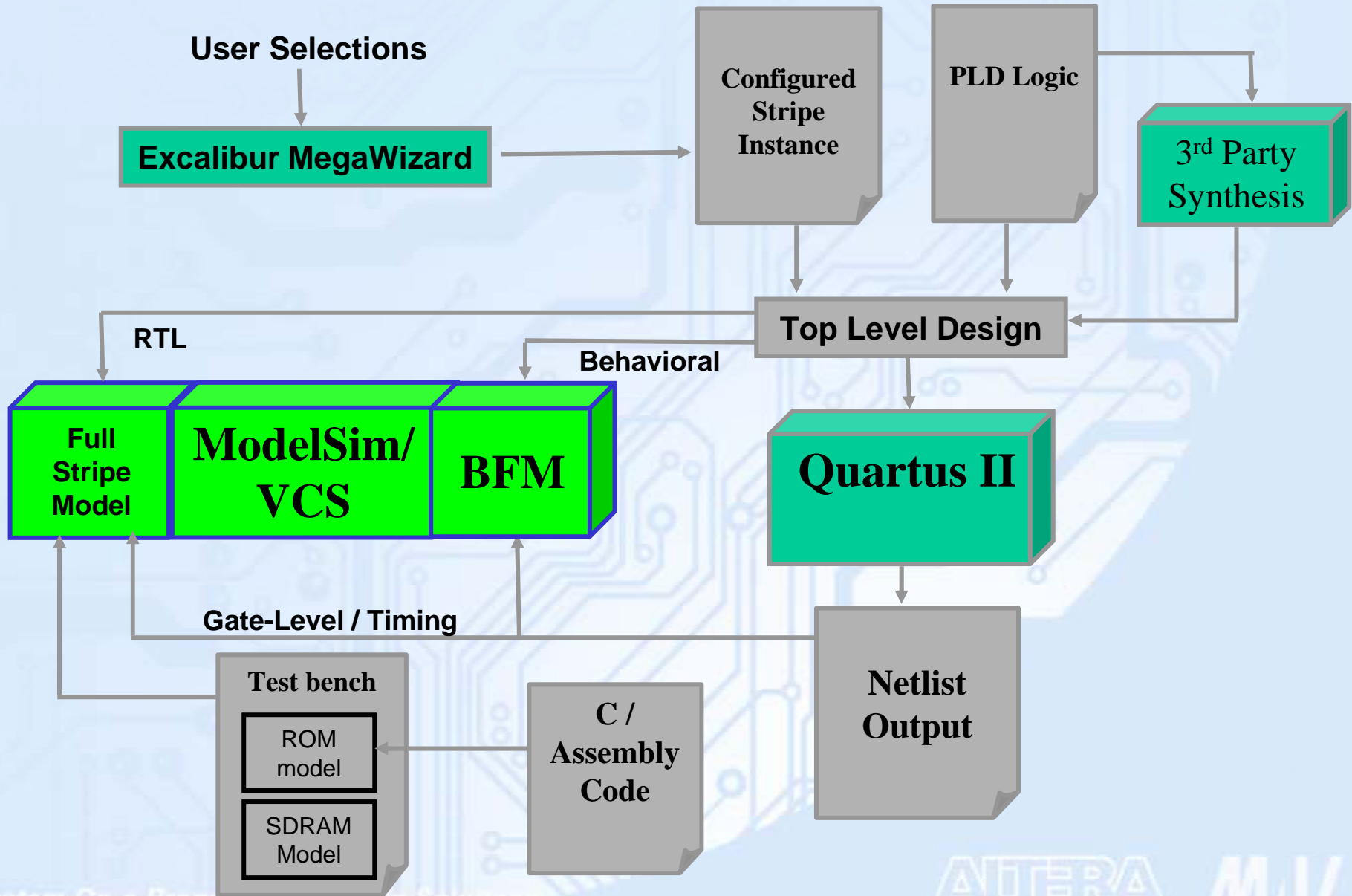
Configuration Methods

Configuration Methods

- **Processor Centric**
  - **Boot From Flash**
  - **Possible for Multiple PLD Images**
- **PLD Centric**
  - **Passive Serial**
  - **Passive Parallel**
  - **JTAG**

Processor-Centric Configuration Mode

Excalibur ARM Processor

| Config Port | EBI | Processor | SRAM | Embedded JTAG Port |

Configuration Unit

Config Registers

Embedded Stripe

PLD

16 or 8 Bit Flash Memory
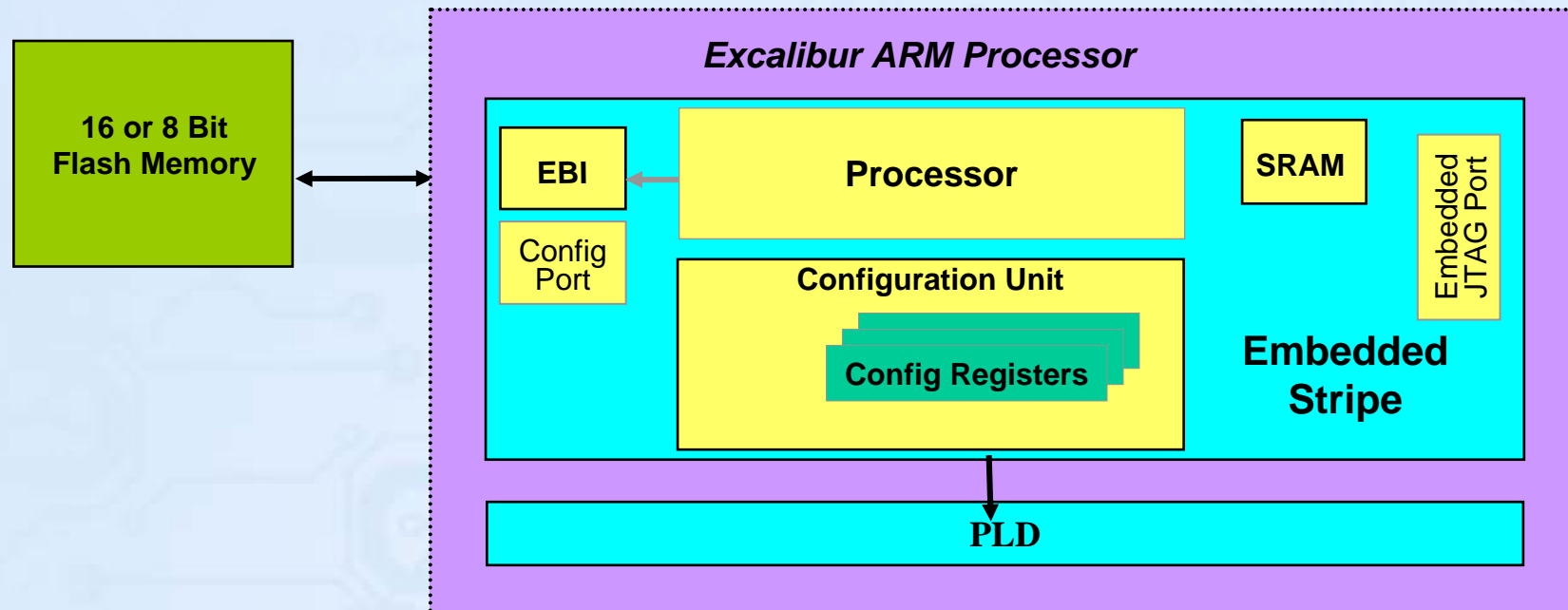
- **Processor boots from External Flash and Configures Embedded Stripe and PLD**
- **First-time flash programming can be done using JTAG**

Configuration File in Flash

Excalibur ARM Processor

EBI

8-bit/16-bit FLASH

intel .HEX
=
.HEX
+
.SBI
+
.SBD

Quartus II
OR
Industry Standard
Compiler/Linker/
Relocator

- User S/WDesign
- Libraries
- RTOS

Quartus II

- User H/W Design
- Other IP
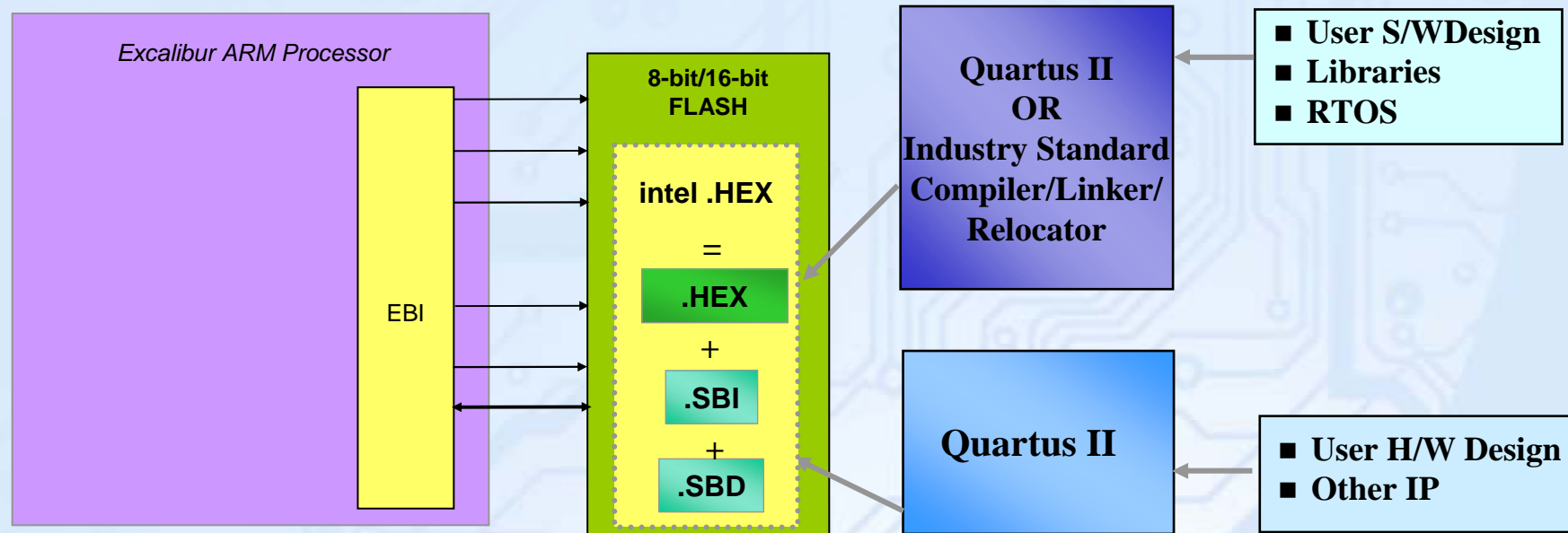
- **The intel .HEX programming file is generated by a combined effort of Quartus II and external softwares**
  - **The .HEX component is made by Quartus II in Software Mode or by external software tool**
  - **The .SBI component is made by Quartus II in Hardware mode**
  - **The .SBD component is made by the Excalibur MegaWizard**

Configuration Files in PLD-centric Mode

- User S/WDesign
- Libraries
- RTOS

Quartus II
OR
Industry Standard
Compiler/Linker/
Relocator

.SOF
.POF/
.RBF/
.TTF/
.HEXOUT
=

.HEX

+

.PSOF

+

.SBD

Dowload Cable

.SOF

OR

Serial / Parallel
PLD
Configurator

.POF/
.RBF/
.TTF/
.HEXOUT

Excalibur ARM Processor

Config Port

- User H/W Design
- Other IP

Quartus II

Software Tools

Quartus II SoftMode

Software Settings

General | CPU | C/C++ Compiler | Assembler | Linker | Library

You can select the processor architecture and toolset.

Changes apply to Software settings 'Debug'

Processor architecture: ARM922T   Byte order: Little endian

Software toolset: ARM   Output type: Intel hex

Custom build command-line: make - f debug.mak

Programming file generation

Post build command-line: make -f flashimage.mak

Include PLD configuration file: chiptrip.bof

Description:

OK   Cancel   Apply

- **Supports Excalibur Processors**
 - **ARM®, Nios™**
- **Integrated Software Development Environment**
- **Generate combined programming files**
  - **PLD configuration plus software code**

ARM Software Development Tools

- **Altera provides ARM Developer Suite (ADS lite), comes free with Quartus license.**
  - ARMasm (ARM Assembler)
  - Compilers (ARM C/C++ Compiler)
  - ARMlink (ARM linker)
  - AXD – ARM debugger
  - Adwu – ARM debugger for windows/Unix
  - Fromelf – Format Changer (ELF to other formats)
- **Altera ADS will be supported with Quartus only**
- **Full version ADS can be obtained from ARM.**
- **GNU ARM tools will also be offered by Altera**

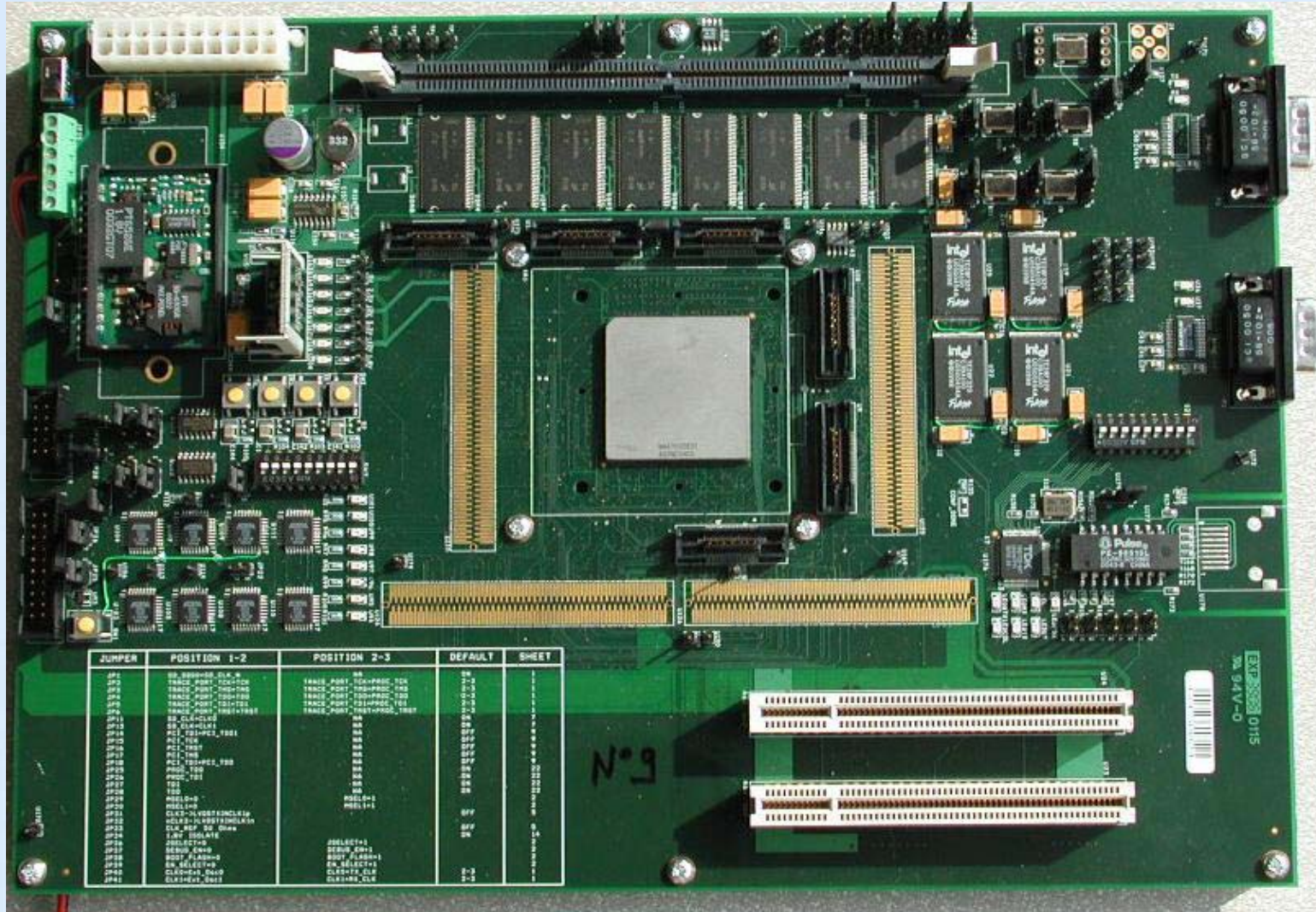# ARM Mult-ICE & Multi-Trace Solution
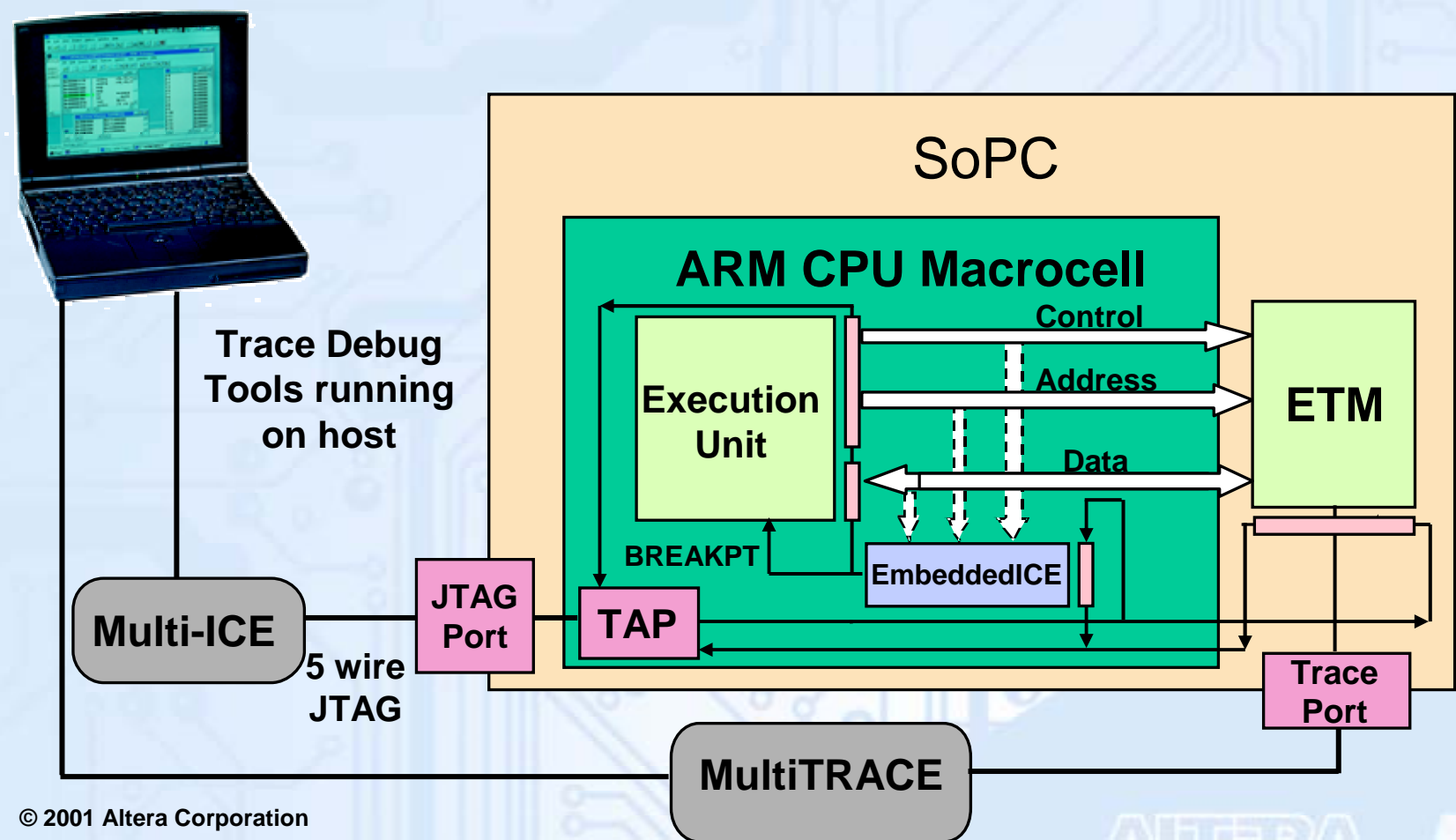
ARM-base device RTOS support

- **VxWorks AE**
- **Nucleus**
- **Linux**
- **Enea OSE**

RTOS BSP will be provided for our Excalibur Development Board

EPXA10 development board

EPXA10 Development Board Features

- **Interconnects**
  - **10/100 Ethernet with full and half duplexing**
  - **2 PCI connectors**
  - **Two RS232 ports**
- **Memory subsystem**
  - **128Mbyte DDR sited on board for layout issues**
  - **Up to 512MB SDR SDRAM in a DIMM socket**
  - **16MB flash memory**
- **Other hardware features**
  - **ByteBlaster/MasterBlaster connectors(download, debug, SignalTap)**
  - **Switches, LEDs, DIP switches**
  - **EPC2 programming capabilities**
- **Clock Flexibility**
  - **Crystal on the input clock can be changed**
  - **External clock generator can be used**

(53)

Excalibur MPLD

- **Pin-Compatible, Drop-In Replacement for Excalibur Devices**
- **No Extra Effort on Customer Side**
- **Considerable Price Reduction**
- **Timing, I/O and Placement Constraints Are Preserved**
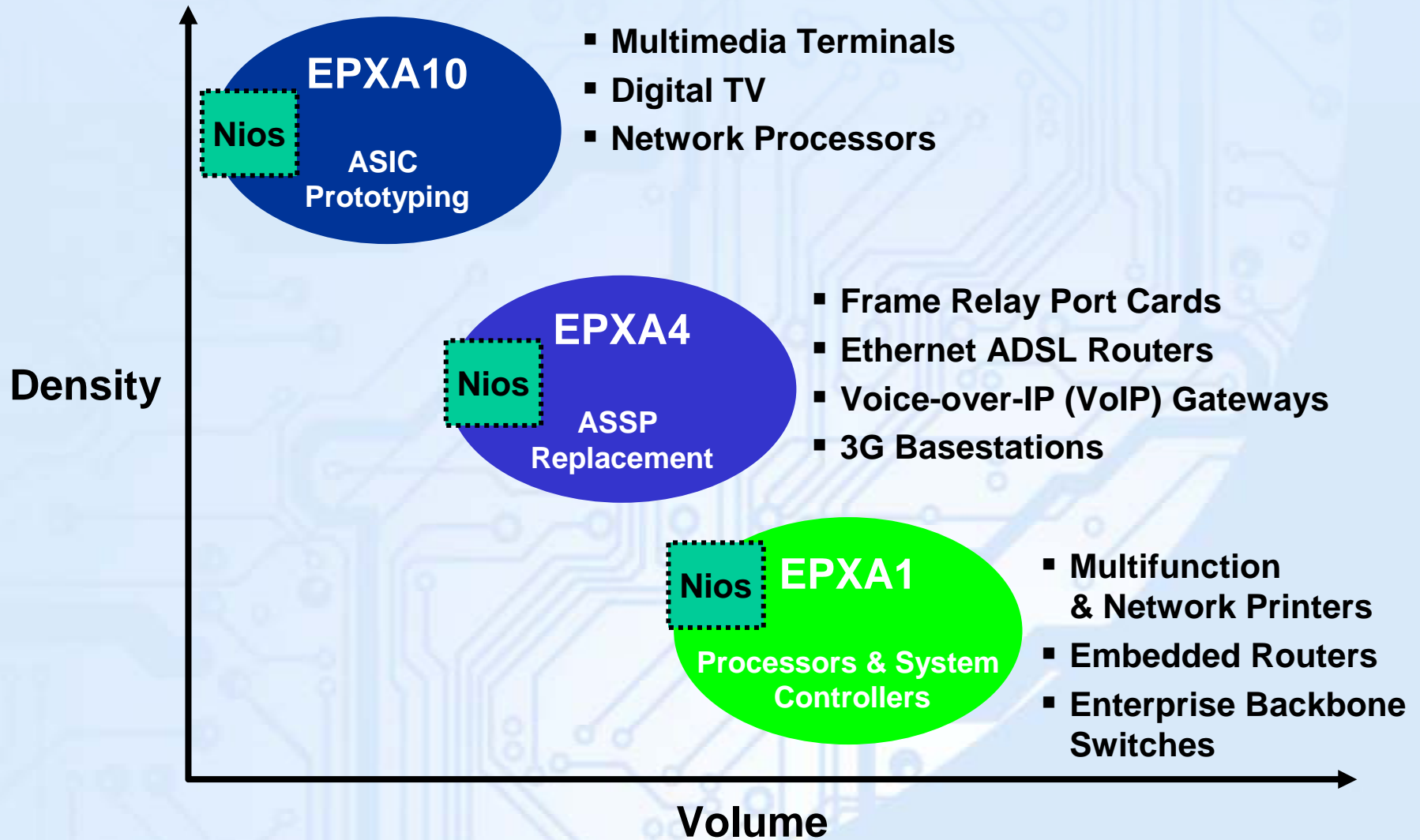- **4-5 Weeks Prototype Turnaround Time at TSMC, Low NRE**

System-On-a-Programmable-Chip Solutions

Excalibur ARM-based Devices Application Examples

Excalibur Family Market Fit

Density

Volume

EPXA10

Nios

ASIC Prototyping

- Multimedia Terminals
- Digital TV
- Network Processors

EPXA4

Nios

ASSP Replacement

- Frame Relay Port Cards
- Ethernet ADSL Routers
- Voice-over-IP (VoIP) Gateways
- 3G Basestations

EPXA1

Nios

Processors & System Controllers

- Multifunction & Network Printers
- Embedded Routers
- Enterprise Backbone Switches

Enterprise Backbone Switches

MAC: Media Access Control
PHY: Physical Layer
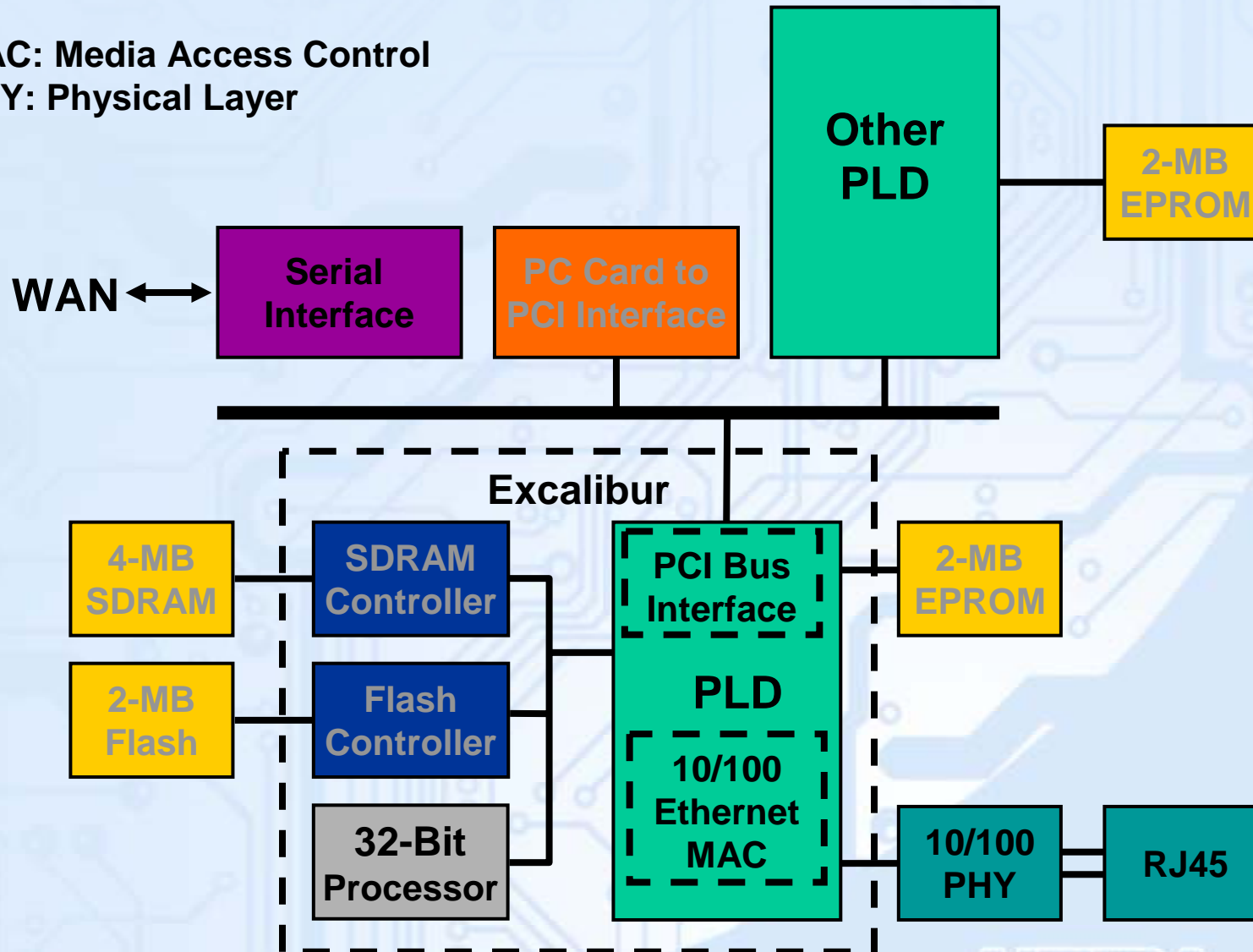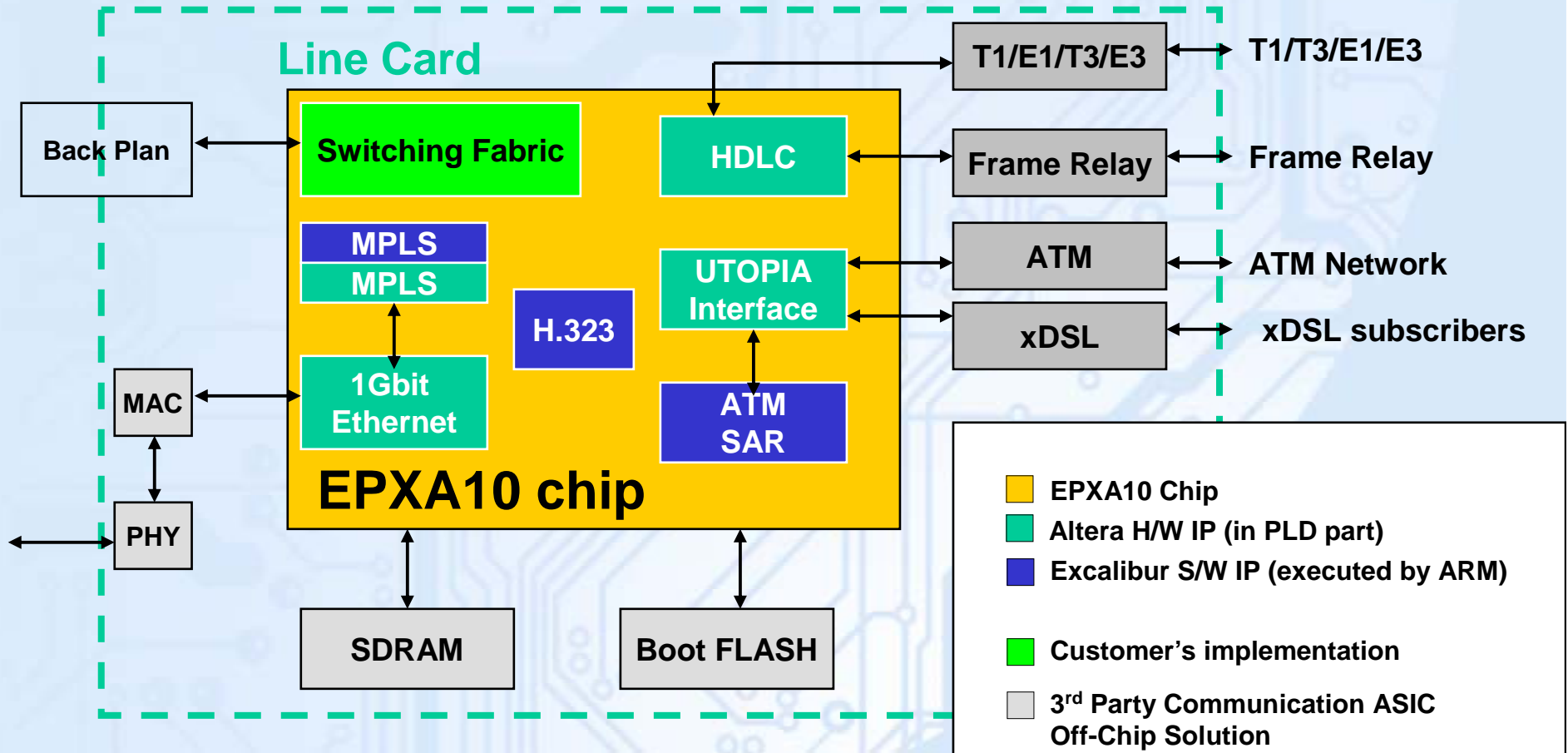
Excalibur ARM-based Device Summary

- *Complete* **Solution for SOPC**
  - **Hardware & Software Solution**
  - **Development Board, Drivers, IP**
  - **Built-In Licensing for ARM-based Devices**
- *Flexible* **Solution**
  - **Make Changes During Development**
  - **Make Changes in Production**
  - **Painless Route to Low-Cost HardCopy Solution**
- *Fast* **Solution**
  - **Performance**
  - **Time-to-Market**
  - **System Development**
    - **Quartus II/MegaWizard**

POP QUIZ

(60)

System-On-a-Programmable-Chip Solutions

Quiz Question

Which of the following statement is false?

A) Altera provides Excalibur MegaWizard to configure Excalibur embedded stripe.

B) Altera provides both bus-functional model & full-stripe model to verify ARM-based Excalibur devices

C) Both single-port and dual-port SRAM are part of the embedded stripe of ARM-based Excalibur devices.

D) Ethernet MAC and PCI interface are part of the the embedded stripe of ARM-based Excalibur devices.

Quiz Answer

Which of the following statement is false?

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C) Both single-port and dual-port SRAM are part of the embedded stripe of ARM-based Excalibur devices.

D) Ethernet MAC and PCI interface are part of the the embedded stripe of ARM-based Excalibur devices.