
System-On-a-Programmable-Chip Solutions
PLD World Korea 2001
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SoPC Solution

System-On-a-Programmable-Chip Solutions

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Agenda (10:00 – 10:45)

- APEX™ II
  - APEX™ II Device Family Overview
  - Device Features
  - Applications, etc
- Mercury
- Excalibur
- HardCopy
- MAX Devices
- Quartus® II
- IP
  - Open Core Plus
  - IP Roadmap
- SOPC Summary

SOPC Strategy

High-Density PLDs

Development Software

Intellectual Property

Design Services

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APEX II

- APEX™ II Device Family Overview
- Device Features
  - LVDS Details
  - Embedded System Blocks (ESBs)
  - External Memory Integration
  - Additional Features
- Applications
- Summary

APEX II: The Next Generation

- **High-Speed I/O Capabilities**
  - 1-Gbps True-LVDS™ Solution, LVPECL, PCML & HyperTransport
  - 624-Mbps, Flexible-LVDS™ Solution, LVPECL & HyperTransport
  - RapidIO, Utopia IV, Flexbus CSIX, POS-PHY Level 4
  - 250-MHz HSTL

- **Internal & External Memory Options**
  - 4-Kbit Memory Blocks with Bi-directional Read / Write Ports
  - External Interface Support for ZBT, DDR & QDR RAMs
- **Maximized Chip-to-Chip Performance**
  - Clock-Data Synchronization
  - 1-Gbps LVDS & LVPECL
  - Up to 124 High-Speed Channels

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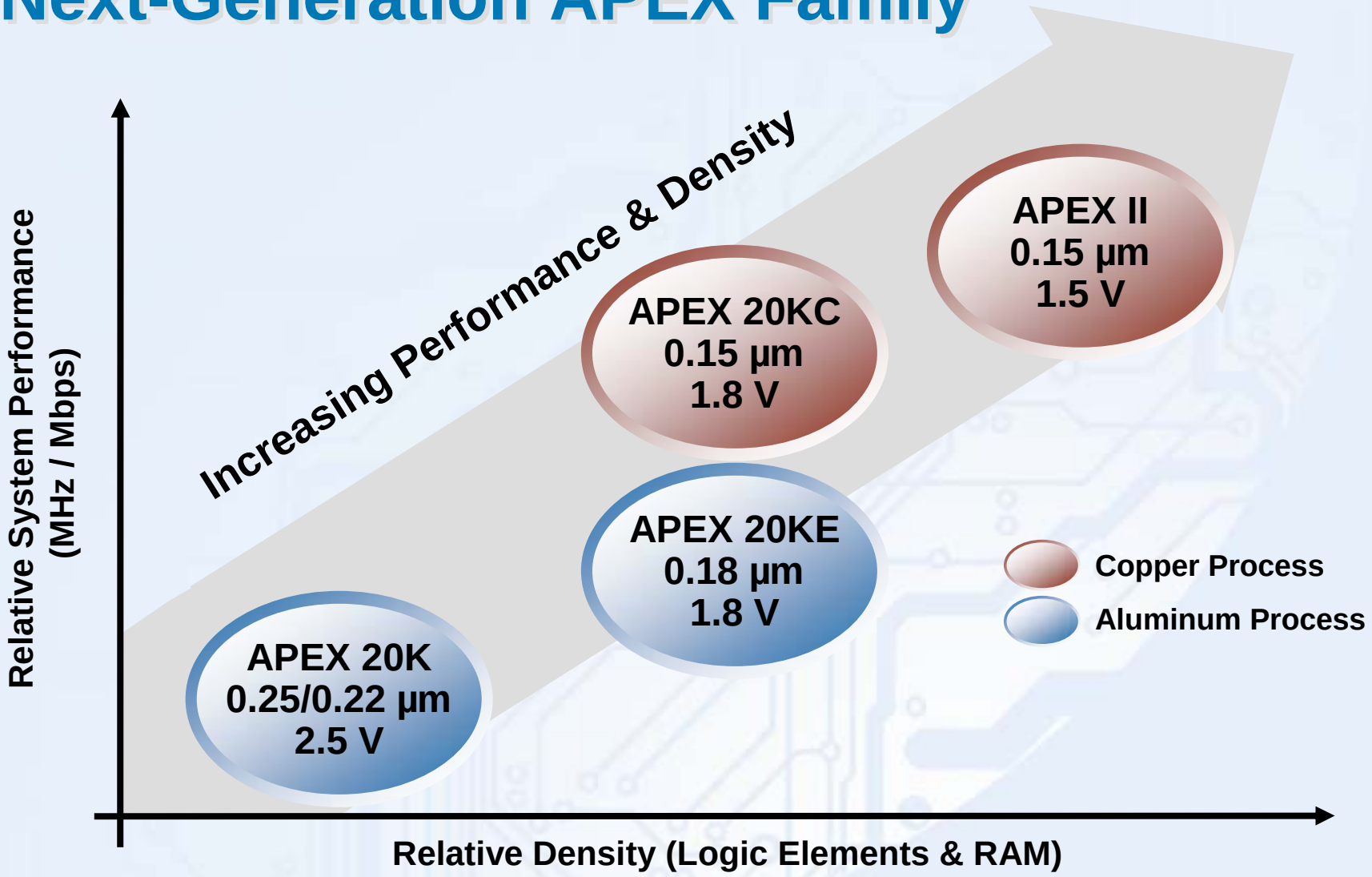
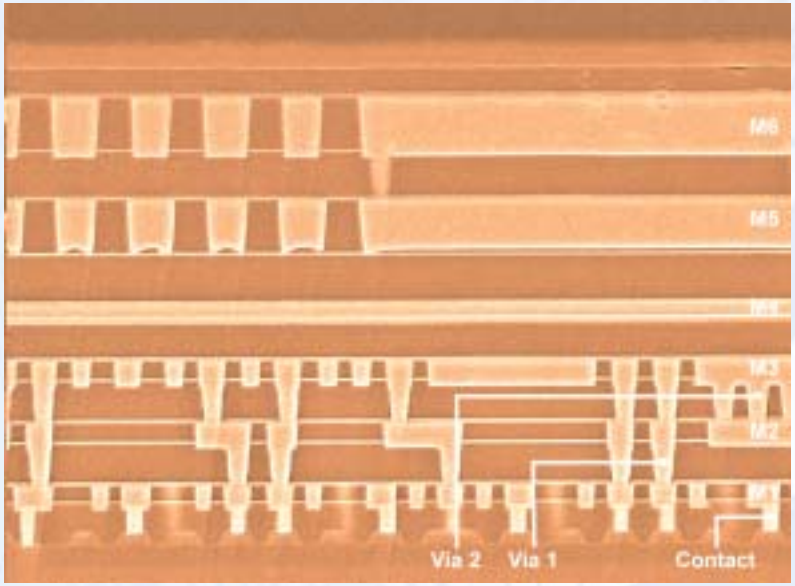
Next-Generation APEX Family



Partial Copper Vs. All-Layer Copper

- Partial Copper Layers
  - Copper Used on Top Layers Only
  - Top Layers Are Power Planes,
    Not Performance-Critical Interconnects
  - Provide No Significant Performance Benefits
- All-Layer Copper
  - Significant Performance Increase



Power Plane

Interconnects

APEX II Product Offerings

Device	EP2A15	EP2A25	EP2A40	EP2A70	EP2A90
Maximum Gates	1,900,000	2,750,000	3,000,000	5,250,000	7,000,000
Typical Gates	600,000	900,000	1,500,000	3,000,000	4,000,000
Logic Elements	16,640	24,320	38,400	67,200	89,280
Embedded System Blocks (ESBs)	104	152	160	280	372
RAM Bits	425,984	622,592	655,360	1,146,880	1,523,712
True-LVDS Channels* (Input/Output)	36 / 36	36 / 36	36 / 36	36 / 36	36 / 36
Flexible-LVDS Channels** (Input/Output)	56 / 56	56 / 56	88 / 88	88 / 88	88 / 88
Max. User I/O Pins	492	607	735	1,060	1,140

* True-LVDS Channels Also Support LVPECL, PCML & HyperTransport I/O
** Flexible-LVDS Channels Also Support LVPECL Inputs & HyperTransport I/O

APEX II LVDS Support

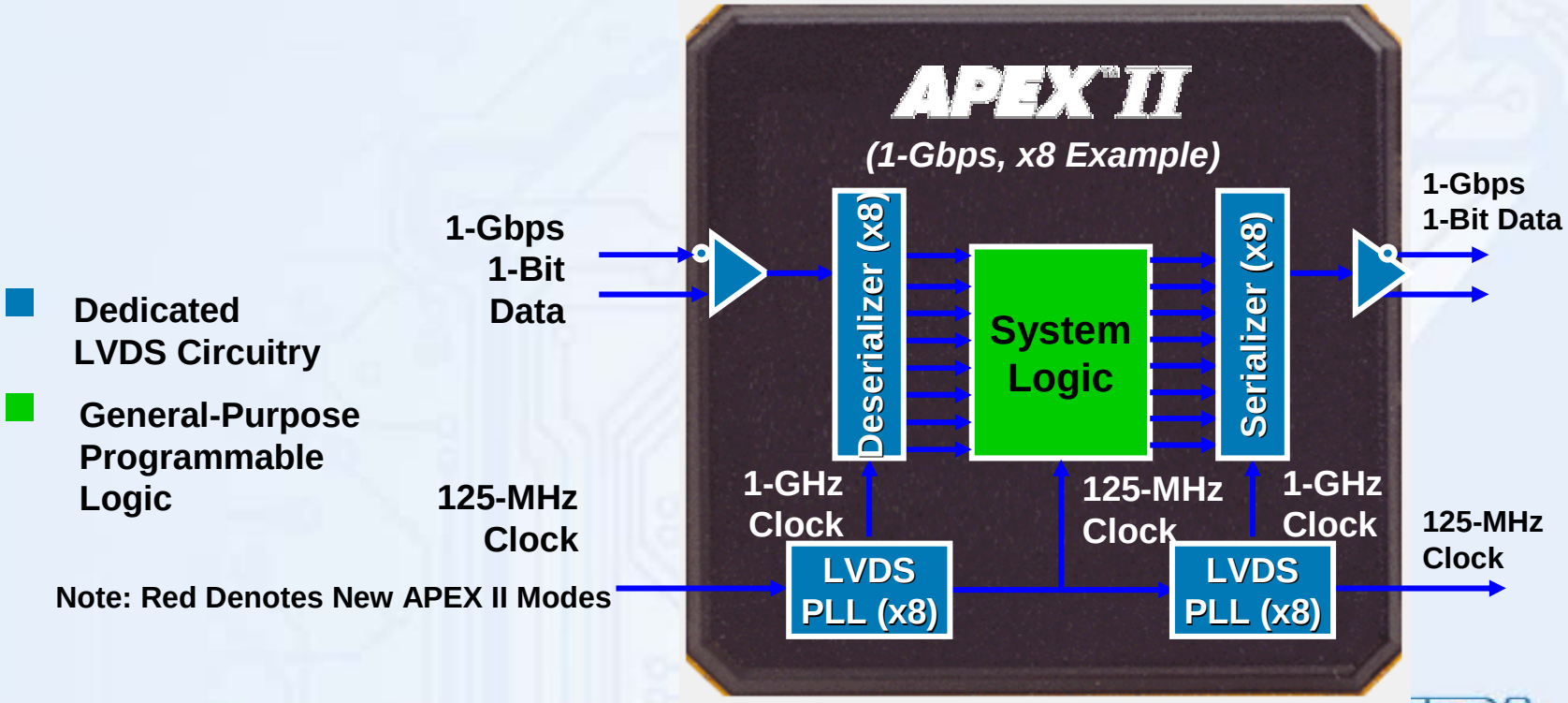
Device	True-LVDS Channels * (Input/Output) 1-Gbps per Channel	Flexible-LVDS Channels ** (Input/Output) 624-Mbps per Channel
EP2A15	36/36	56/56
EP2A25	36/36	56/56
EP2A40	36/36	88/88
EP2A70	36/36	88/88
EP2A90	36/36	88/88

*** True-LVDS Channels Also Support LVPECL, PCML & HyperTransport I/O**
**** Flexible-LVDS Channels Also Support LVPECL Inputs & HyperTransport I/O**

Total Differential Bandwidth
Up to 182 Gbps

APEX II True-LVDS Circuitry

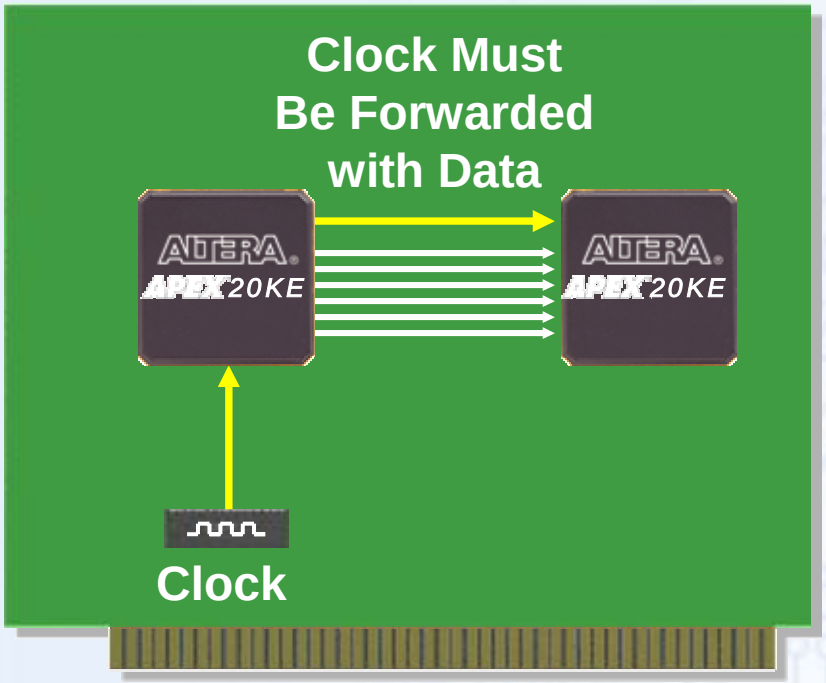
- Dedicated True-LVDS Circuitry Enables 1-Gbps Differential Signaling
- 36 Input & 36 Output Channels per Device
- LVDS, LVPECL, PCML & HyperTransport
- Features 2 Improved & Independent Clock Domains
- True-LVDS Supports 1x, 2x, 4x, 5x, 6x, 7x, 8x, 9x & 10x SERDES Modes



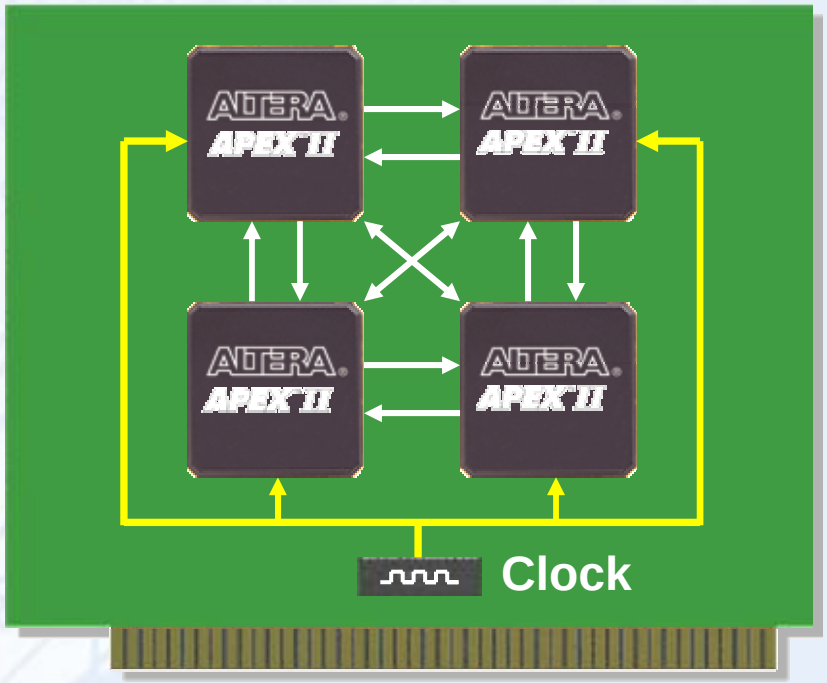
APEX II Clock-Data Synchronization

- CDS Circuitry Synchronizes True-LVDS Channels to System Clock
  - Performed Independently on All Channels

Source-Synchronous Transfer Limited to 2 Devices

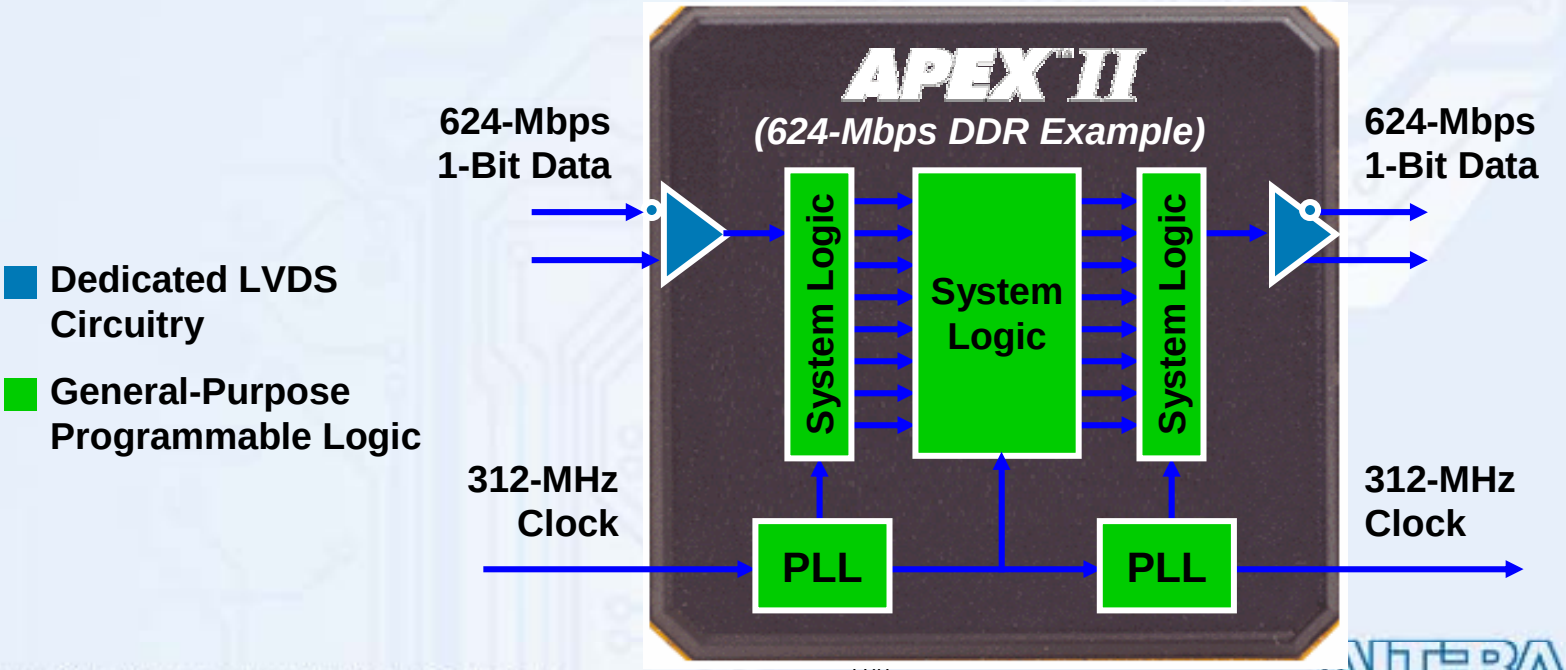


Chip-to-Chip Transfer with CDS Unlimited Chip-to-Chip Communication



APEX II Flexible-LVDS Circuitry

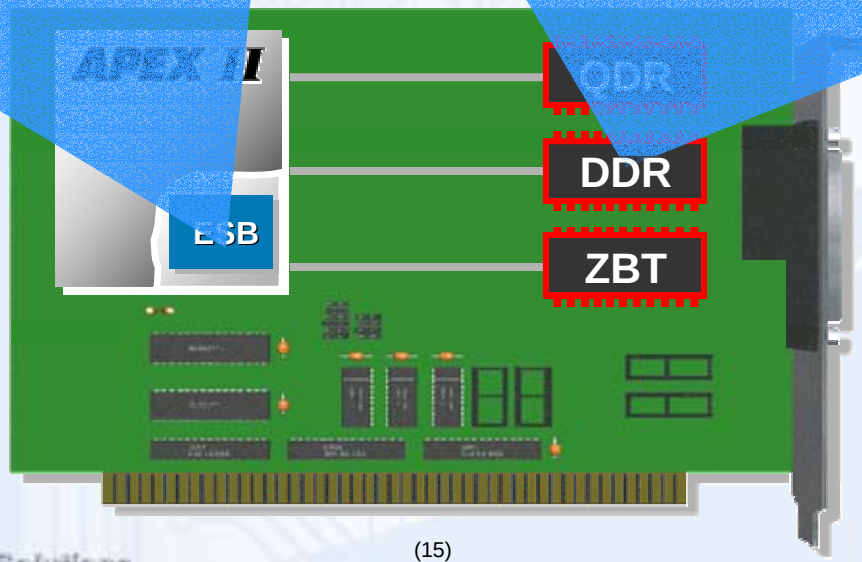
- Flexible-LVDS Circuitry Enables 624-Mbps Double Data Rate per Channel
  - LVDS, LVPECL & HyperTransport
- Up to 88 Input & 88 Output Channels per Device
- Dedicated Differential I/O Buffers
- General-Purpose Logic Used for SERDES & Clock Management
- Up to 12 Independent Clock Domains



Complete Memory Solution

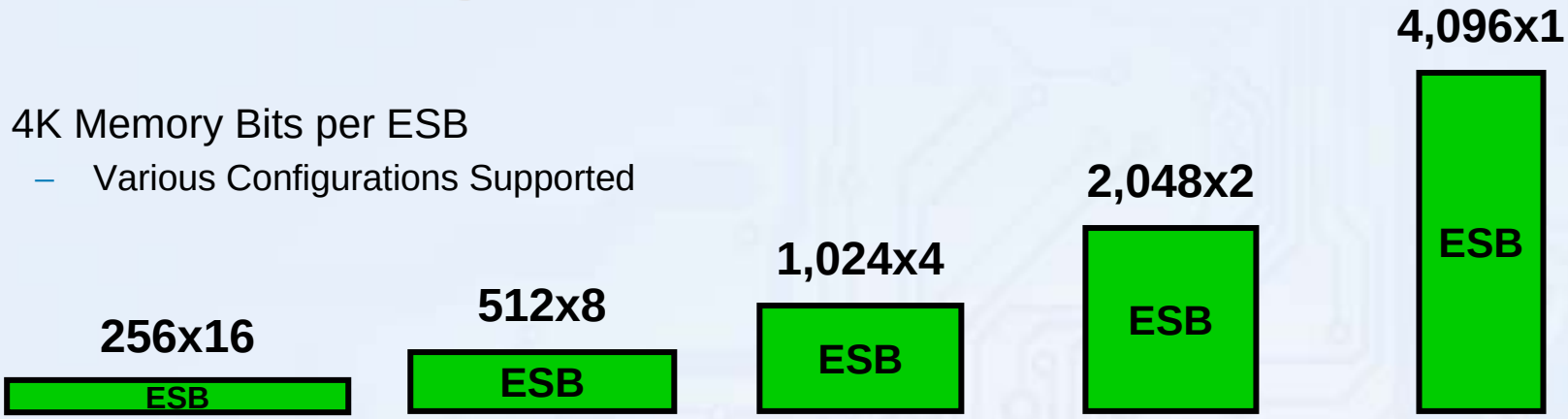
Internal RAM Blocks
4 Kbits per Block
Dual-Port+ Mode
Packing Mode
Mixed Port Widths

External Memory Interfacing	
Memory Type	**Performance**
ZBT SRAM	200 MHz
SDR SDRAMs	200 MHz
DDR SRAMs	334 Mbps
QDR SRAMs	668 Mbps
DDR SDRAMs	334 Mbps

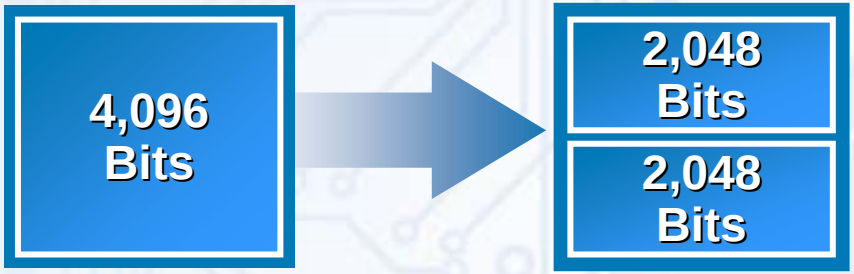


Embedded System Blocks

- 4K Memory Bits per ESB
  - Various Configurations Supported



- Single-Port, Packed Mode
  - ESBs Can Be Partitioned into Two Identical 2-Kbit Blocks



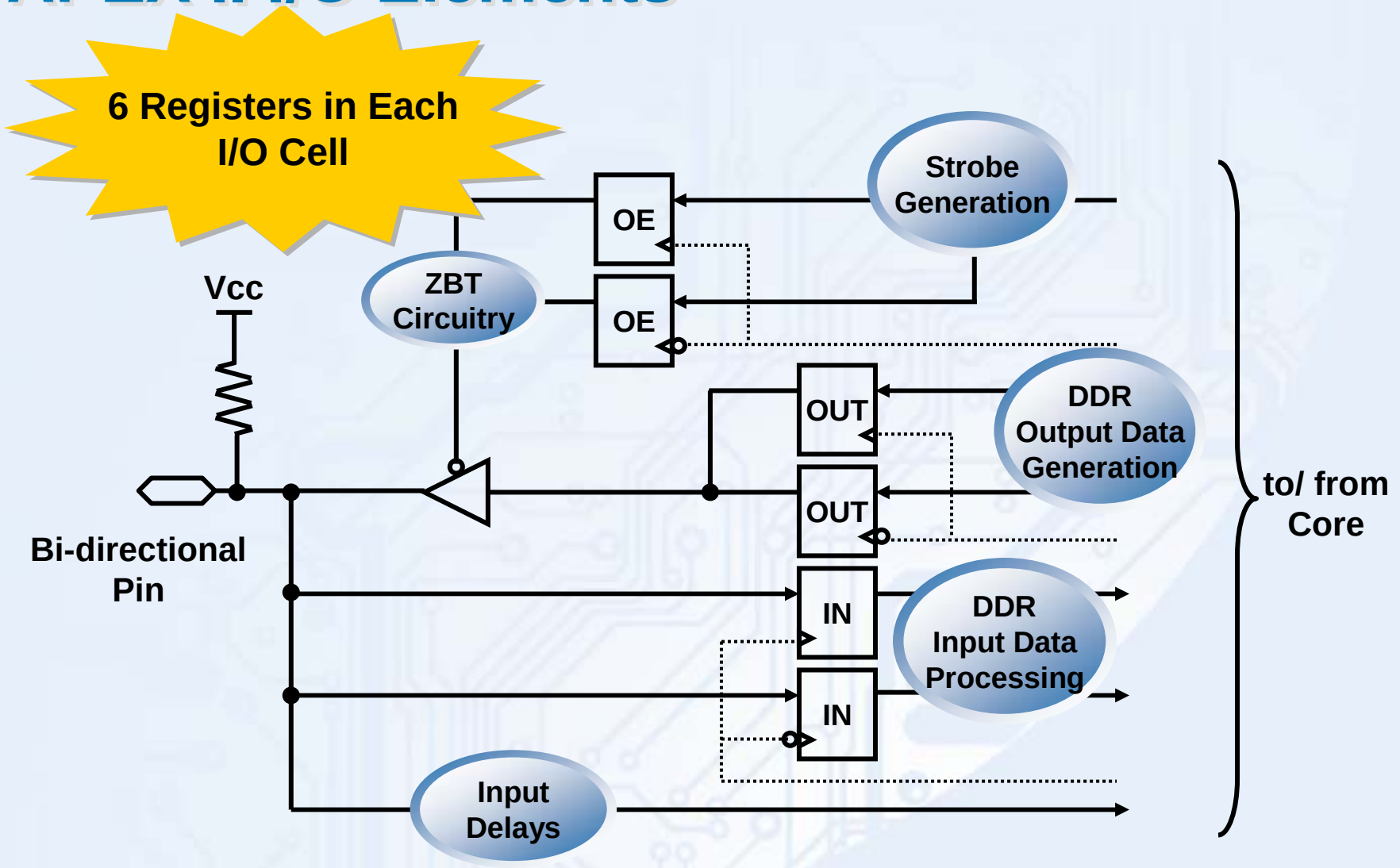
External Memory Integration

- Dedicated Support for Emerging High-Speed Memory Interfaces
  - Performance Targeted for Future Memory Devices

Memory Type	V_{CCIO}	I/O Standard	Performance
ZBT SRAM	3.3 V	LVTTL	200 MHz
SDR SDRAMs	3.3 V	LVTTL	200 MHz
DDR SRAMs	1.5 V	HSTL	334 Mbps
QDR SRAMs	1.5 V	HSTL	668 Mbps
DDR SDRAMs	2.5 V	SSTL-2 II*	334 Mbps

*** ClearOne Provides Resistor Packs for Transmission & Receiver Termination for DDR SDRAM Interface**

APEX II I/O Elements



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APEX II Features:

I/O Standards, PLLs,
Packaging, Configuration,
Redundancy

New I/O Standards

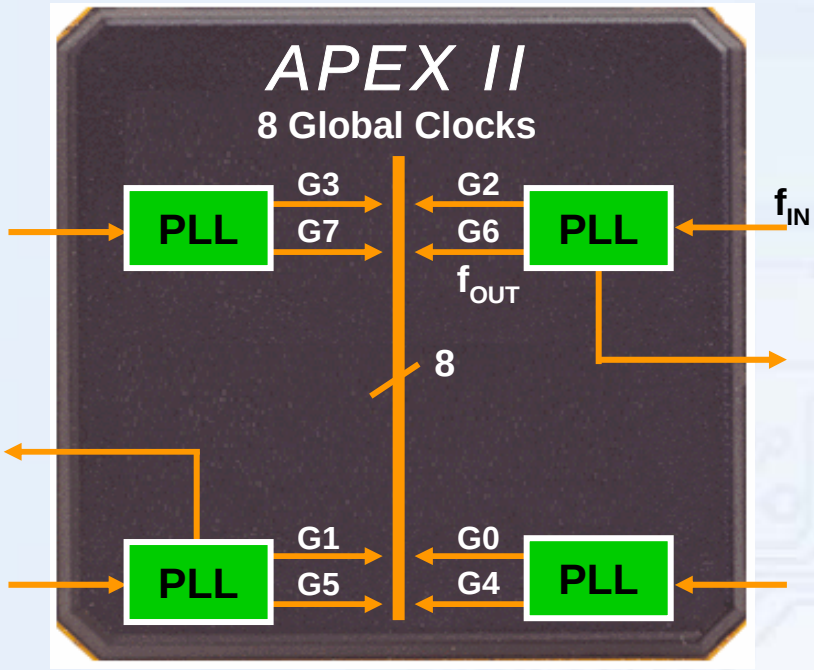
I/O Standard	Performance	Type
LVPECL	1 Gbps	Differential
PCML	1 Gbps	Differential
HyperTransport	1 Gbps	Differential
HSTL Class I, II	250 MHz	Single-Ended
SSTL-2 Class I, II	167 MHz	Single-Ended
SSTL-3 Class I, II	167 MHz	Single-Ended
PCI-X	133 MHz	Single-Ended

APEX II Additional I/O Capabilities

- Programmable Output Drive
  - 3.3-V LVTTL
    - 4-mA,12-mA, 24-mA, PCI or PCI-X
- Programmable Bus Hold
  - Eliminates Pull-up/Pull-down Resistors
  - Eliminates Noise-Induced Switching
- MultiVolt I/O Operation
  - Simplifies Integration with Mixed-Voltage Systems

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.5	1.8	2.5	3.3	1.5	1.8	2.5	3.3
3.3	✓	✓	✓	✓				✓
2.5	✓	✓	✓	✓			✓	
1.8	✓	✓	✓	✓		✓		
1.5	✓	✓	✓	✓	✓			

APEX II General-Purpose PLLs

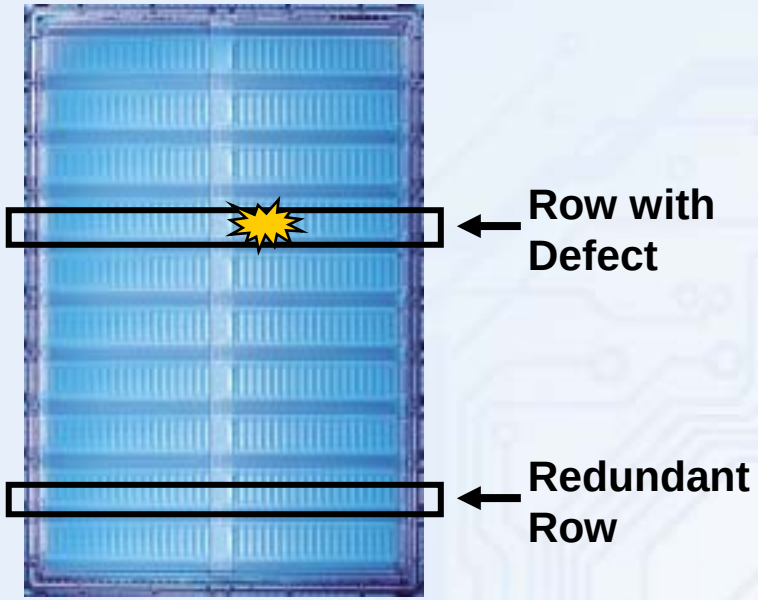


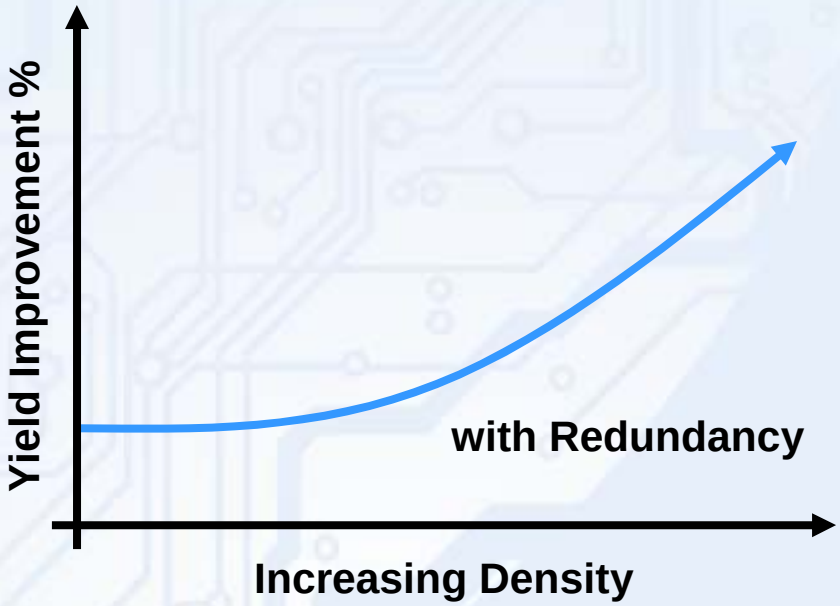
*APEX II Devices Include Four Additional LVDS PLLs

Feature	APEX II Support
PLLs*	4
PLL Outputs	2 per PLL (8 per Device)
Global Clocks	8 (1 per PLL Output)
External Outputs	2 in All Densities
Frequency Range	Input: 1.5 MHz to 420 MHz Output: 1.5 MHz to 420 MHz
ClockBoost™ Circuitry	$f_{OUT} = (m/(n*k))f_{IN}$ m,k: 1 to 160 n: 1 to 16
ClockShift™ Circuitry	Coarse: 90, 180, 270 Fine: 0.5-ns Resolution
Input Jitter Tolerance	50 ps or 2% Input Period

Yield Improvement in APEX II Devices

- Redundancy Increases Wafer Yield
  - All APEX II Devices Incorporate Redundancy





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Mercury™

The Programmable ASSP

Mercury

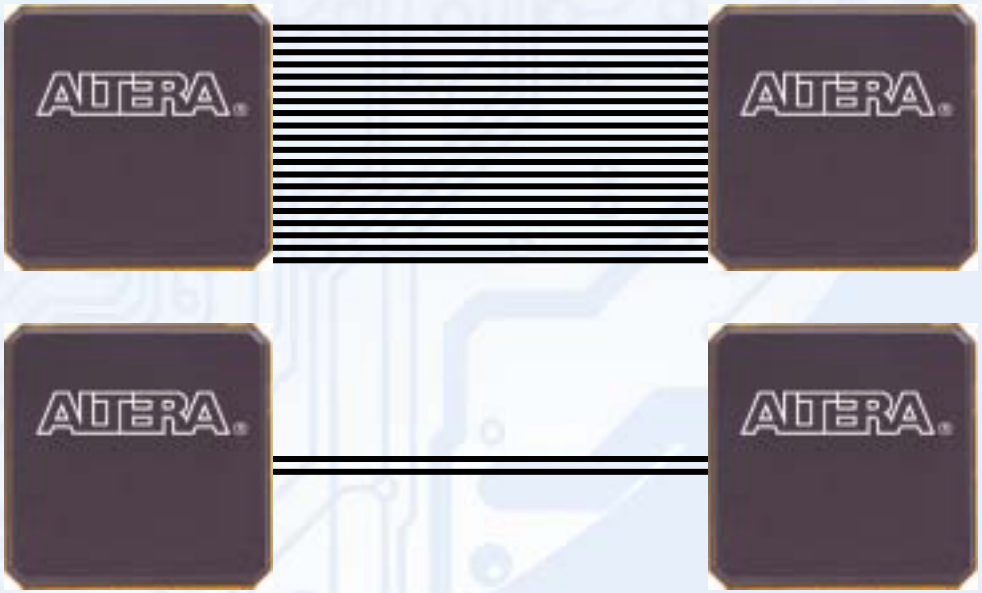
- The Programmable Application-Specific Standard Product (ASSP)
- Mercury™ Devices Family Overview
- Mercury I/O Features
- Mercury Core Features

Serial Transmission Advantages

- Higher Performance
- Lower Power
- Increased Noise Immunity
- Reduced Board Space

LVTTL
20 pins @ 42 MHz

LVDS
2 pins @ 840 Mbps



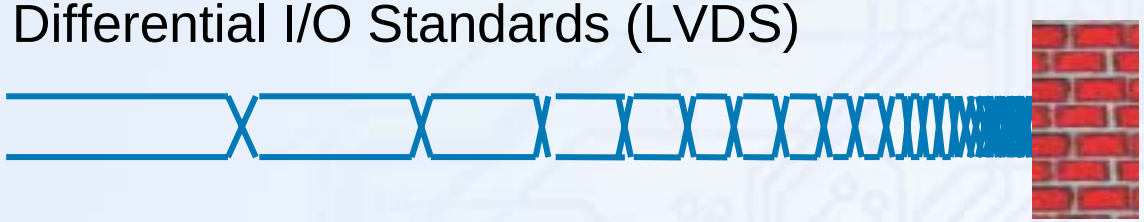
CDR: The I/O Performance Solution

Single-Ended I/O Standards

Single-Ended Standards Hit Noise Limitations at ~250 MHz

100 MHz **250 MHz**

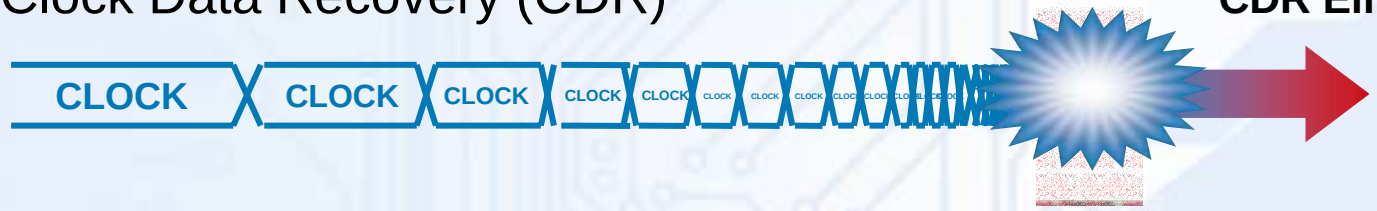
Differential I/O Standards (LVDS)



Clock Skew Overwhelms Differential I/O Standards at ~ 1 Gbps

100 Mbps **250 Mbps** **500 Mbps** **750 Mbps** **1 Gbps**

Clock Data Recovery (CDR)



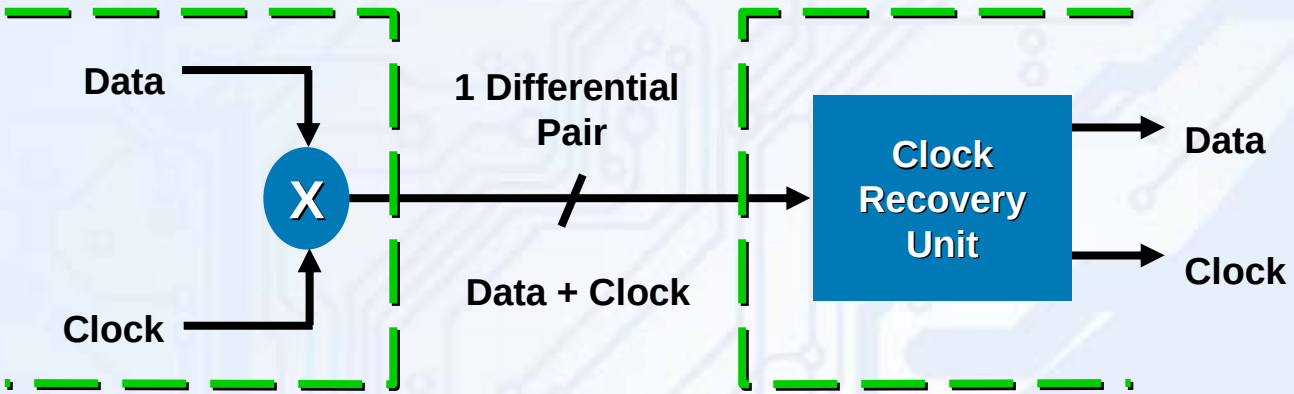
CDR Eliminates Barriers

1.25 Gbps & Beyond

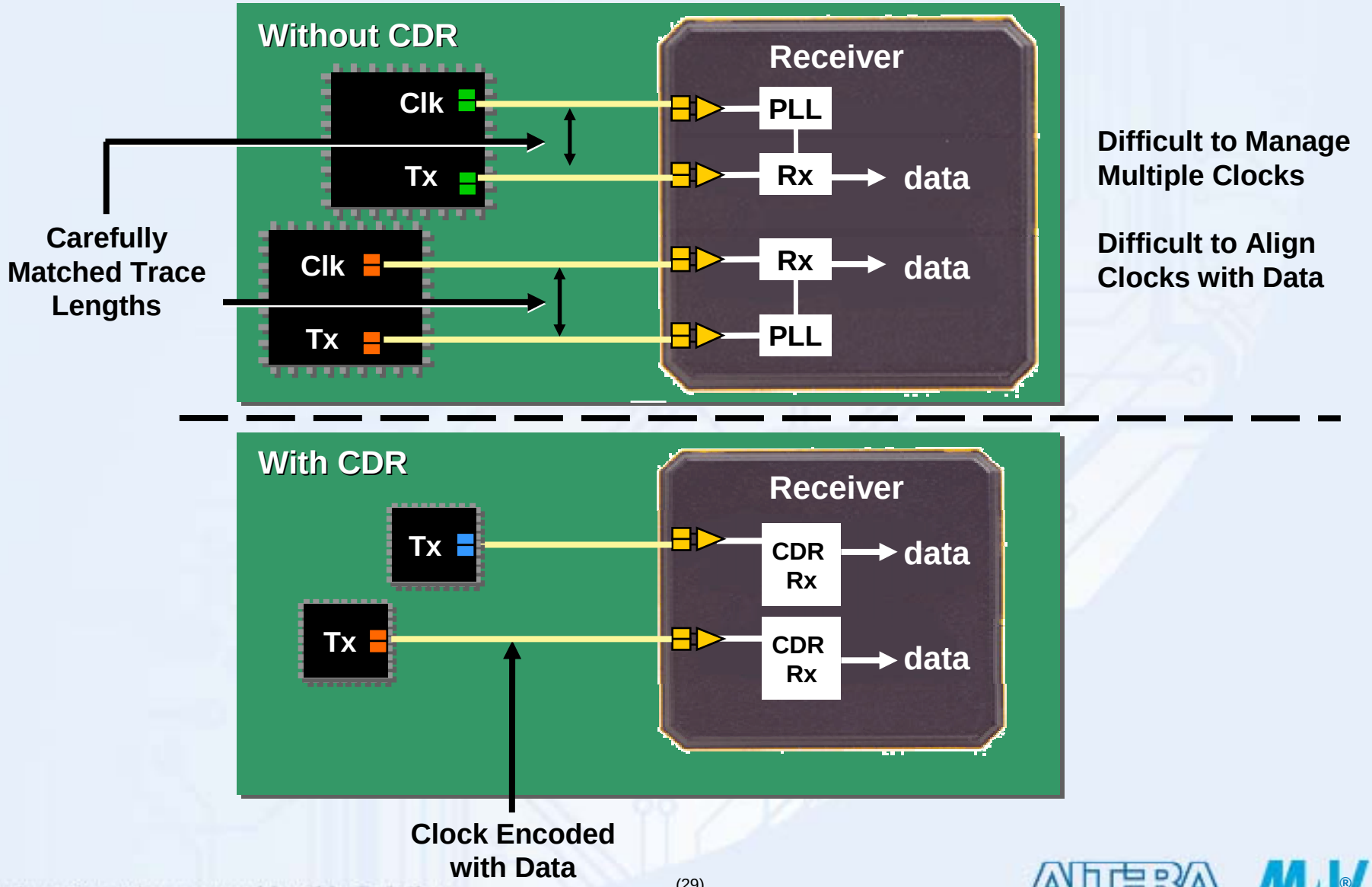
100 Mbps **250 Mbps** **500 Mbps** **750 Mbps** **1 Gbps**

Clock Data Recovery (CDR)

- Differential Signaling Allows High Clock Speeds
- CDR Takes It To The Next Level
  - Higher Speeds
  - Fewer Signals
  - Better Noise Immunity
  - Better Reliability
  - Lower Power

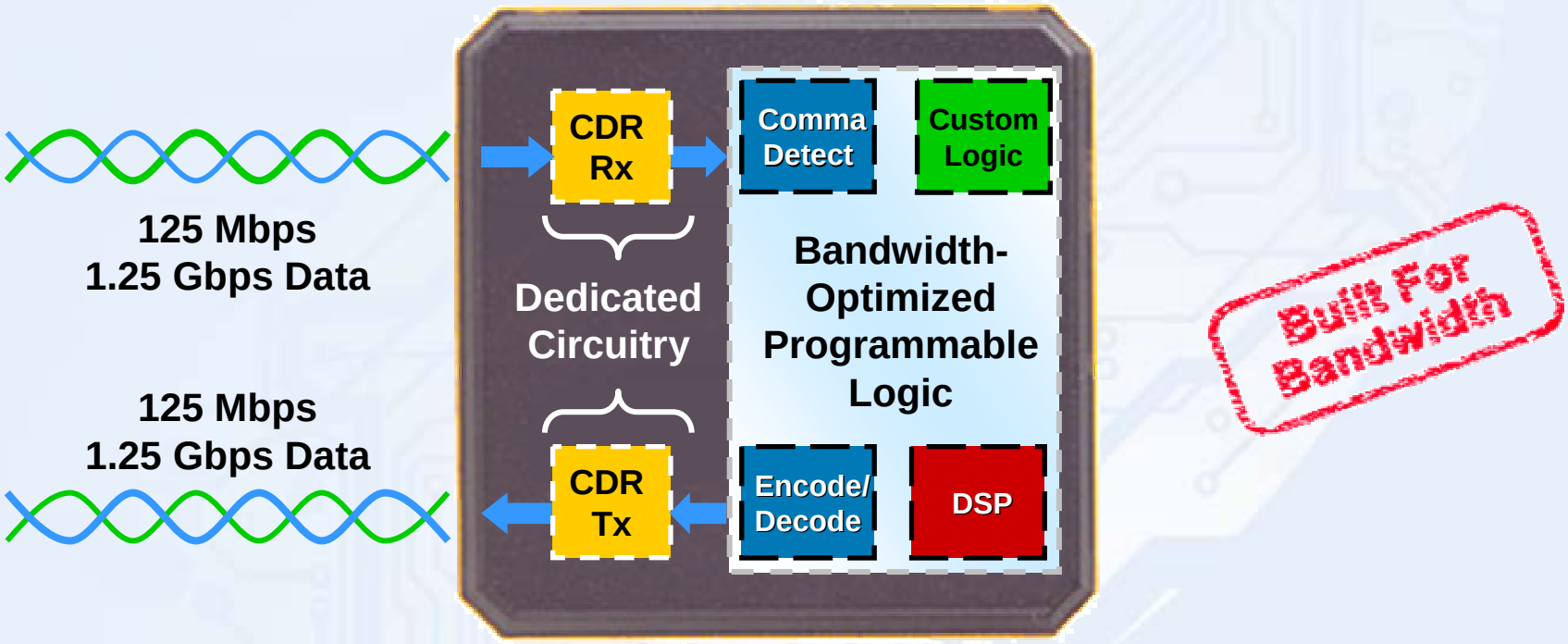


Additional CDR Benefits



The Mercury Solution

= 1.25 Gbit CDR + PLD



The Programmable ASSP

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Mercury Devices Overview

Start with CDR Channels….

Add the Optimized PLD Capability

Family Overview

- Architected From the Ground Up For High Bandwidth Functions
  - High-Speed CDR
  - New Core Architecture
  - Additional I/O Features

Device	CDR Channels	LEs	RAM Bits
EP1M120	8	4,800	48K
EP1M350	18	14,400	112K

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Mercury Features:

(I/O Standards, PLLs, Packaging, ESBs & External Memory Integration)

Advanced I/O Capabilities

Up to 18 Channels of
1.25-Gbps True-CDR

Flexible-LVDS™ Circuitry
on All Pins

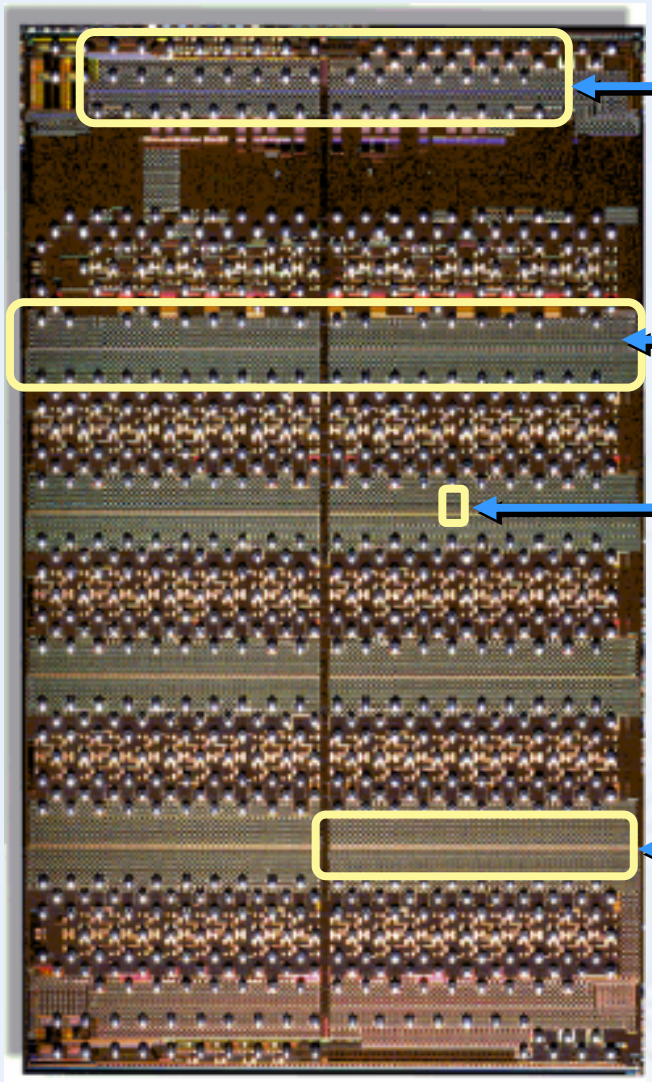
200 MHz ZBT SRAM &
332 Mbps DDR SDRAM Interfaces

HSTL, PCI-X & Other I/O Standards

High-Performance
Flip-Chip Packaging

Up to 12 PLL-Generated Clocks
Enhanced Clock Structures

Feature-Rich Architecture



Larger, Quad-Port Memory Blocks

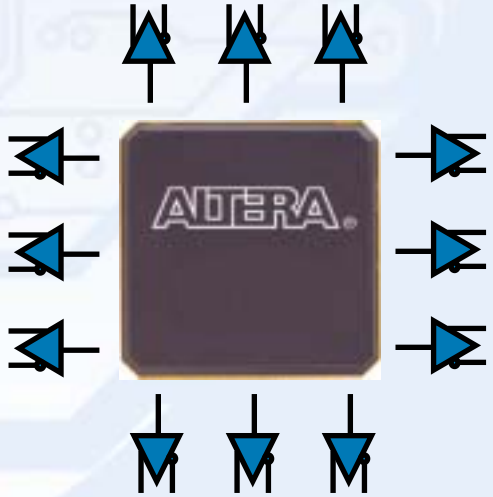
High-Performance Architecture

- Prioritized Routing Structure
- Wider Buses
- Improved Local Routing
- Enhanced Logic Elements (LEs)
- Enhanced Carry Chains

Distributed Multiplier Capability

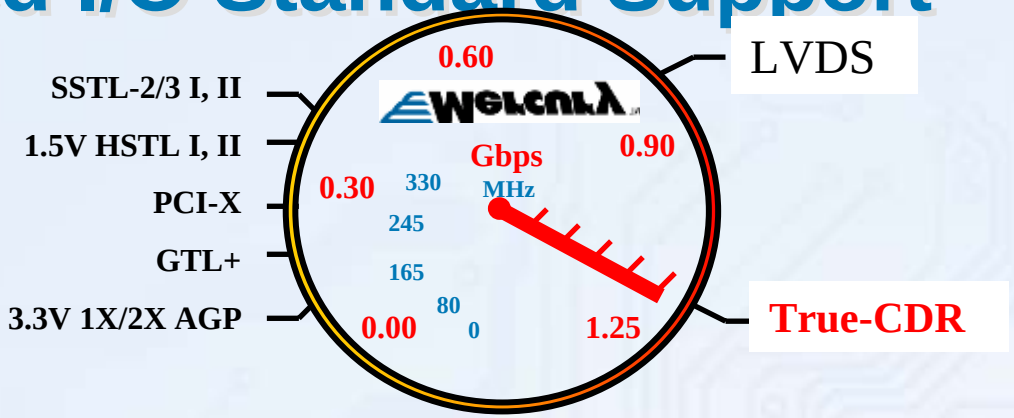
Mercury Flexible-LVDS™

- Additional Support for Differential Standards
- LVDS Available on Every Pin
  - Over 100 Channels on EP1M350
- LVDS Buffers Built into I/O Cell
  - No External Components Needed
- Data Rates of up to 432 Mbps



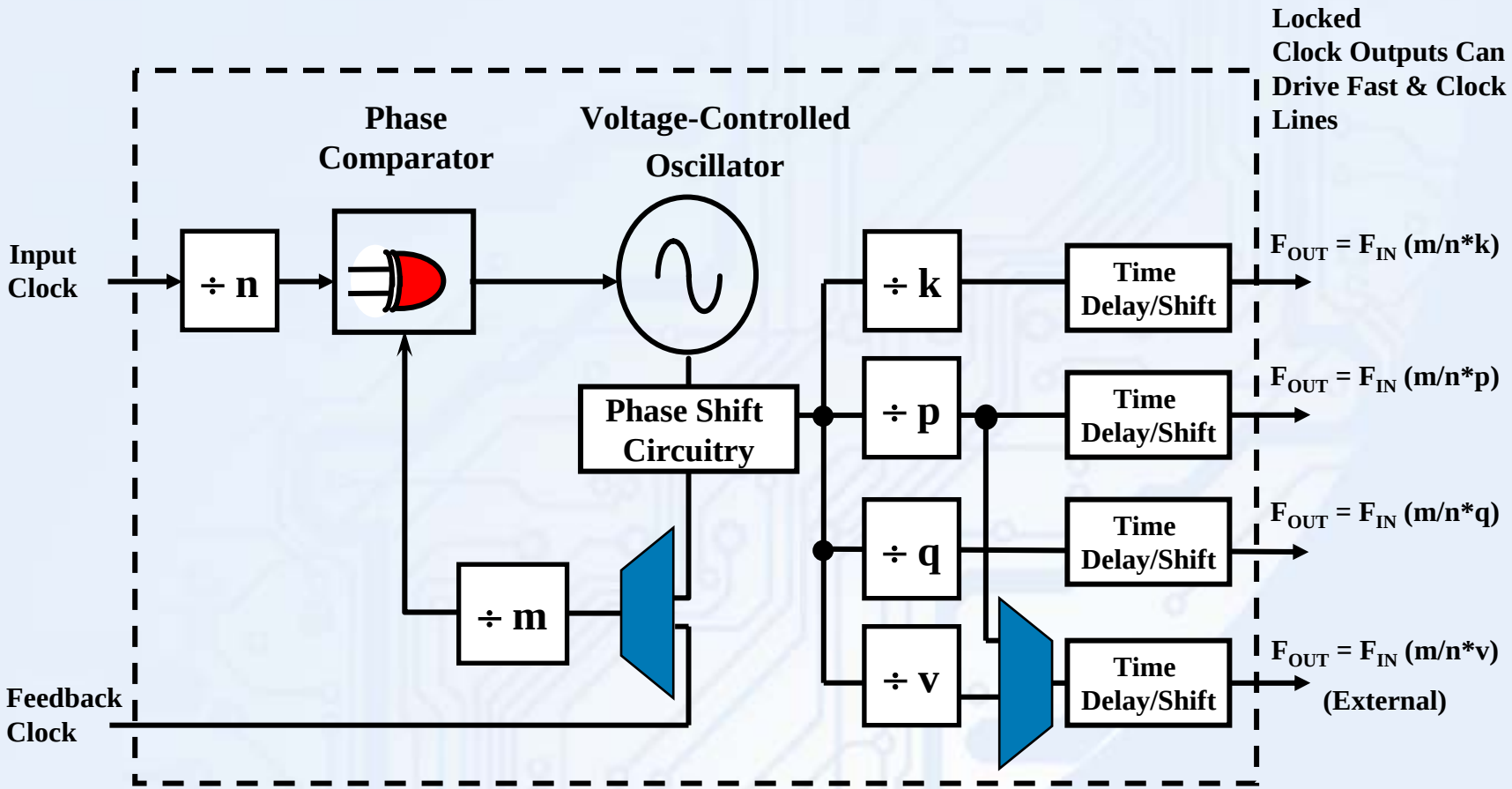
Note: Available on EP1M350 Only

Advanced I/O Standard Support



I/O Standard	Applications	Approximate Speed
LVDS + CDR	Line Side & Backplane	1.25 Gbps
LVPECL + CDR	Clock Distribution	1.25 Gbps
PCML + CDR	High Speed	1.25 Gbps
LVDS	Backplane & Point to Point	840 Mbps
1.5-V HSTL I, II	Cache RAMs/ Fast SRAMs	125 - 250 MHz
SSTL-3 I, II	SDRAMs	80 - 166 MHz
SSTL-2 I, II	DDR SDRAMs	160 - 332 Mbps
GTL+	Backplane Driver	200 MHz
3.3-V 1x/2x AGP	Graphic Processors	66 MHz
CTT	JEDEC Standard	N/A
3.3-V PCI	PC, Embedded	64 bit / 66 MHz
3.3-V PCI-X	PC, Embedded	64 bit / 133 MHz
3.3-,2.5,1.8-V LVTTL	General purpose	250 MHz

Mercury PLL


Locked
Clock Outputs Can
Drive Fast & Clock
Lines
Phase
Comparator
Voltage-Controlled
Oscillator
Input
Clock
÷ n
÷ k
Time
Delay/Shift
F_OUT = F_IN (m/n*k)
Phase Shift
Circuitry
÷ p
Time
Delay/Shift
F_OUT = F_IN (m/n*p)
÷ q
Time
Delay/Shift
F_OUT = F_IN (m/n*q)
÷ m
÷ v
Time
Delay/Shift
F_OUT = F_IN (m/n*v)
(External)
Feedback
Clock

Additional I/O Features

- Three I/O Element Registers
  - Fast Setup & Clock-to-out Times
- Bus Hold
- Programmable Pull-Up Resistor
- Programmable Input Delay
  - Fine-Grained Setup & Hold Time Window Adjustment
- Open Drain Output Option
- Programmable Drive Strength
    - 2 mA, 4 mA, 8 mA, 12 mA, 16 mA, 24 mA, PCI, PCI-X
- Programmable Slew Rate

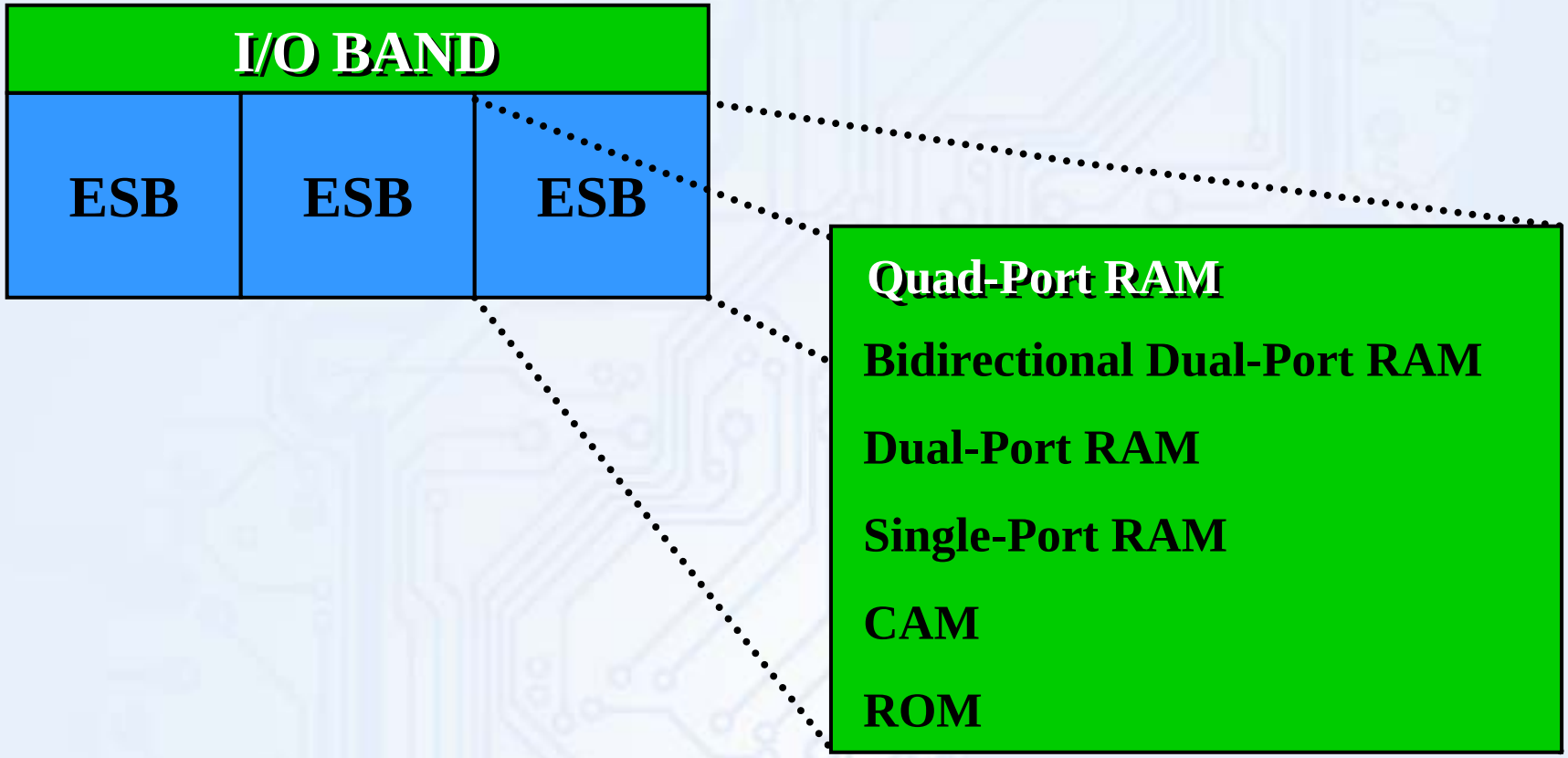
External Memory Support

- Dedicated Support for Emerging High-Speed Memory Standards
  - Performance Targeted for Future Devices

Memory Type	V_{CCIO}	Specifications (I/O Standards)	Performance
ZBT SRAMs	3.3 V / 2.5 V	LVTTL	200 MHz
QDR SRAMs	1.5 V	HSTL	664 Mbps
DDR SRAMs	1.5 V	HSTL	332 Mbps
DDR SDRAMs	2.5 V	SSTL-2 (I/II)	332 Mbps
SDR SDRAMs	3.3 V	SSTL-3 (II)	166 MHz
Synchronous SRAMs	3.3 V / 2.5 V	LVTTL	166 MHz

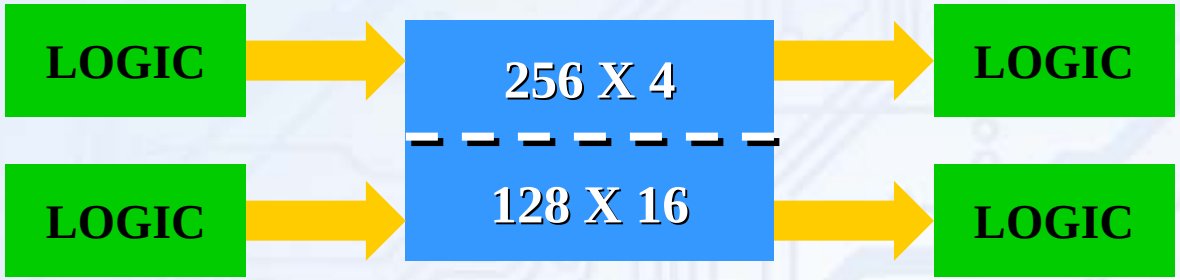
Embedded System Block (ESB)

- Enhanced ESB Structure



ESB Partitioning

- Partition Single ESB into Two Blocks
  - Increase Total Number of Memory Blocks per Device



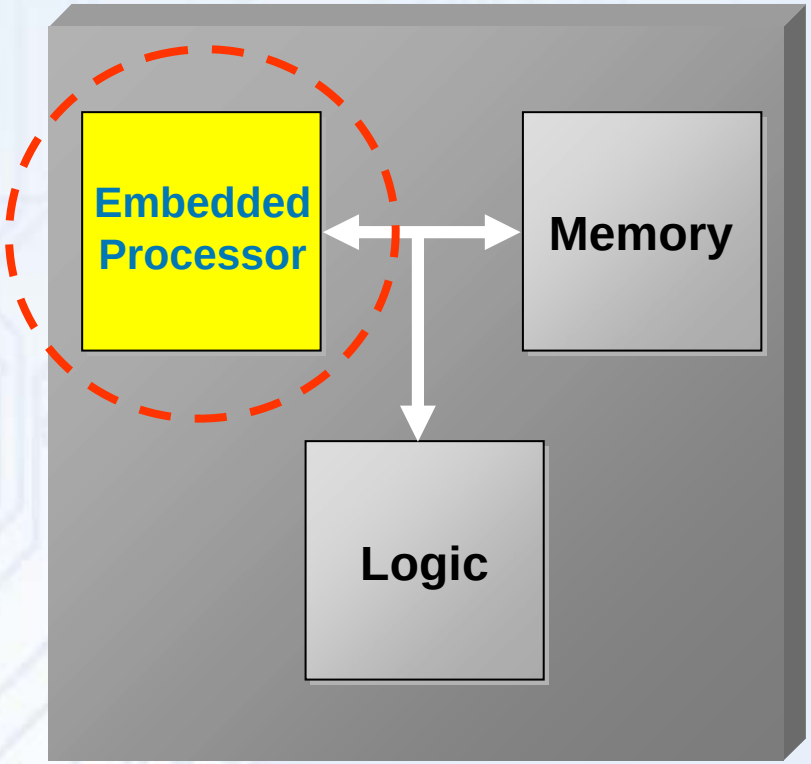
Embedded Processor Solutions

EXCALIBUR™

Integrating Embedded Processors for Complete SOPC Solution

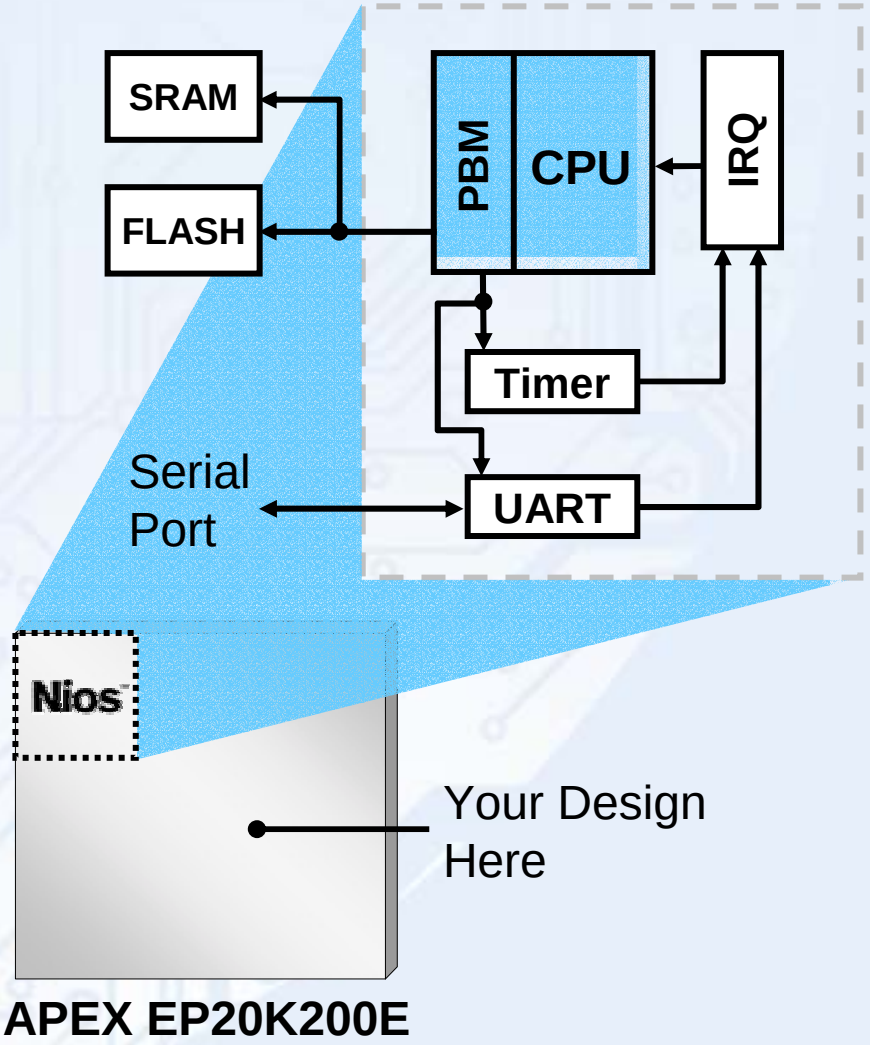
Excalibur Embedded Processor Solutions

- Provide Programmable Flexibility of PLDs
- Provide Horsepower of MPUs
- Provide Fast Time-to-Market in an SOPC Solution



Nios Embedded Processor Core

- Configurable Soft Core
- 16-/32-Bit Datapath
- 50-MIPS Performance
- 16-Bit Instruction Set
- RISC-Based, Five-Stage Pipeline
- One Instruction Per Clock
- Scalability Supports Parallel Processing in Single Chip
- Consumes 25K Gates
  - 12% of APEX EP20K200E
  - 2% of APEX EP20K1500E

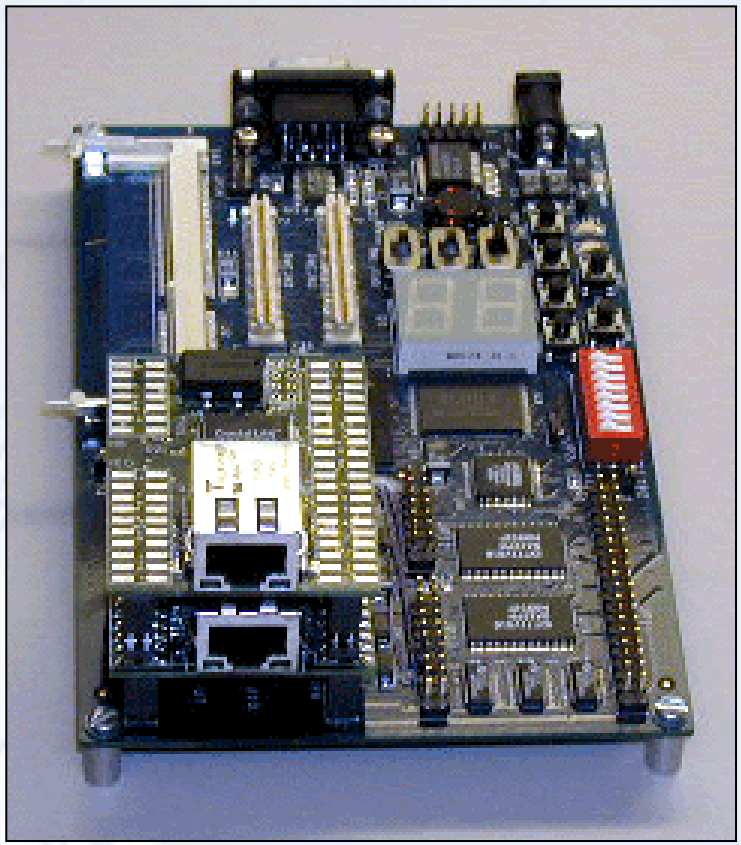


Nios Complete Development Kit

- Altera® Nios RISC Processor
- Development Tools
  - Quartus™ II Software
  - Cygnus GNUPro
- Peripherals
- Reference Design
- Development Board & Download Cable

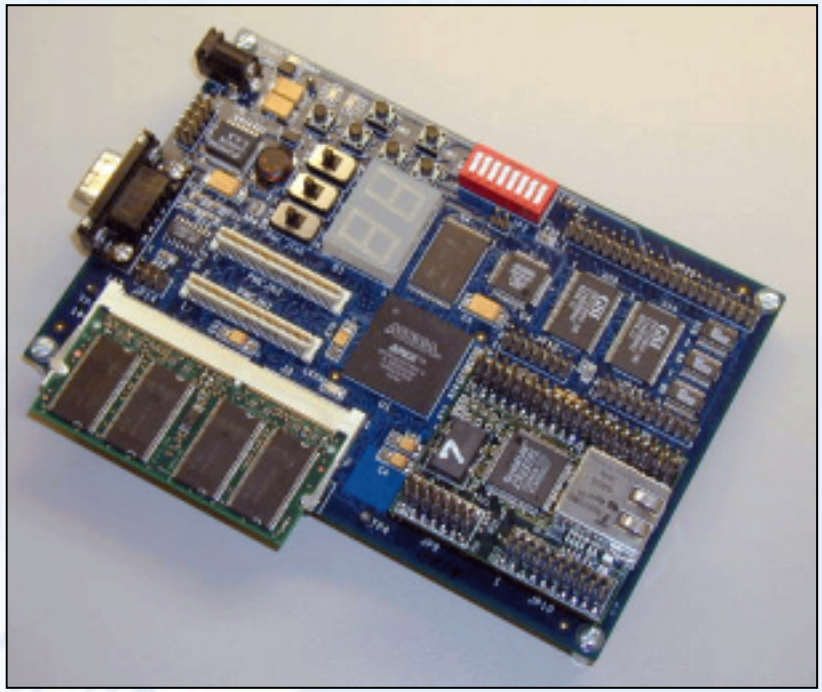
Nios Ethernet Appliance Kit

- Supports a Wide Range of Applications
  - Factory Floor Automation
  - Basic Ethernet Connectivity
  - Internet Upgradable Hardware
- Supports All PLD Families
- Development Board
  - External 10Mb MAC/Phy
  - Support for 2 Ports
- Software
  - TCP/IP Stack
- Reference Design
  - Quartus Project
  - Web Server Application
- Price US$500



Nios Linux Development Kit

- Open-Source uCLinux OS
- Development Kit Contents:
  - uCLinux Source Code
  - Host Daughter Board
  - SDRAM / Flash Module
  - Nios Internet Appliance Kit
  - Reference Design
    - Quartus Project
    - Web Server
- Price US$2500

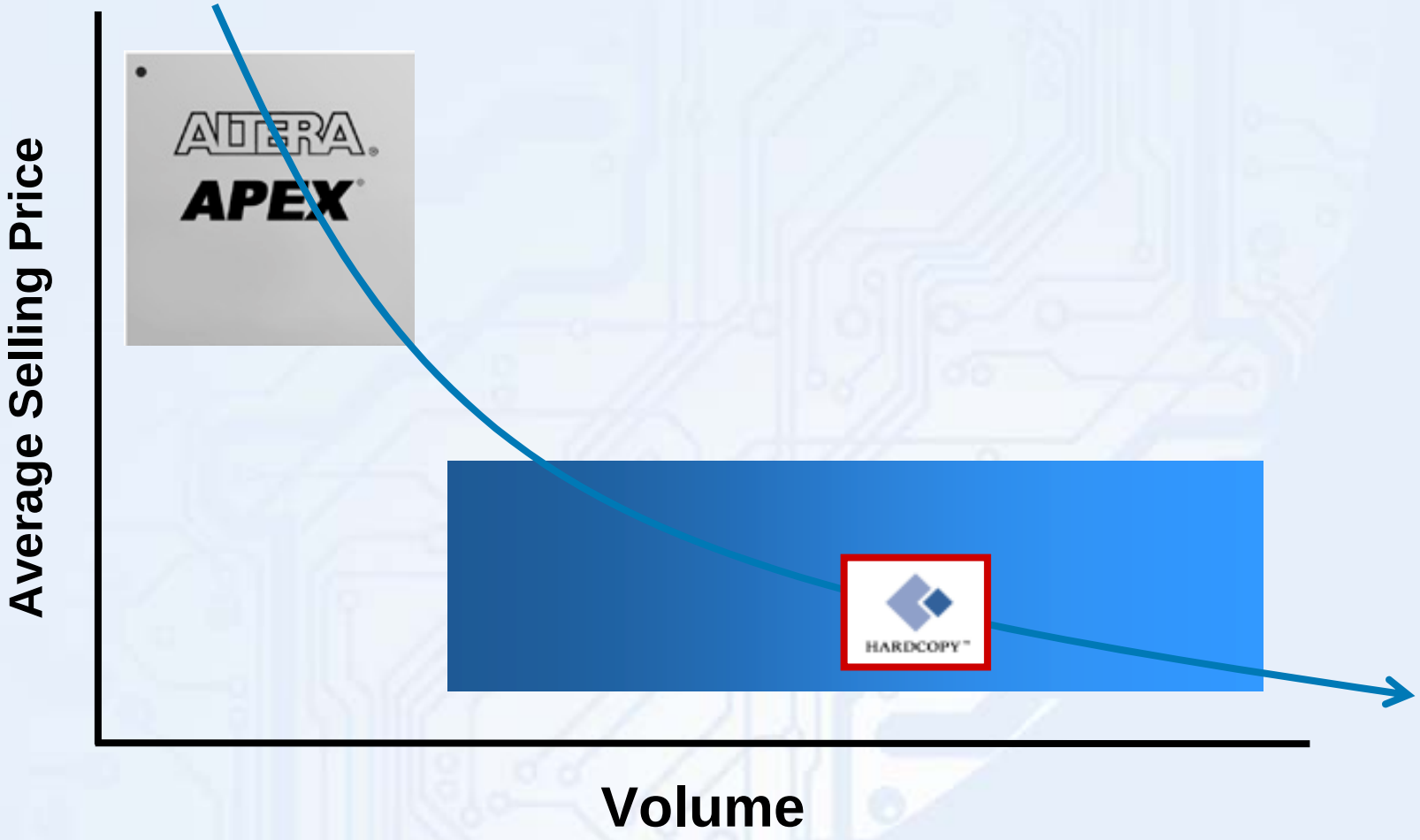


Details of the Excalibur ARM Products will be provided in the next conference session

ALTERA®

HARDCOPY™

HardCopy + PLD = Maximum Flexibility



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HardCopy
(New MPLD Program)

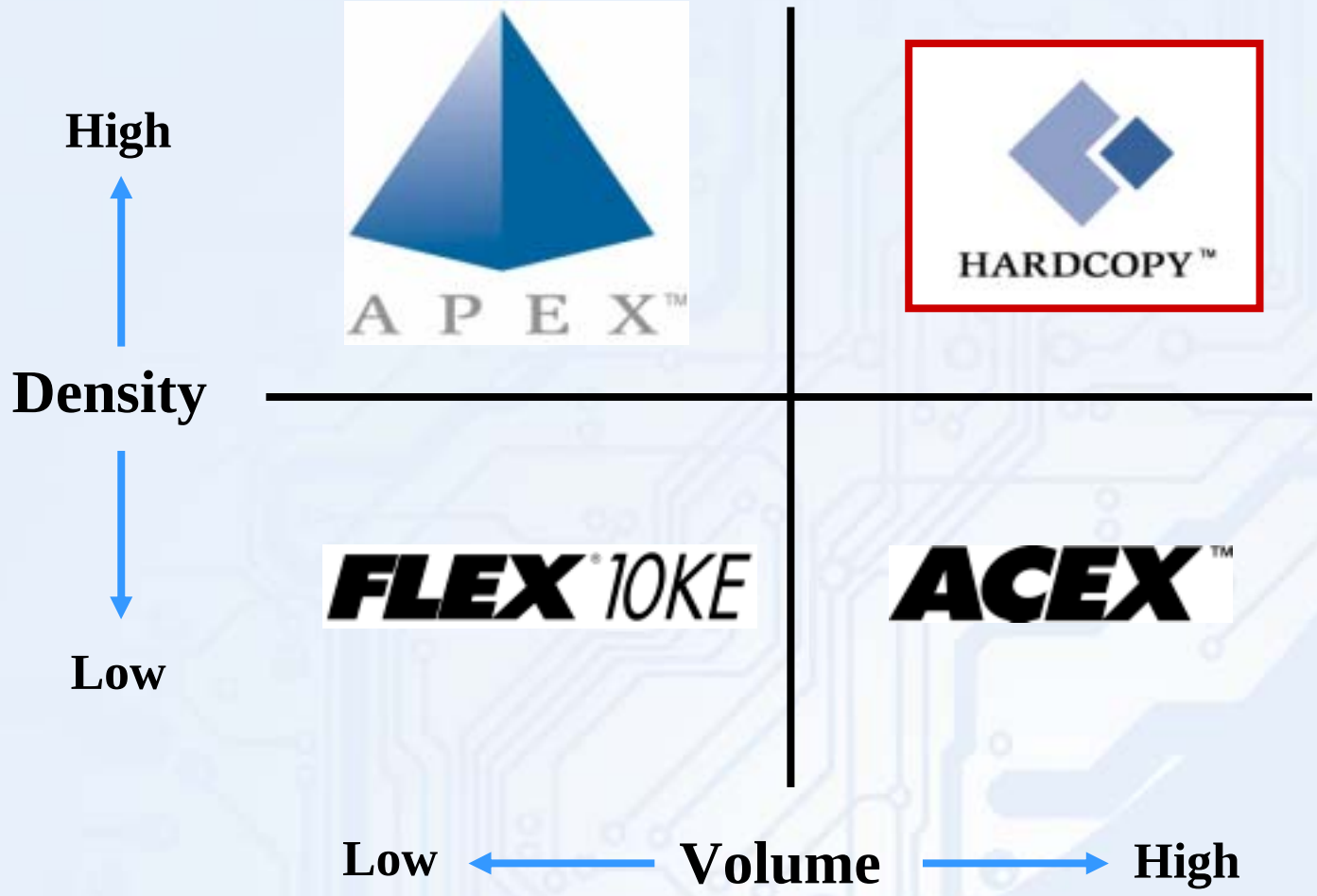
System-On-a-Programmable-Chip Solutions

ALTERA. MJL

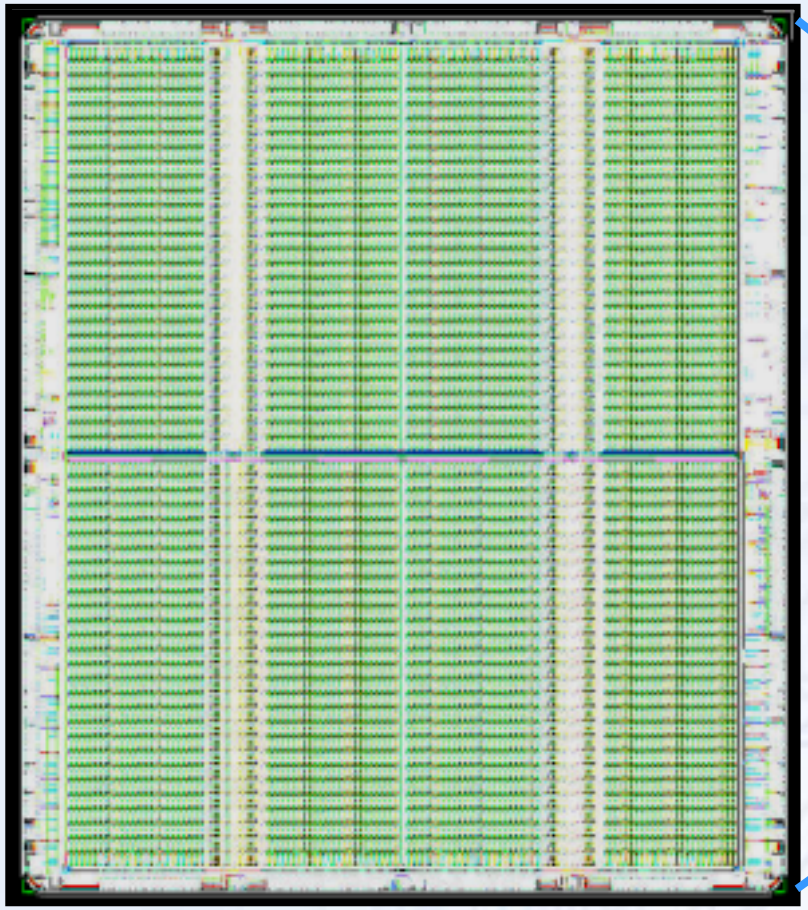
Introducing Altera HardCopy

- High-Volume, Low-Cost Roadmap for High-Density PLD Designs
- 90% Cost Savings from APEX™ 20KE Derived from 75% Die Shrink
- Revolutionary MPLD Implementation Process Provides Guaranteed Functionality & Performance with Minimal Customer Involvement
- PLD/MPLD Solution Optimizes Product Life Cycle Management
- New Process: <15 Weeks From Design Start to Production!

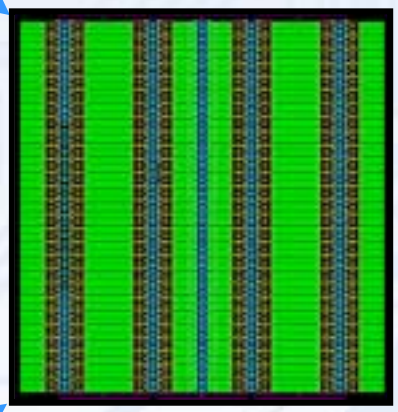
MPLD High Volume Solution



Die Size Reduction



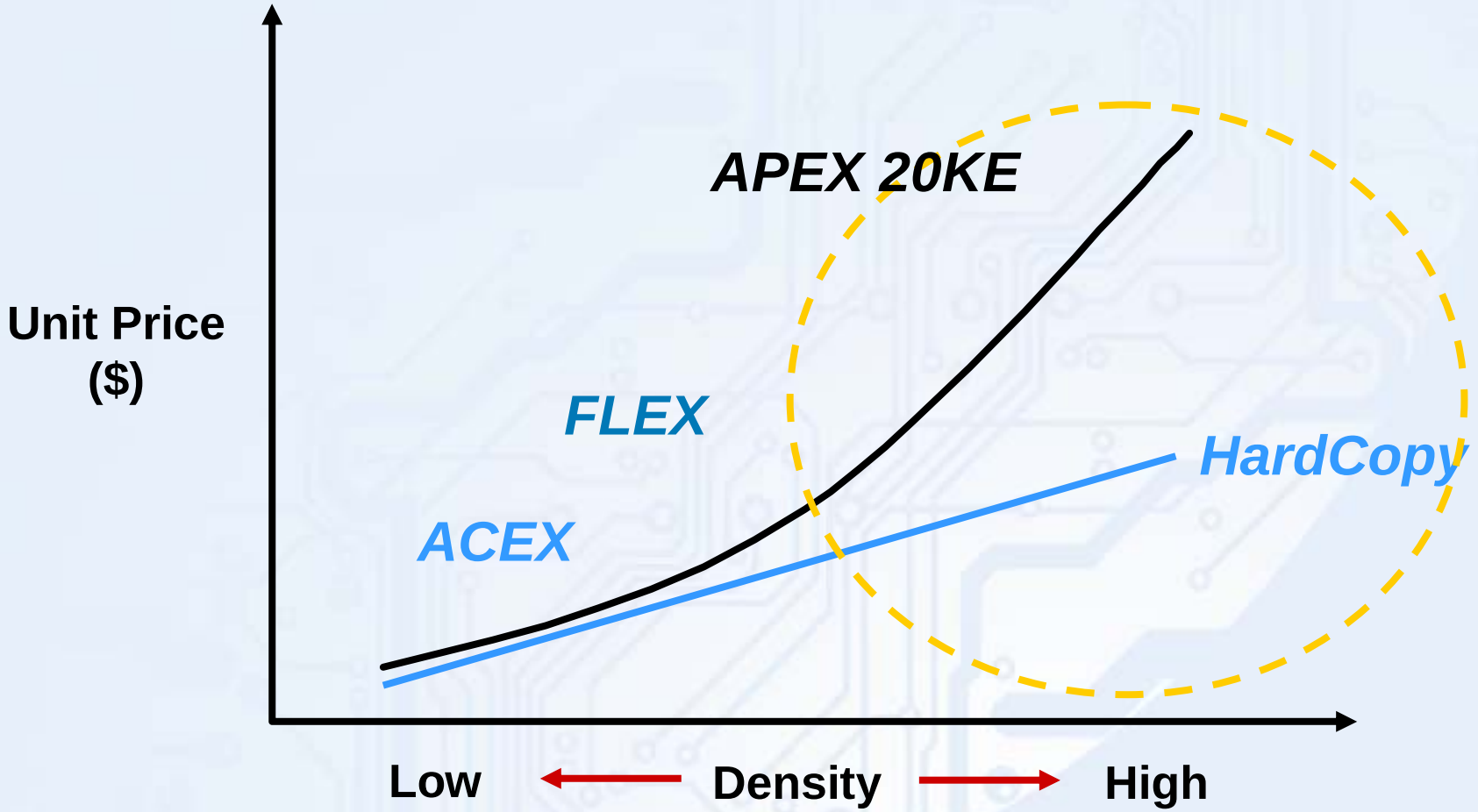
Original EP20K1500E



HardCopy
1500E Device

75% Reduction in Die Size

HardCopy Opportunity

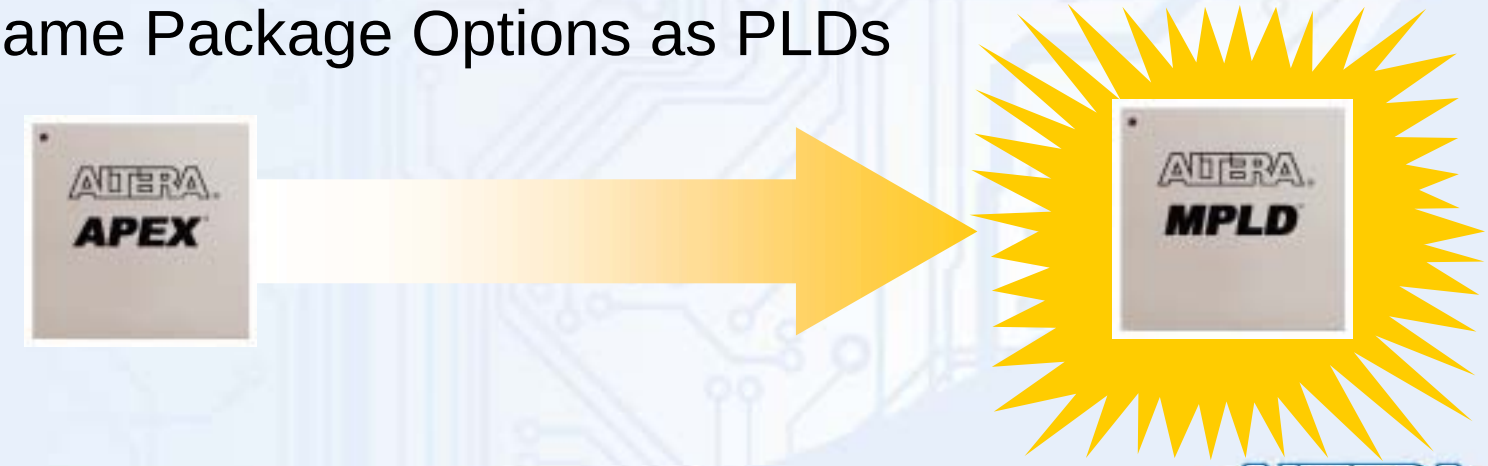


New MPLD Program Devices

Device	APEX 20KE Die Size	HardCopy Die
MP20K1500E		
MP20K1000E		
MP20K600E		
MP20K400E		

HardCopy Process Description

- Complete Design Development in APEX 20KE Device
- 1:1 Mapping of Logic Elements & Embedded System Blocks
- Remove Configuration Circuitry & Multiplex Interconnect Overhead—Replace with Metal Routing
- Guaranteed Functionality & Performance
- Pin-to-Pin Compatibility
- Same Package Options as PLDs



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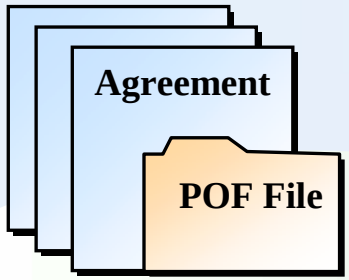
HardCopy Implementation & Business Guidelines

System-On-a-Programmable-Chip Solutions

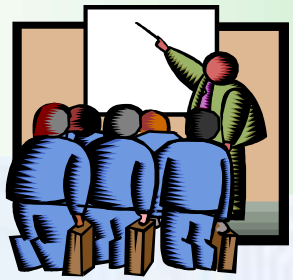
ALTERA. MJL

MPLD Engagement Flow



Step 1

Customer Submits APEX 20K Netlist or Programmer Object File (.pof) & Required Paperwork



Step 2

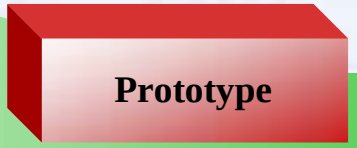
Altera Reviews & Accepts Design

Step 3

Customer Provides Order for DCC & First Year Production Quantity with Schedule

Step 4

Altera Starts MPLD Implementation



Step 5

Altera Delivers Prototypes to Customer

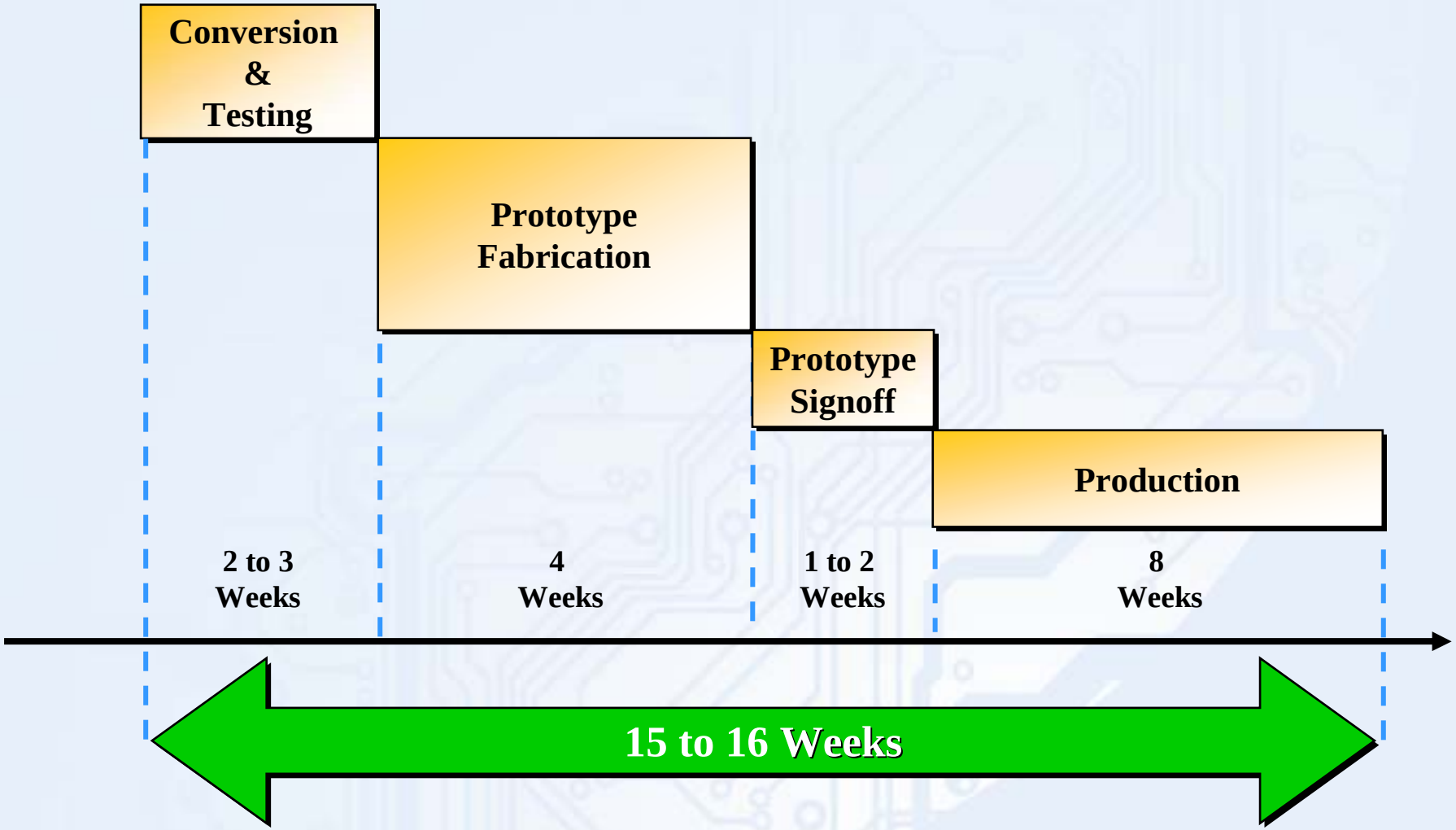
Step 6

Customer Approves Prototype

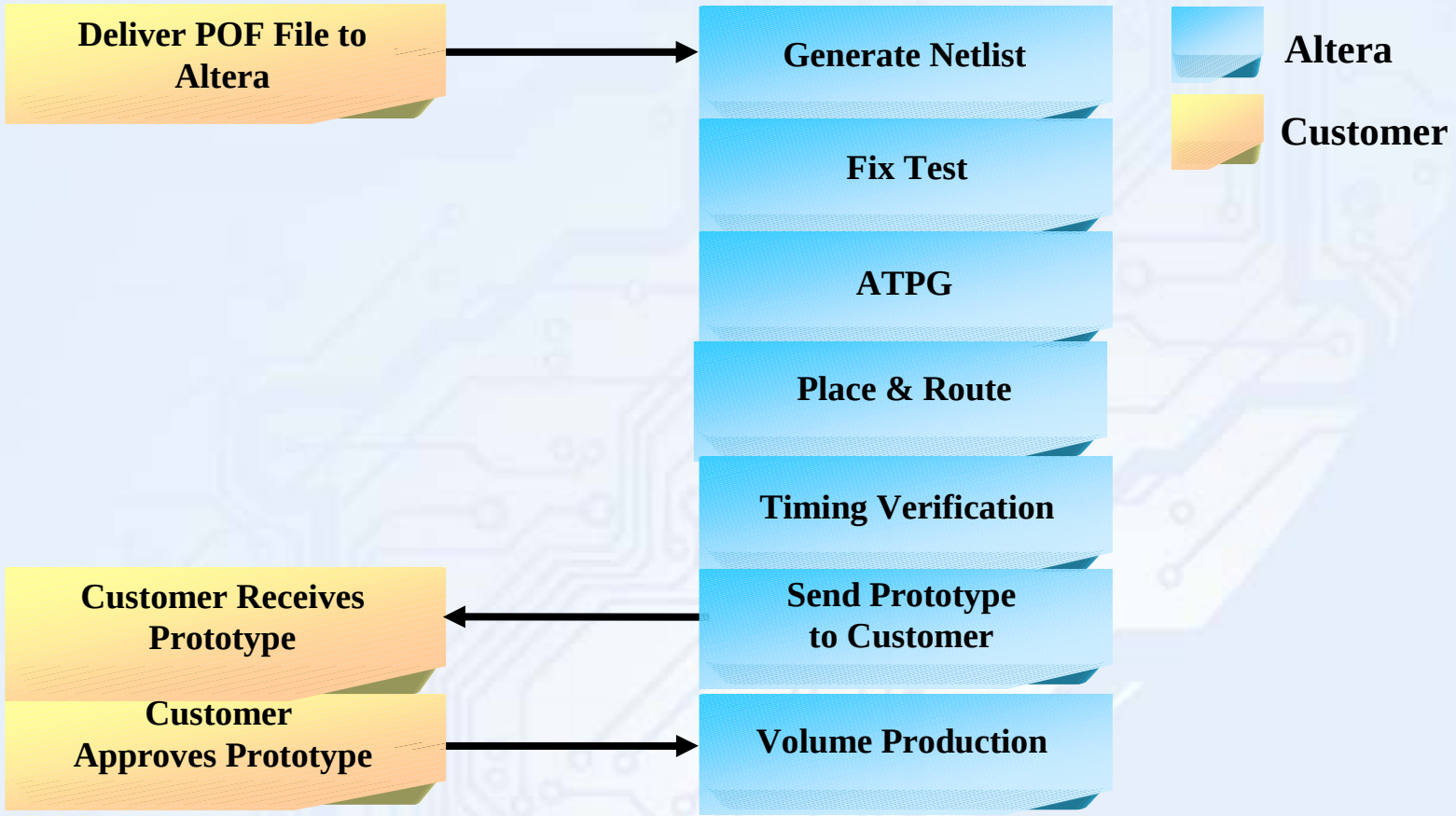
Step 7

Altera Starts Production

MPLD Implementation Timeline



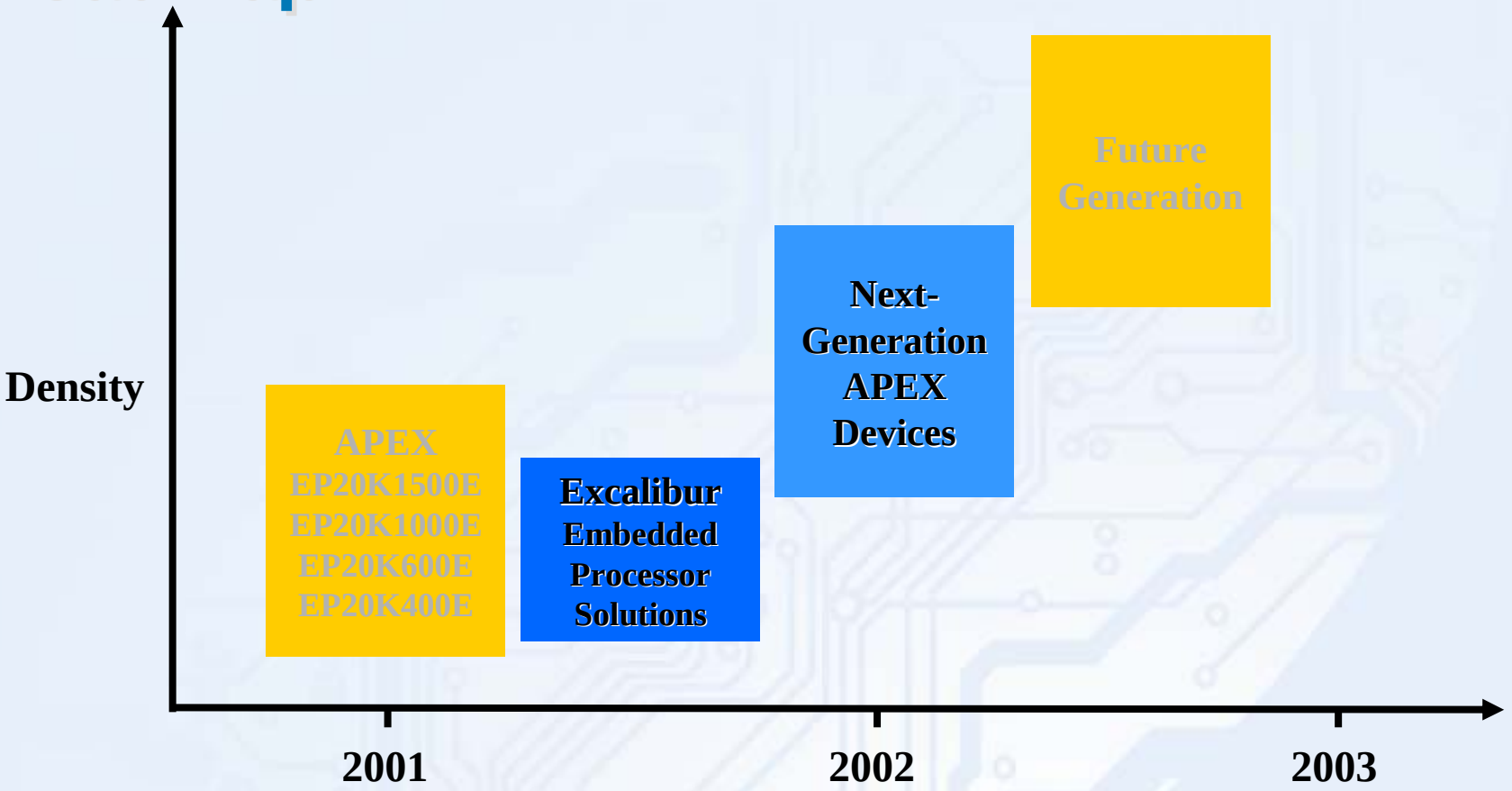
Testability & Verification Flow



Conversion Guideline

- Availability of Fully Functional APEX Netlist, .pof File
- Compliance with Design Rules
- No Customization or Changes from Original Design
  - Strictly One-to-One Conversion
  - No Direct Conversion from Virtex or Other Competitor Devices
  - No N:1 Conversion

Roadmap



For Each Generation, Only Highest-Density Members Are Offered as MPLDs

Business Guidelines

- Design Conversion Cost (DCC) Required
- Must Meet Annual Minimum Order Quantities
- Non-Cancelable & Non-Returnable

Device	Design Conversion Charge	Minimum Quantity per Year	High Volume* MPLD
MP20K1500E	$175K	2,500	$150
MP20K1000E	$150K	5,000	$100
MP20K600E	$125K	15,000	$ 60
MP20K400E	$100K	25,000	$ 45

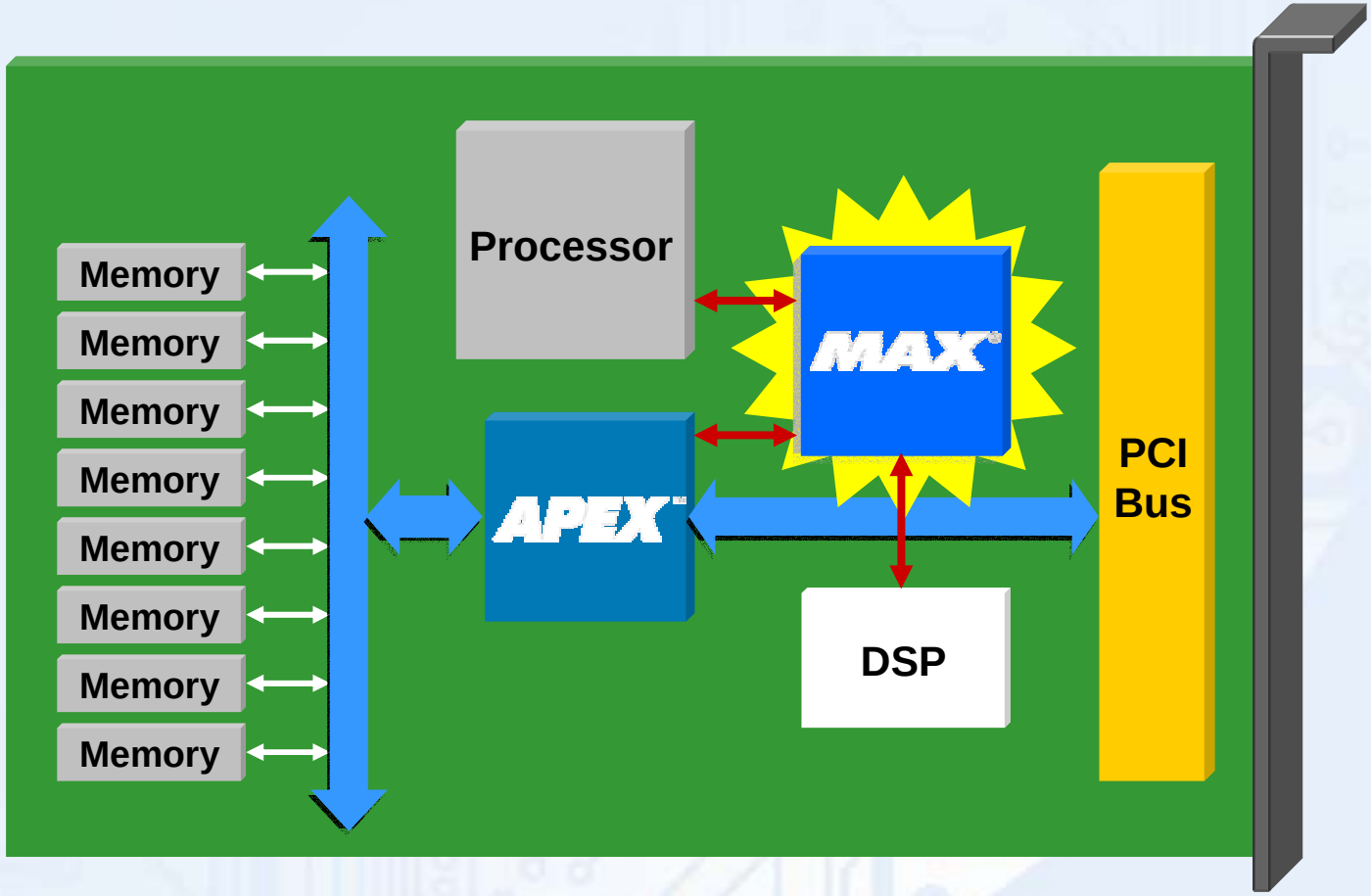
*Budgetary 100,000 Unit Pricing

Summary

- PLD + HardCopy = Maximum Flexibility
  - Develop & Ramp into Production with PLDs
  - Migrate to Volume Production with HardCopy Devices
- Low Cost
  - Up to 90% Cost Saving over High-Density PLDs
  - Eliminates Development & Qualification Costs
- Easy “No-Risk” Implementation
  - Minimal Customer Interaction
  - Guaranteed Functionality & Performance

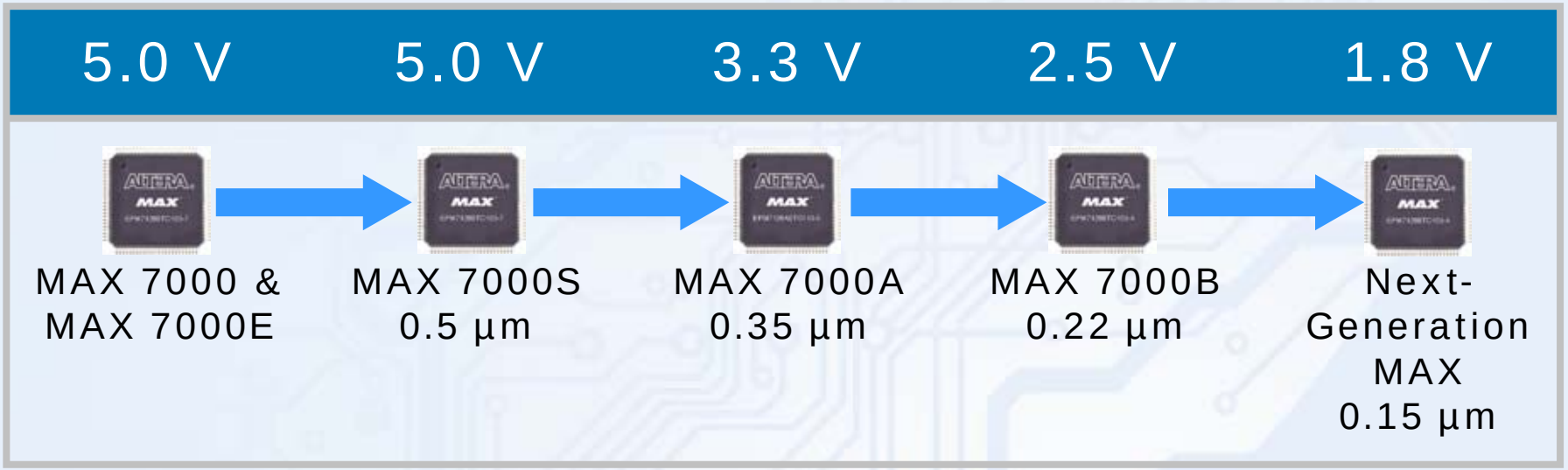
ALTERA®

MAX Devices: *Super* Glue Logic



Five Generations of MAX Devices

- Altera Continues to Invest Aggressively in MAX Devices

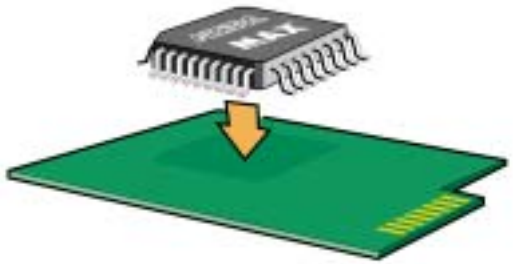


History of Technology Leadership

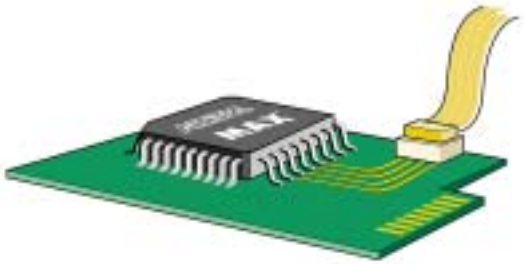
MAX 7000B


No comparison.
ALTERA
MAX
7000B
Other Vendors:
Insert here,
when available.
• 0.22-µ, 2.5-V ISP
• Industry's fastest PLD
• 32 to 512 macrocells
• Advanced high-speed I/O standards
• Shipping any volume, any time
MAX
ON BOARD
Dare to compare.
We've made comparing our MAX® 7000B family easy. That's because feature for feature no other family of devices comes close. With 2.5-V advanced ISP,
as fast as 3.5 ns, and counters as fast as 285 MHz, MAX 7000B devices extend Altera's ISP leadership even further.
But don't take our word for it—compare for yourself.
Go to http://www.altera.com/compare for a sample kit with a free MAX 7000B device, and see what we offer that the competition can't.
Altera. The clear ISP leader.
ALTERA.
The Programmable Solutions Company®
http://www.altera.com/compare

ISP Increases Flexibility



Mount Unprogrammed



Program In-System

Reprogram in the Field

- No Device Handling
- No Bent Leads
- Allows Generic Inventory
- Easy Prototyping
- Supports Changes During Manufacturing/ Test Flow
- Allows Field Upgrades
- Add Enhancements Quickly & Easily

Why Product-Term Devices?

- Low-Density Logic Integration
  - Best Technology for Simple Integration
- High Performance
  - t_{PD}, t_{SU}, f_{MAX}
- Ease-of-Use, Predictability, Comfort Level
  - Software, Routing, Methodology, Timing, No Configuration, Etc.
- Non-Volatile, Single Chip
  - Great for Start-up Functionality
  - No Cost for Configuration

End Applications: You Name It!

- Communication Infrastructure Systems
  - Switches & Routers
  - ATM Line Cards
  - Wireless Basestations
  - Optical Networking Systems
- Consumer Systems
  - Set-Top Boxes
  - MP3 Music Players
- Data Processing Systems
  - Storage/Applications Servers
  - RAID Systems
  - Laptops/Notebook Computers

Two-Tier Product Offering

5.0 V

MAX 7000S

- Performance Leader
- Feature Leader
- Wide Range of Package Offerings
- Industrial-Grade Offerings

3.3 V

MAX 7000AE

- Performance Leader
- Feature Leader
- Wide Range of Package Offerings

MAX 3000A

- Price Leader
- Equivalent Performance
- Feature & Package Subset of MAX 7000AE

2.5 V

MAX 7000B

- Performance Leader
- Feature Leader
- Wide Range of Package Offerings

MAX 3000B

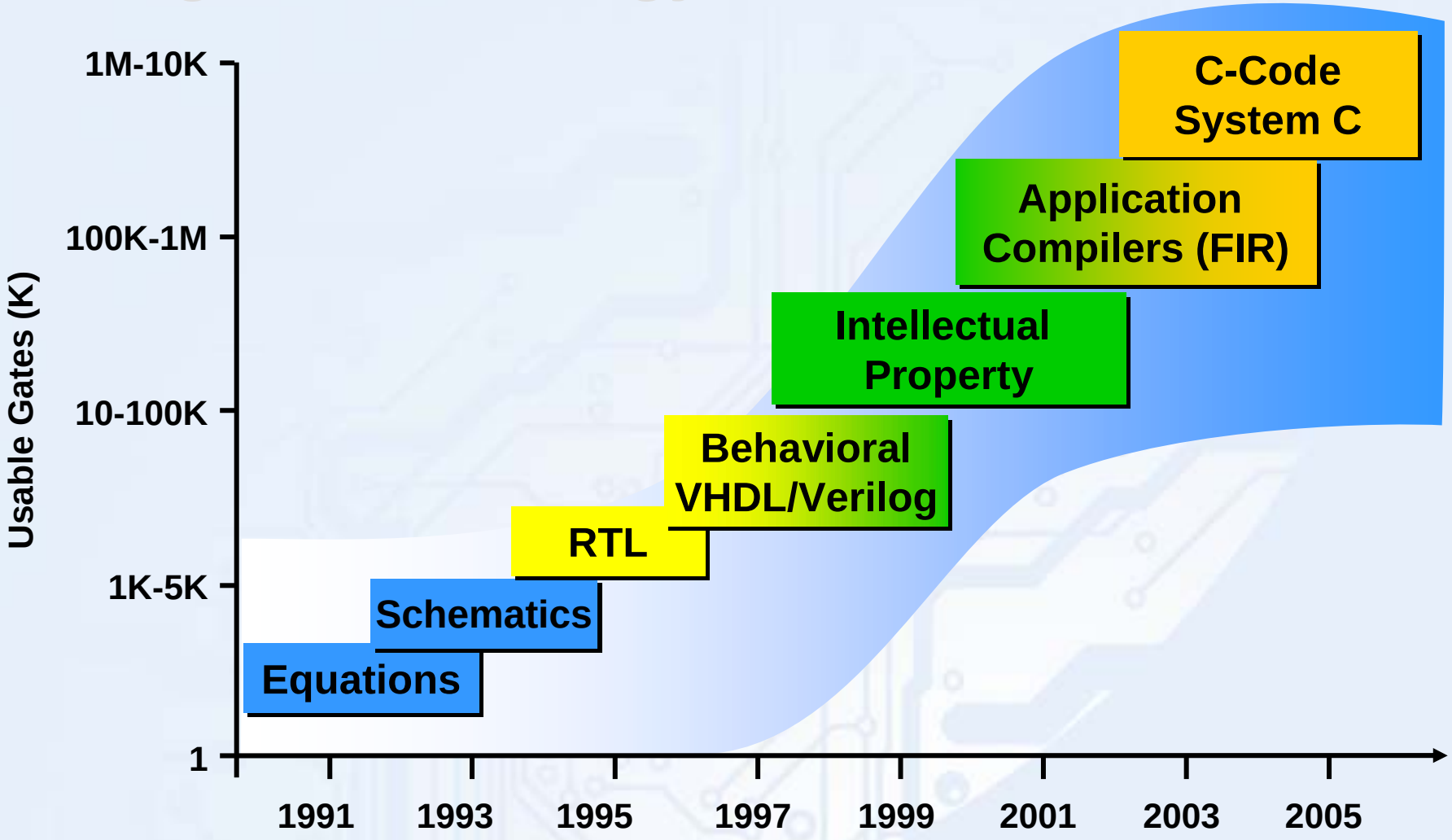
- Price Leader
- Slower Performance
- Feature & Package Subset of MAX 7000B

ALTERA®

Quartus II

- **Quartus® II Background**
- **Quartus II Overview**
- **Quartus II Features**
  - LogicLock™ Incremental Design Methodology
  - Excalibur™ Embedded Processor Design Flow
  - Complete IP Integration Design Flow
- **Summary**

Design Methodology Shifts



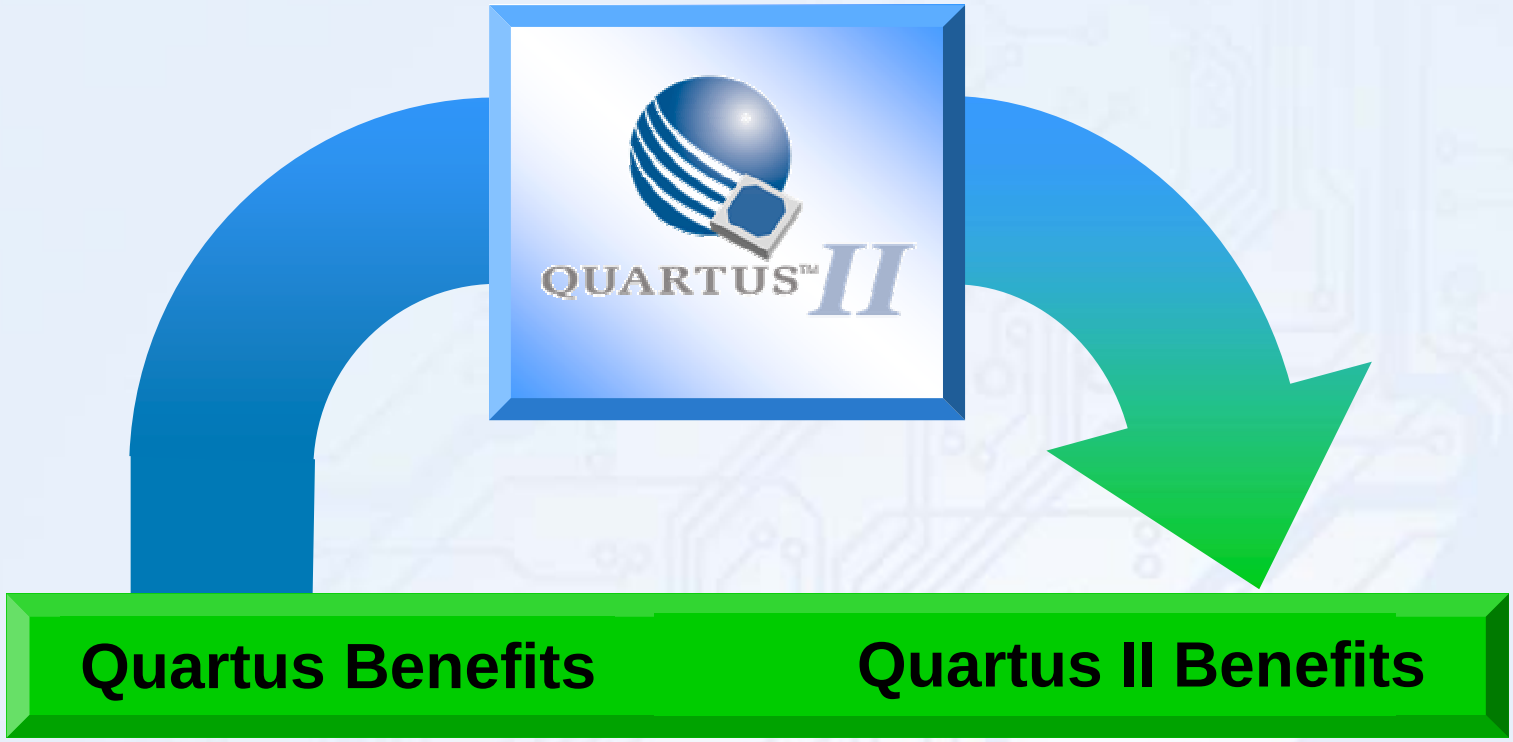
SOPC Design Flow

- **System-Level Design Capabilities**
  - LogicLock Incremental Design Flow
  - System-on-a-Programmable-Chip (SOPC) Builder IP Integration Tool
  - ARM® Development Tools
  - I/O Features Support
  - MegaWizard® Plug-In Portal
  - DSP System Design Flow

- **Fastest Performance**
  - PowerFit™ Technology
  - Wildcard Support
  - LogicLock Performance Preservation
  - New Routing Algorithms
  - New Constraint User Interface

- **Robust Verification**
  - ModelSim™ Tool AE Included
  - SignalTap® II Logic Analyzer
  - Development Boards
  - Simulation Models for Supported Devices

Quartus Software Benefits



- SignalTap Logic Analysis
- NativeLink™ Integration
- Intellectual Property
- TCL Scripting

- LogicLock Incremental Design
- Industry's Fastest Place & Route
- 30% to 60% f_{MAX} Improvement
- SOPC Design Environment

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LogicLock

The First Real Incremental Design Methodology for Programmable Logic

ALTERA. MJL

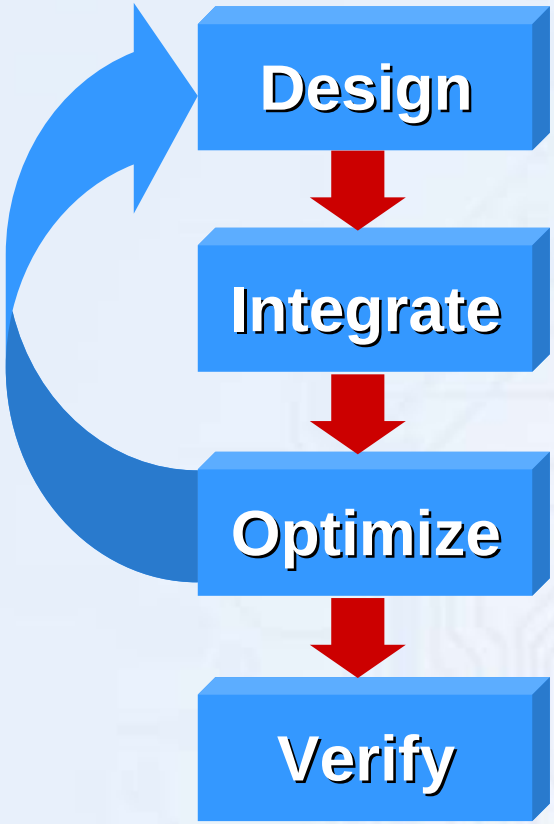
System-On-a-Programmable-Chip Solutions

LogicLock Benefits

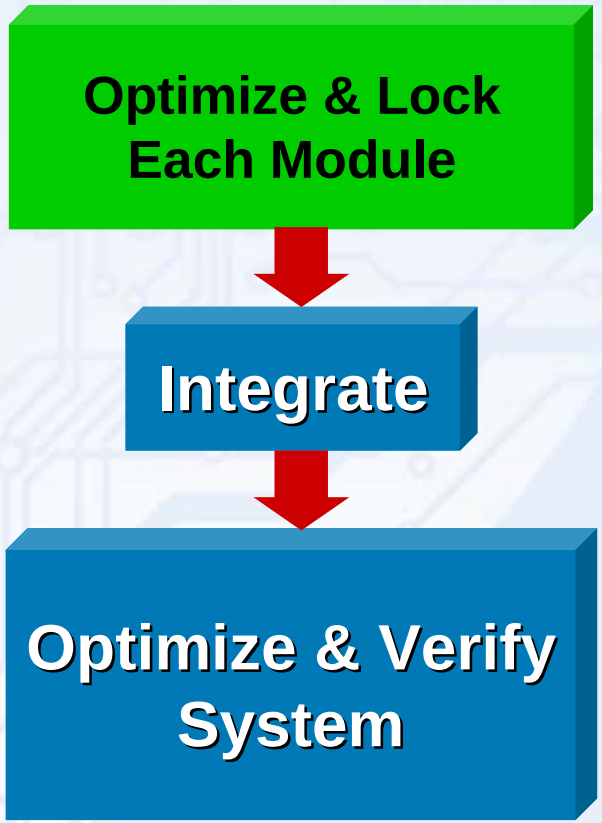
- Block-Level Performance Preservation
  - Synthesis
  - Fitting
- Designer Productivity Increased
  - Supports Iterative Design Process for Multi-Clock Domains
  - Enables Teamwork on Very Large Designs
- Design Reuse Enabled
  - Allows Portable Constraints
  - Reduces IP Development Cost
  - Reduces IP Reuse Risks

Design Flows

Old Design Flow

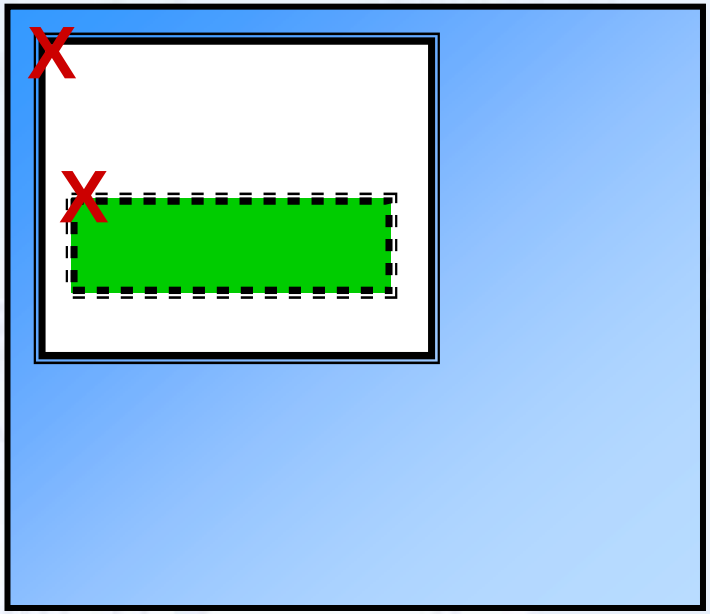


LogicLock Design Flow

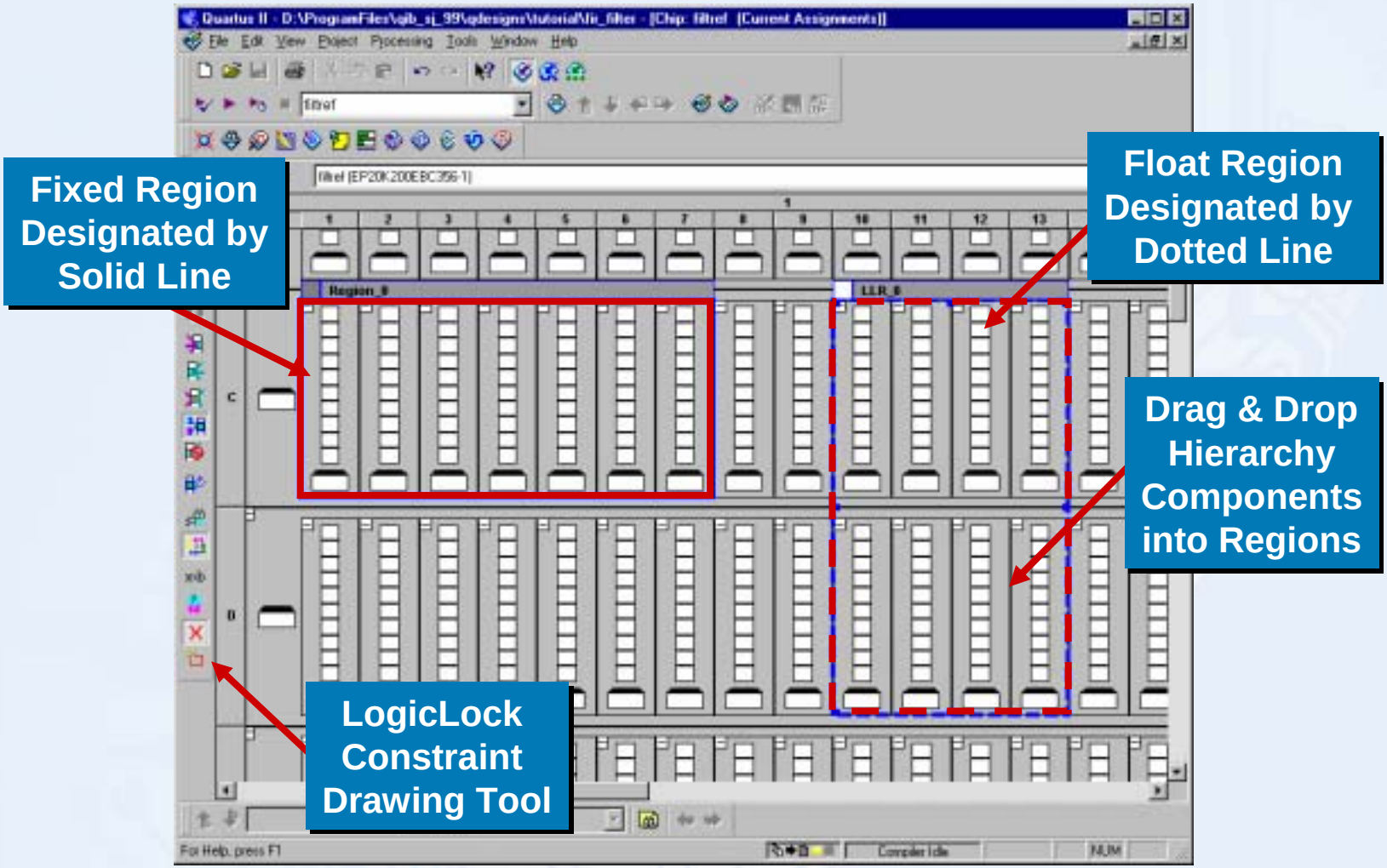


LogicLock Location Constraint Types

- Fixed Region
  - Hard Assignment to Specific Location
  - Not Portable between Devices
  - Designated by Solid Line in Floorplan Editor
- Floating Region
  - Quartus II Tool Chooses Location
  - Portable between Devices
  - Designated by Dotted Line in Floorplan Editor
- Relative
  - Hierarchical Constraint “Children”
  - Define Region Constraint Relative to Higher Level Constraint
  - Portable between Devices
  - If Parent Moves, Child Moves Too (Even if Fixed)

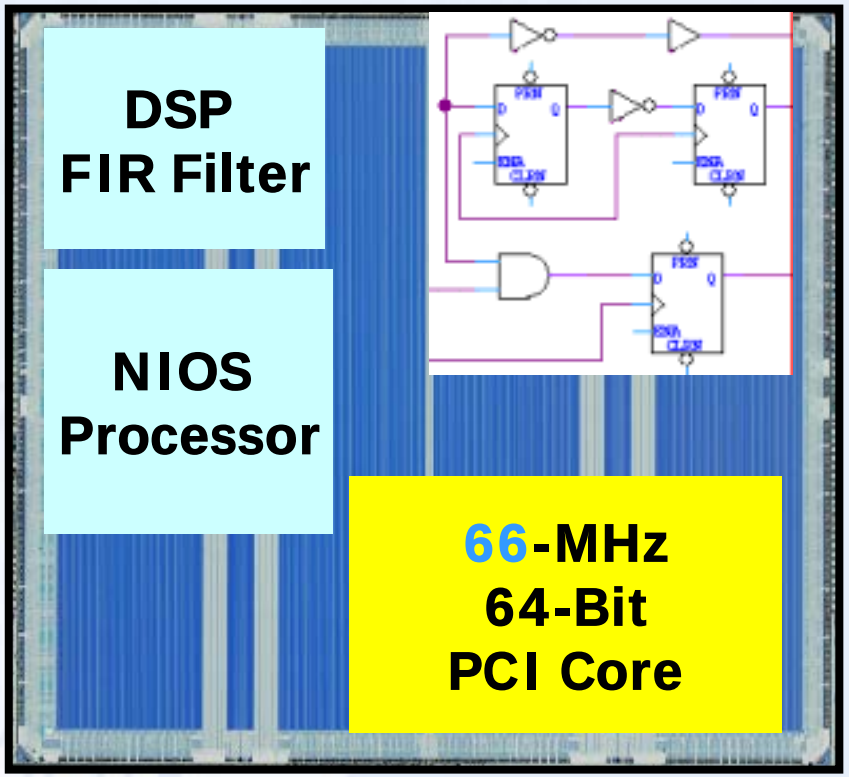


Simple Example



Modular Design Capability

- Optimize Module
  - Meet Performance
  - Verify Module
- Lock Down Module
  - e.g. DSP FIR Filter
- Add Additional Modules
  - Performance on DSP FIR Filter Maintained
- Optimize Additional Modules
  - Meet Performance
  - Verify Modules
- Verify System Performance



What is Incremental Compilation

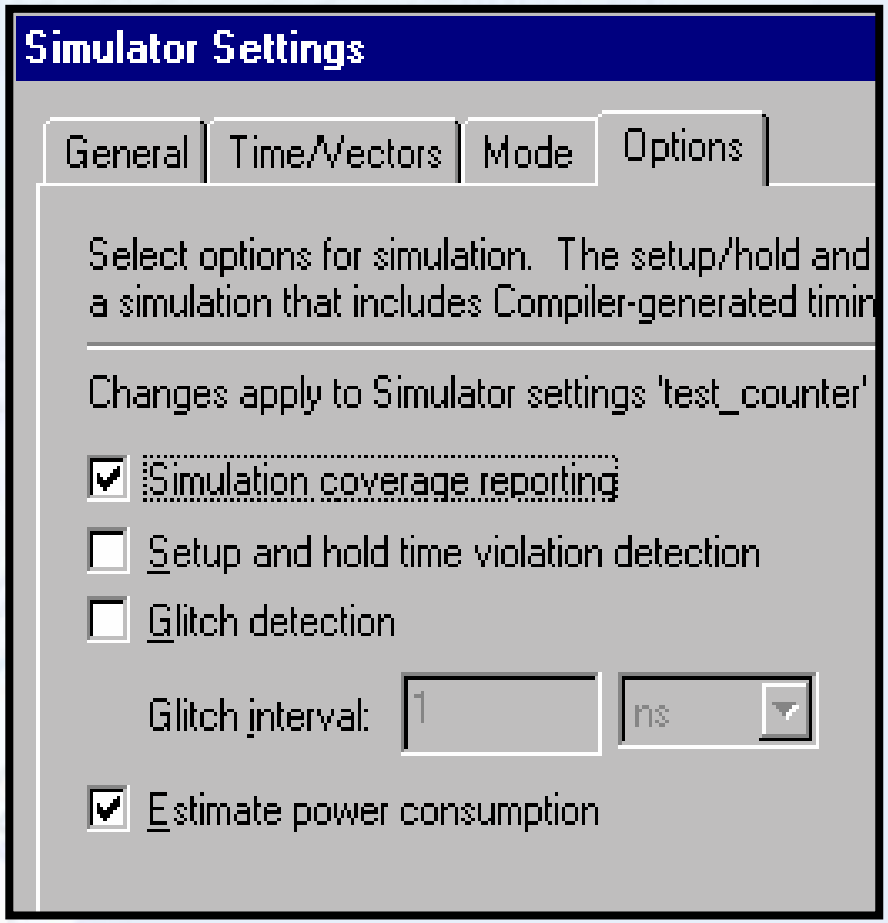
Incremental Synthesis	Incremental Fitting
Multiple EDIF/VQM Files User Creates EDIF/VQM for Modules User Implements Modules with Constraints User Can Export EDIF/VQM & Constraints Recompile Only Modified EDIF/VQMs	Placement Hard Lock Nodes to Fitted Lcells in region Soft Lock Nodes Floating in Region Lock Complete Project
Synthesize_Separately Option Synthesizes Only Modified Source Files	Routing Routing is Not Lockable

PowerGauge™ Analysis Software

- Calculates Power Estimation Based on Simulation File
  - Toggle Rate Derived from User Generated Simulation Vectors
  - Uses Quartus Simulator
  - Accuracy Dependent on Test Vectors

Summary

Setting Name	Setting Value
Simulation Start Time	0 ps
Simulation End Time	100.49 ns
Number of transitions	91
Internal Power	144.725 mW
IO Power	231 . mW
Total Power	375.725 mW



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Excalibur Processor Design Flow & IP Integration Tools

System-On-a-Programmable-Chip Solutions

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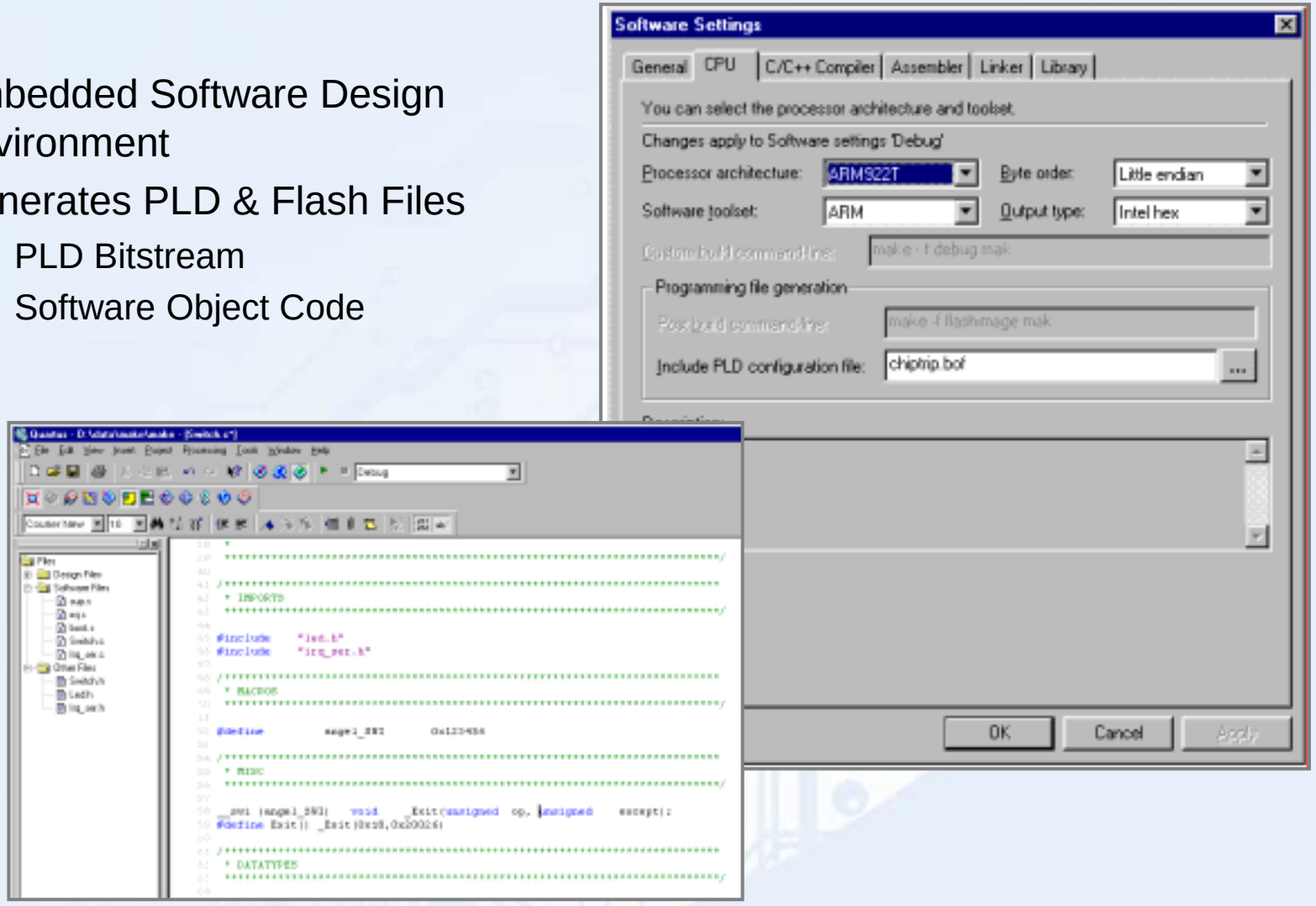
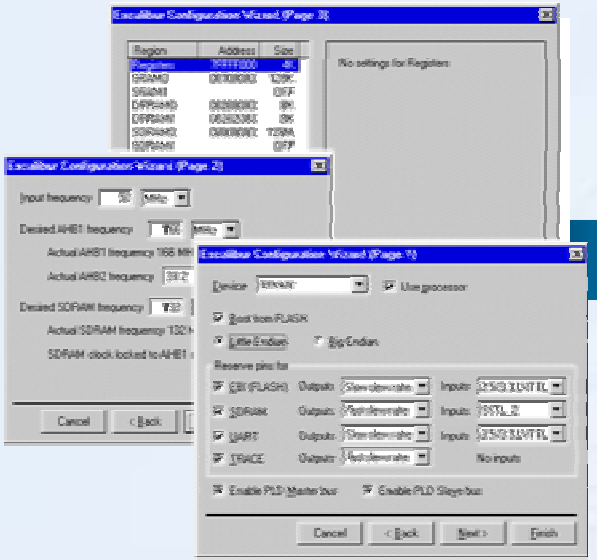
Quartus II SoftMode™ Design Entry

- Embedded Software Design Environment
- Generates PLD & Flash Files
  - PLD Bitstream
  - Software Object Code



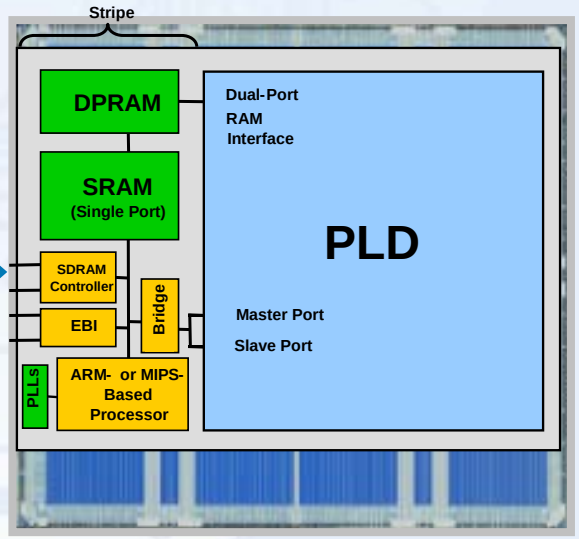
SOPC Builder



Configured Silicon Features
(e.g., Memory Mapping)

Configured IP Cores

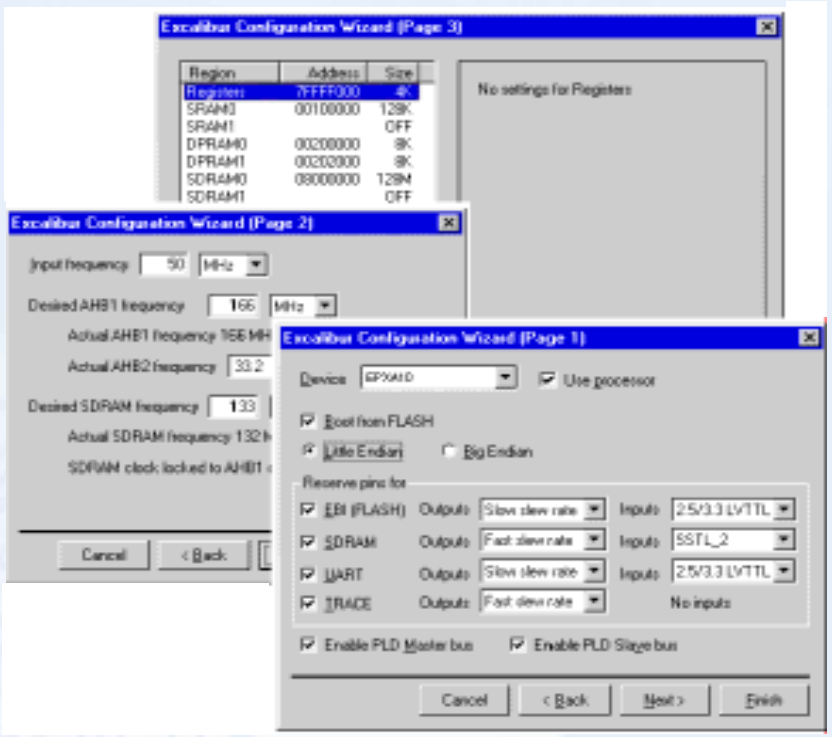
Interconnect Ports



Completed SOPC Architecture

SOPC Builder Benefits

- “Risk-Free” Architectural Exploration
- Automated IP Integration Flow
- Excalibur Demo



Instant Embedded Processor Design!

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OpenCore Plus & IP Roadmap

ALTERA. MJL

The Altera OpenCore Philosophy

- Industry-First “Try Before You Buy” Philosophy for Intellectual Property
  - Risk-Free IP Evaluation Since 1996

- Altera OpenCore Technology Allows Evaluation of SOPC Design Containing IP Prior to Purchase of IP
  - Evaluate Entire Design, Not Just IP
  - Fully Featured IP
- Available for All Altera MegaCore and Most AMPP IP Products

Current OpenCore Flow

Simulate RTL in Third-Party Software

Download

Parameterize

Evaluate in Software

Purchase License

Ship Product

OpenCore™

MegaWizard™ Plug-In

QUARTUS™ II

BUY

Evaluate in Hardware

Introducing OpenCore Plus

- Truly Risk-Free IP Evaluation
- Free Hardware Evaluation
  - Time-Limited Hardware Evaluation Models Allow Use of Any Board
- Free RTL Simulation
  - Encrypted Models Support All Leading VHDL and Verilog Simulators
- Seamless Evaluation and Design Flow

New OpenCore Plus Flow

Simulate RTL in Third-Party Software

Now Free!

Purchase After RTL and H/W Evaluation

Download

Parameterize

Evaluate in Software

Purchase License

BUY

Ship Product

OpenCore™

MegaWizard™ Plug-In

QUARTUS™ II

Now Free!

Evaluate in Hardware

OpenCore Plus RTL Simulation

- Encrypted Models of MegaCore Functions Used for RTL (Functional) Simulation
- Models Are Parameterizable Via MegaWizard
- Faster than Gate-Level (**.vo**/**.vho**) Simulations
  - Up to 20X Faster Simulation Times
  - Faster Design Iterations - No Quartus Compilation Required
- Supports Most Common Simulators on PC or UNIX
  - ModelSim, Leapfrog, VCS, VSS, NC Verilog
- Two Primary Delivery Mechanisms
  - Models Created with Innoveda Visual IP Software
  - Models Created with ModelSim (Temporary)

OpenCore Plus Hardware Evaluation

- Special “Time-Limited” Version of Selected IP Functions Will Allow User to Generate a Special Programming File for Evaluation Only
  - IP Function Will Time-out After a Predetermined Number of Clock Cycles – May Reconfigure Device to Reset Timer
  - Same Features and Performance as Standard Version
- Requires Free OpenCore Plus License Available from www.altera.com Licensing Page
  - License Allows Compilation of Time-Limited Version for 7 Days
  - No Limitation on Number of Licenses – May Renew at Any Time
- Some Limitations:
  - No Gate-Level Netlist Generation Allowed for Time-Limited Version (Must Use Standard Version of IP for RTL Simulation)
  - MegaCore License Agreement Prohibits Use in Production System

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Intellectual Property Cores

Communications	Bus Interface	Digital Signal Processing	Processor, Peripheral
Ethernet MAC (10/100/Gigabit)	PCI Target	FIR Filter Compiler	Nios™ Processor
SONET Framer	PCI Master-Target	IIR Filter Compiler	Tensilica X-tensa Processor
T3/E3 Framer	PCI-X	Fast Fourier Transform	PalmChip Bus
Packet Over SONET Processor	CAN Bus	Reed Solomon Encoder/Decoder	SDRAM Controller
Utopia Master & Slave	IIC Master & Slave	Viterbi Decoder	DDR-SDRAM Controller
POS-PHY Interface	IEEE 1394	Turbo Encoder/Decoder	QDR-SDRAM Controller
HDLC Protocol Core	PowerPC Bus Arbiter	Interleaver/Deinterleaver	8237 DMA Controller
ADPCM (u-law, a-law)	PowerPC Bus Master	Digital Modulator	8255 Peripheral Interface
ATM Controller	PowerPC Bus Slave	NCO	8259 Interrupt Controller
CRC	USB Function Controller	Color Space Converter	8254 Timer/Counter
IMA Controller	USB Host Controller	Discrete Cosine Transform	8051, 6502, Z80
Telephony Tone Generator		Image Processing Library	

And More!

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SOPC Summary

System-On-a-Programmable-Chip Solutions

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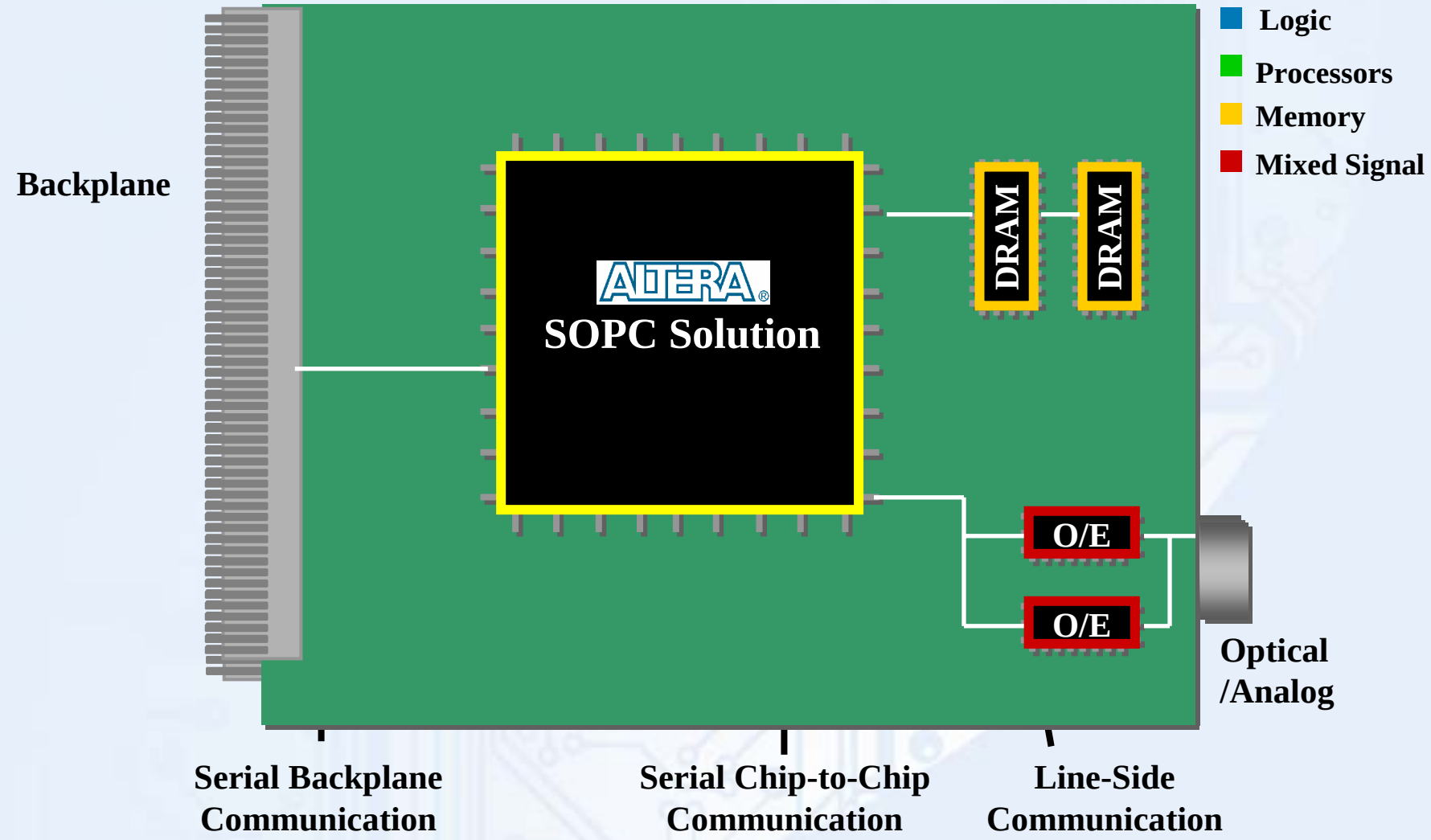
ALTERA SoPC Solution




POP QUIZ

Question

다음 중 Altera 에서 SoPC Solution으로 제공되는 제품들은?

1) Quartus II (Development Tool)
2) APEX 20KE/C, APEX II 디바이스
3) Altera MegaCore IP
4) Excalibur ARM 디바이스
5) 위의 모든 제품들

TIME'S UP!

End…Thank you!