SOPC WORLD 2002

Altera SOPC Solution

ALTERA.

2002: A Year to Remember

FPGAs for a System-on-a-Programmable Chip World

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SOPC Products From Applications

General-Purpose	High-Speed I/O Signaling	Embedded Processor	Low Cost, High-Volume
Stratix™	Stratix™ GX	EXCALIBUR™	Cyclone™ MAX®

Consumer & Automotive

Communications

Storage & Computer

Wireless

The PLD That Changes Everything

Now Shipping

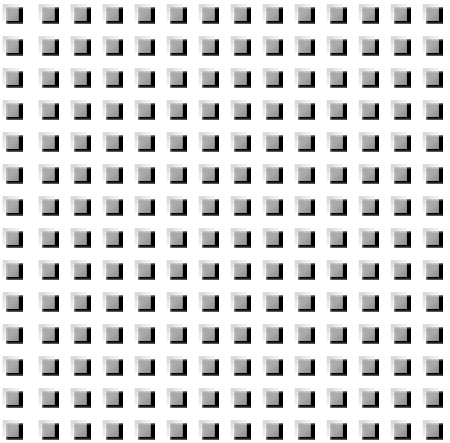
Up to 10-Mbits of TriMatrix™ Memory
Digital Signal Processing (DSP) Blocks
Advanced Clock Management Circuitry
Terminator™ Technology
Dedicated Memory Interface Circuitry

New Levels of System Integration

TriMatrix Memory

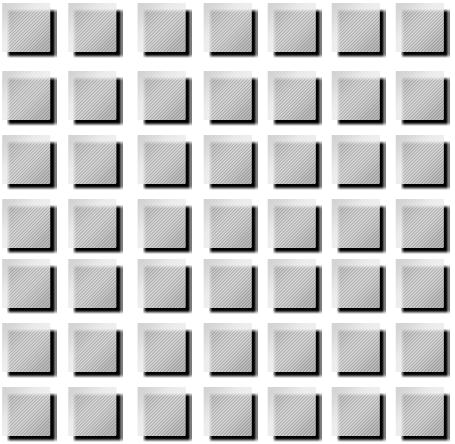
More Data Bits for Larger Memory Buffering

M512 Blocks



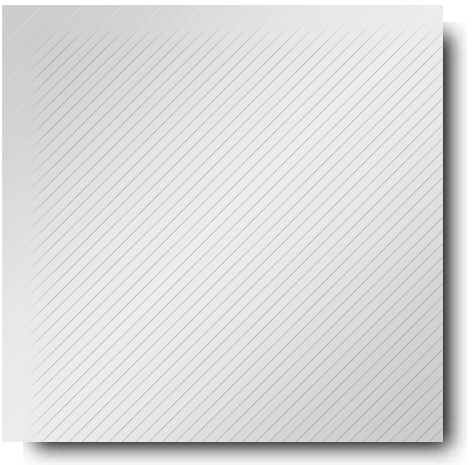
- 512 Bits per Block
- 32 Ports per Kbit
- Up to 1,118 Blocks

M4K Blocks



- 4 Kbits per Block
- 8 Ports per Kbit
- Up to 520 Blocks

M-RAM Block



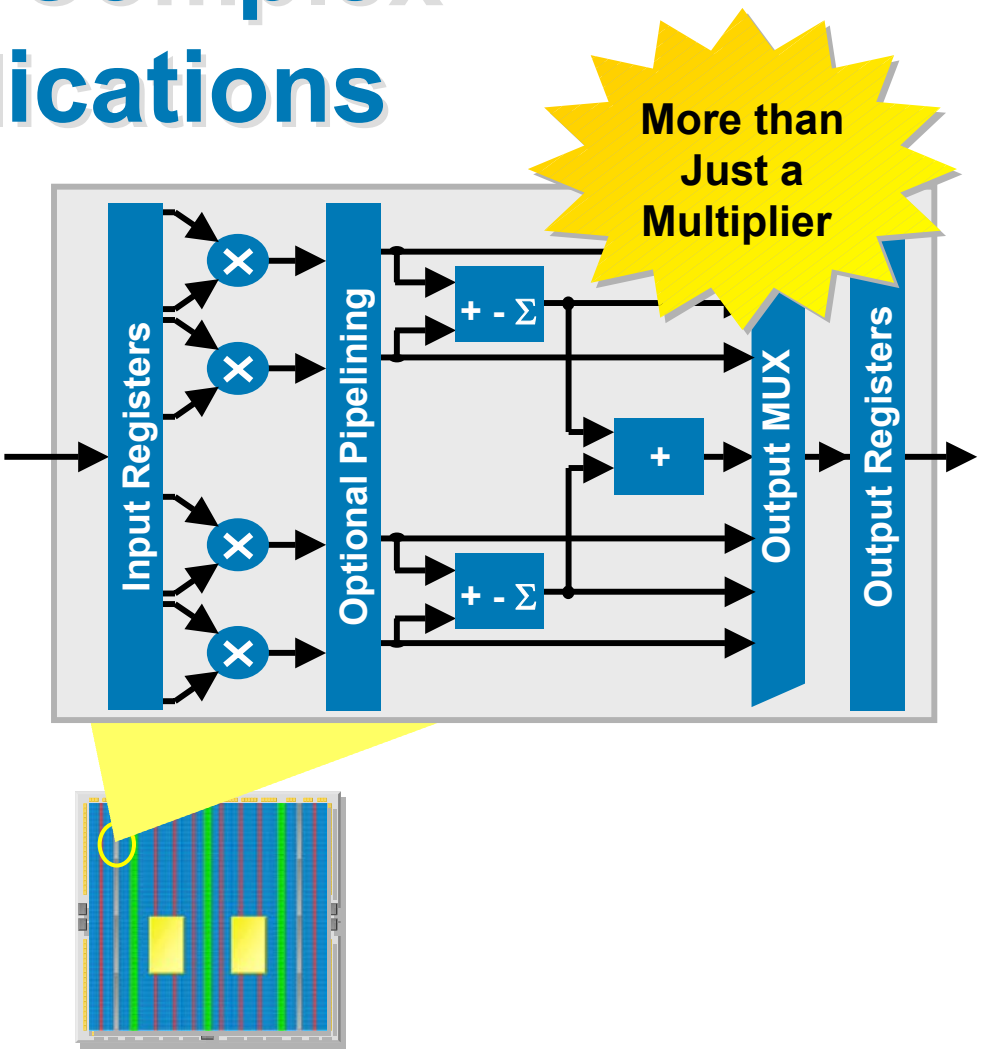
- 512 Kbits per Block
- 0.25 Ports per Kbit
- Up to 12 Blocks

More Data Ports for Greater Memory Bandwidth

Addresses Memory Bandwidth & Capacity Requirements

DSP Blocks for Complex Arithmetic Applications

- Wireless
  - Filtering & Compression
  - Encryption
  - Signal Processing
- Consumer
  - Image Processing
  - Audio Processing
  - Compression
- DataCom
  - Barrel Shifting
  - QoS Algorithms
  - Wide MUX Functions



Industry's Fastest DSP Performance

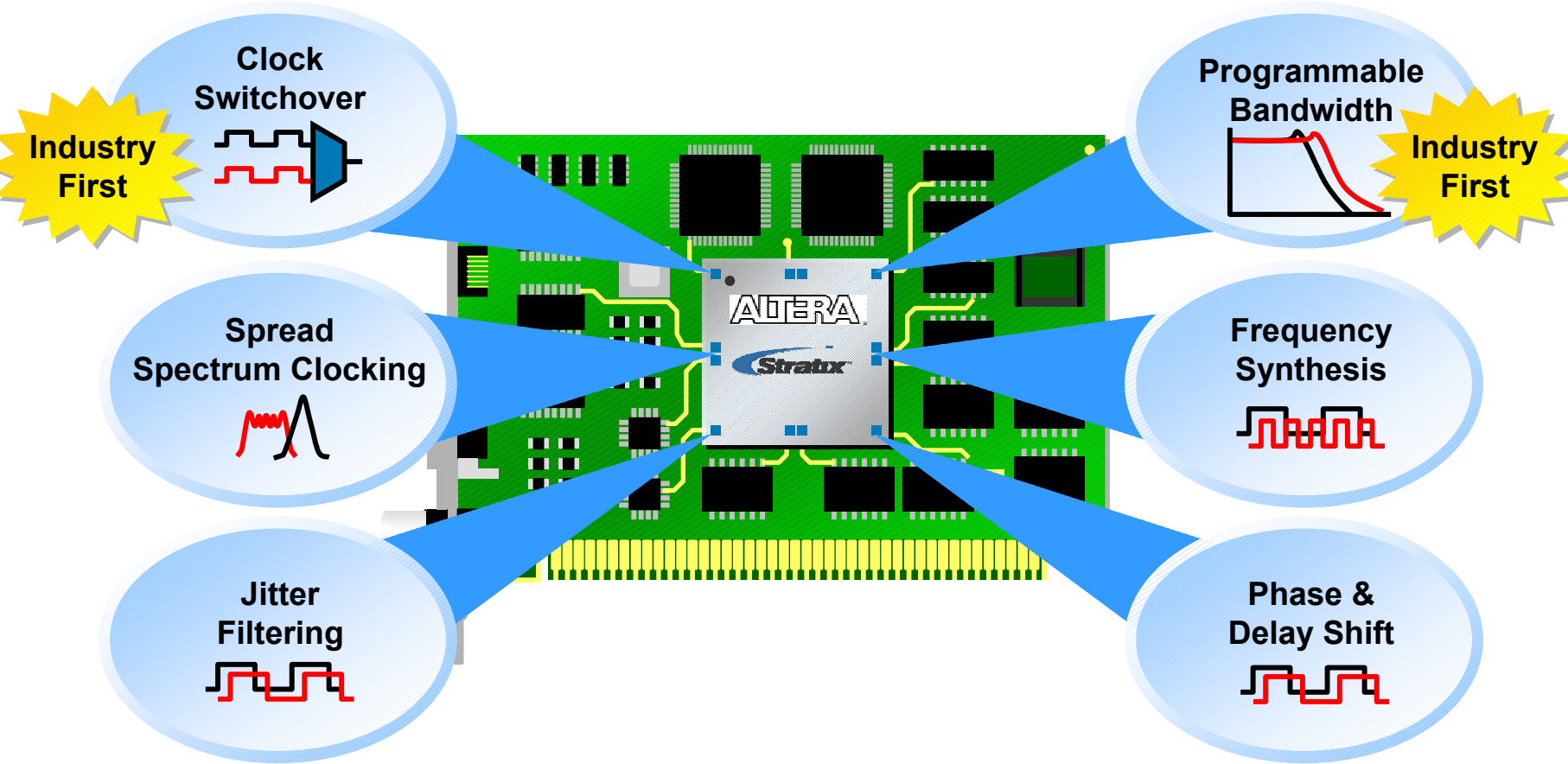
External Memory Interfaces

- Additional Storage Capacity Using External Memory Devices
- Data Access Performance Maximized
  - Enhanced I/O Circuitry
- Minimized Development Time
  - Off-the-Shelf, Customizable Controllers

Memory Technology	Maximum Clock Speed	Maximum Data Rate
Single Data Rate (SDR) SDRAM *(1)*	200 MHz	200 Mbps
Double Data Rate (DDR) SDRAM	200 MHz	400 Mbps
DDR Fast Cycle RAM (FCRAM)	200 MHz	400 Mbps
Quad Data Rate (QDR) SRAM *(2)*	167 MHz	668 Mbps
QDRII SRAM	167 MHz	668 Mbps
Zero Bus Turnaround (ZBT) SRAM	200 MHz	200 Mbps

(1) Synchronous Dynamic Random Access Memory
(2) Synchronous Random Access Memory

System Clock Management



Advanced Feature Set for Complete System Clock Management

The Stratix Device Family

Device	Logic Elements	32x18 M512 Blocks	128x36 M4K Blocks	4,096x144 M-RAM Blocks	Total RAM Bits	DSP Blocks	Sample Availability
EP1S10	10,570	94	60	1	920,448	6	NOW
EP1S20	18,460	194	82	2	1,669,248	10	NOW
EP1S25	25,660	224	138	2	1,944,576	10	NOW
EP1S30	32,470	295	171	4	3,317,184	12	NOV'02
EP1S40	41,250	384	183	4	3,423,744	14	NOW
EP1S60	57,120	574	292	6	5,215,104	18	APR'03
EP1S80	79,040	767	364	9	7,427,520	22	NOW
EP1S120	114,140	1,118	520	12	10,118,016	28	2H'03

EP1S10, EP1S25, EP1S40 & EP1S80 Shipping Today

Need for Two Technologies

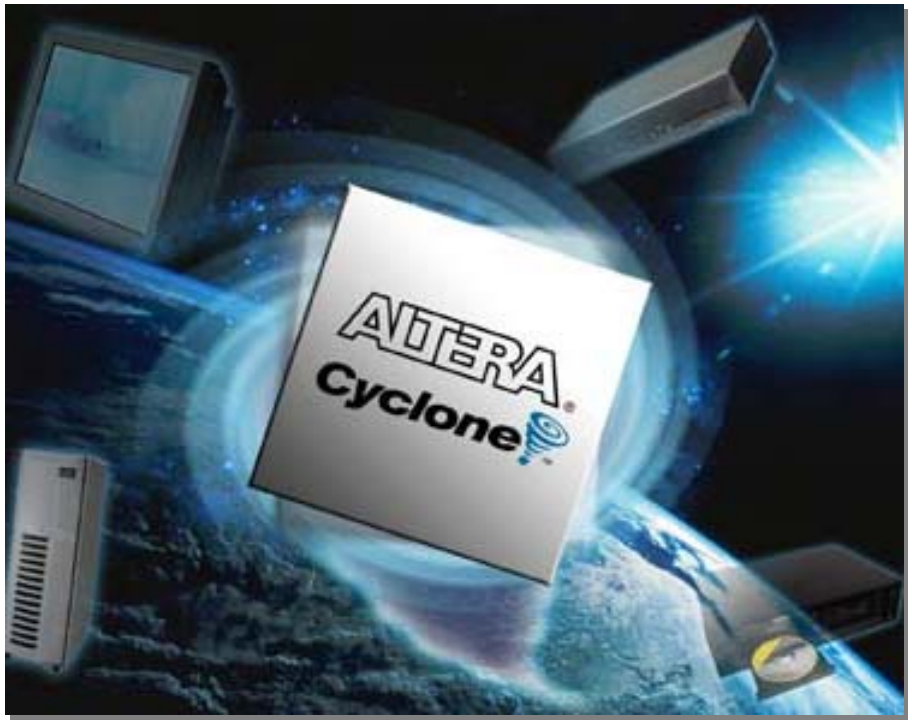
End Product ASP	$25K +	$1000 to $25K	$200 to $1000
Typical Units	< 10K Units	10K - 100K Units	100K - 5M Units

Stratix™

Cyclone™

Introducing Cyclone Devices

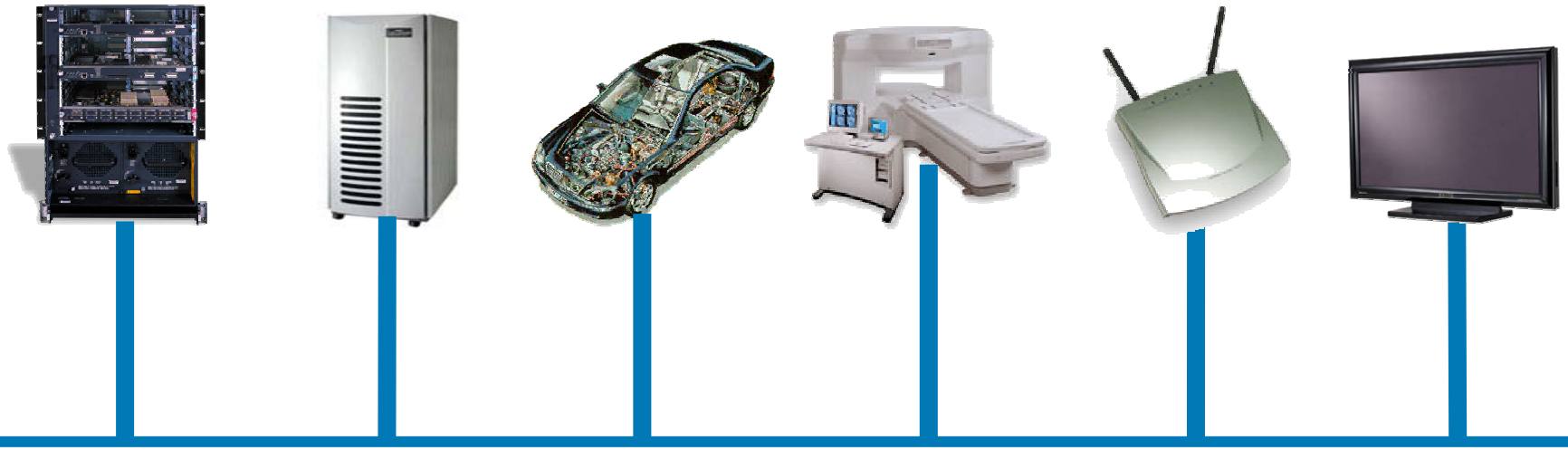
- Industry's Lowest Cost FPGA Family
  - Half the Price of The Competition
  - 4X The Density of Previous Low-Cost FPGAs
- Targeted Feature Set
- Eliminates the Low-End ASIC Decision



The Storm is Here!

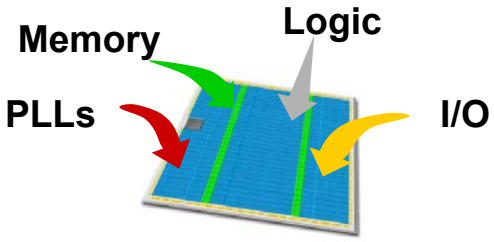
Low Cost By Design

Networking *Computer* *Automotive* *Industrial* *Wireless* *Consumer*



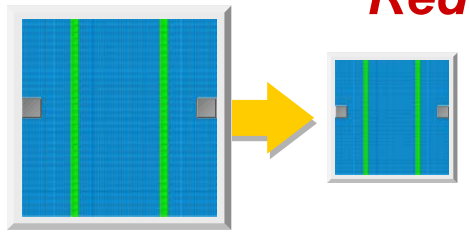
1 **Customer Requirements**

2 **Architecture Definition**

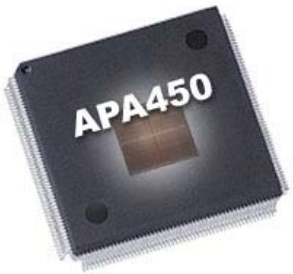


3 **Architecture Optimization**

60% Reduction



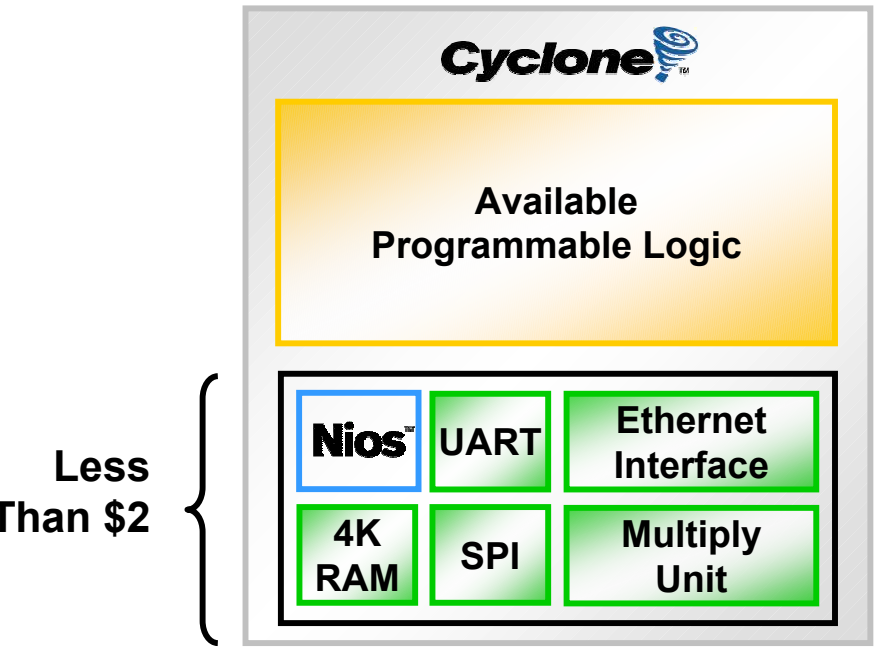
Half the Price of Competition

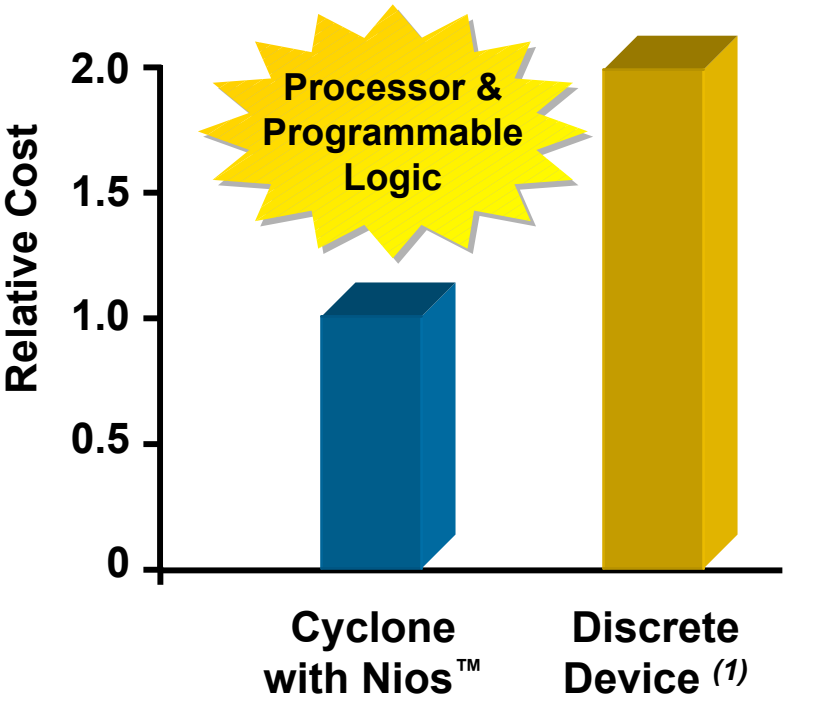
Product Features	Cyclone Devices	Spartan-IIE Devices	ProASIC^{PLUS} Devices	ispXP Devices
				
Relative Die Size	1.0	2.1	N/A	N/A
Density (LEs)	5,980	6,144	~6,100	7,056
Price (1)	$8.95	$17.95	~$35.00	~$125.00

(1) Obtained From (or Based on) Product Press Releases

The Key to High Volume

Low-Cost Microprocessor





(1) Based on Motorola 68HC12 Distributor Pricing

32-Bit RISC Processor Subsystem for Less than $2

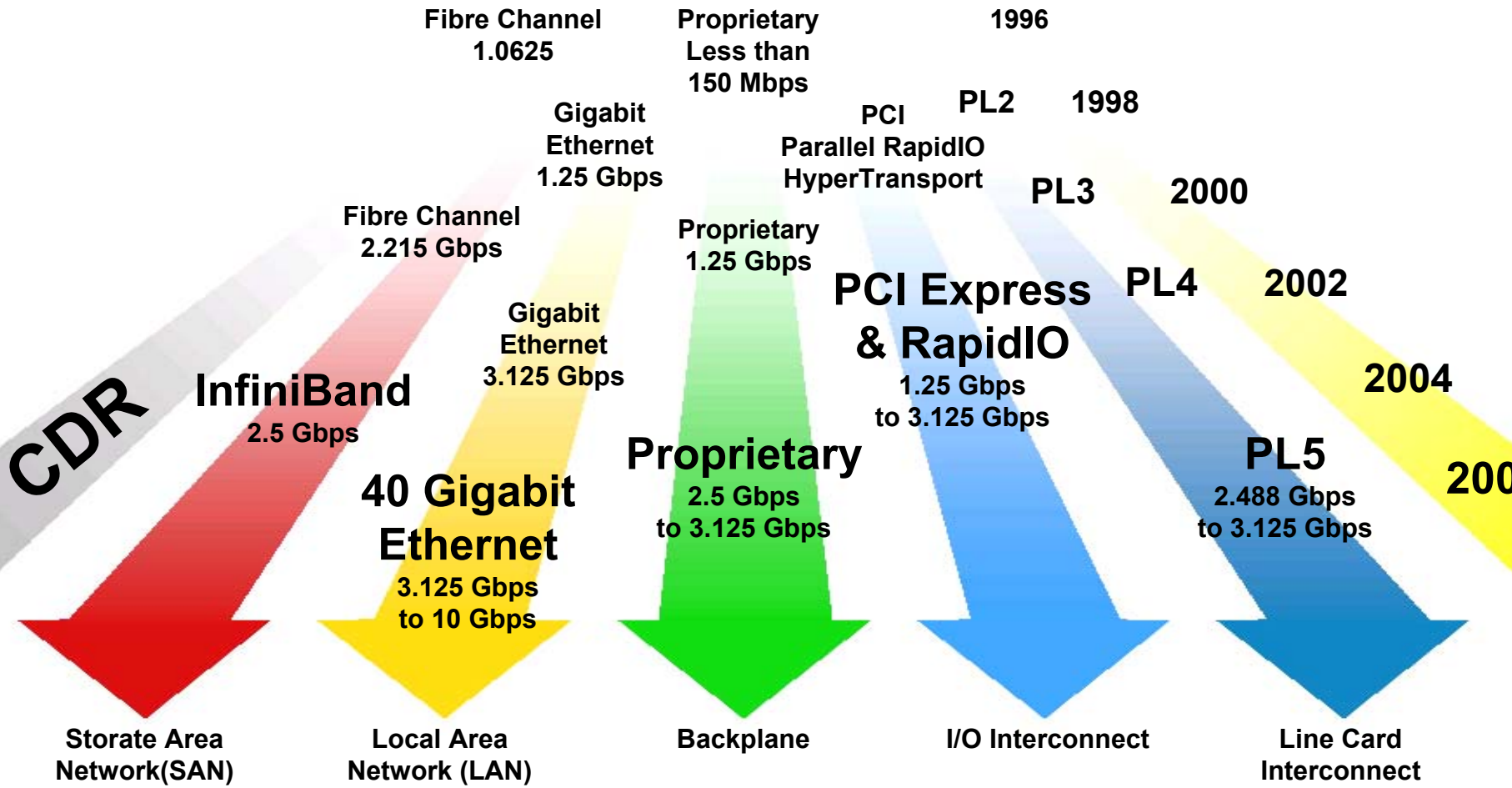
The Cyclone Device Family

Device	Logic Elements	PLLs	Embedded Memory Bits	Maximum User I/O	Maximum LVDS Channels	Price *(1)*
EP1C3	2,910	1	60 K	104	34	$4.00
EP1C6	5,980	2	92 K	185	72	$8.95
EP1C12	12,060	2	240 K	249	103	$20.00
EP1C20	20,060	2	300 K	301	129	$40.00

(1) Price Based on 250K units in 2004

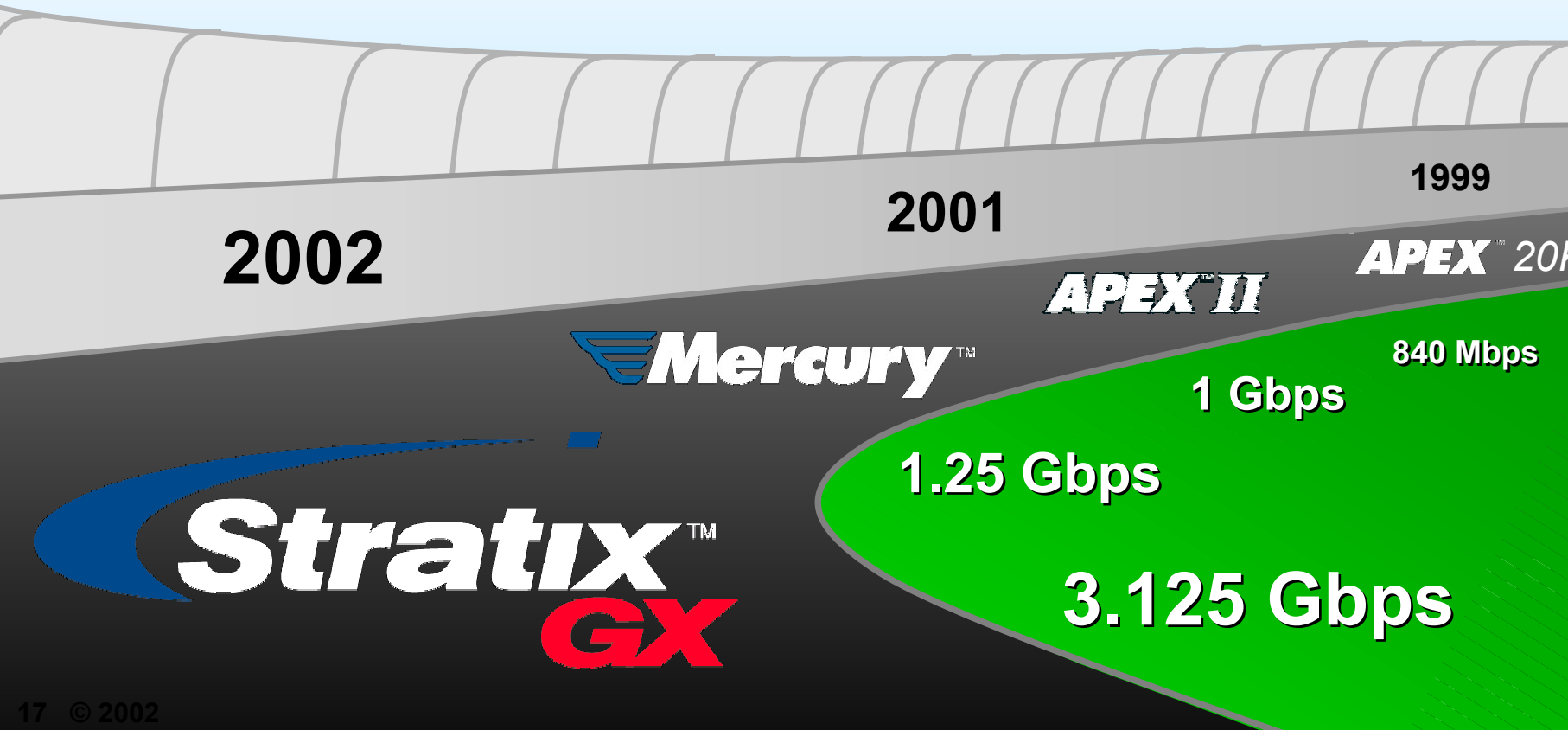
Samples Available in January 2003

Bandwidth Demand Growth



Building on Experience

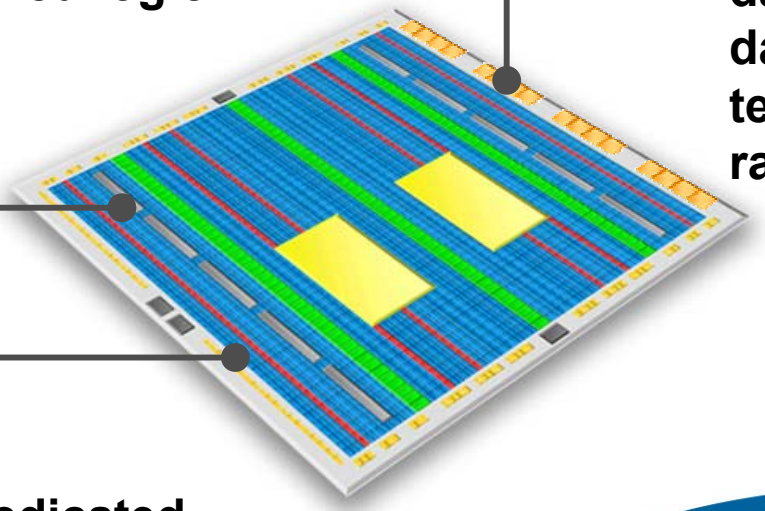
- Industry Leadership in High-Speed I/O Innovation & Expertise



Matching Transceiver & FPGA Bandwidth

Stratix™ (străt′ĭks) n. The industry's fastest FPGA device family offering unrivaled logic & memory resources

Transceiver (trăn-se′vər) n. Clock data recovery-based data transmission technology supporting rates up to 3.125 Gbps



DPA (dē′pē ā) n. Dedicated circuitry for resolving clock-to-channel and channel-to-channel skew, only found in Stratix GX devices

Stratix™ GX

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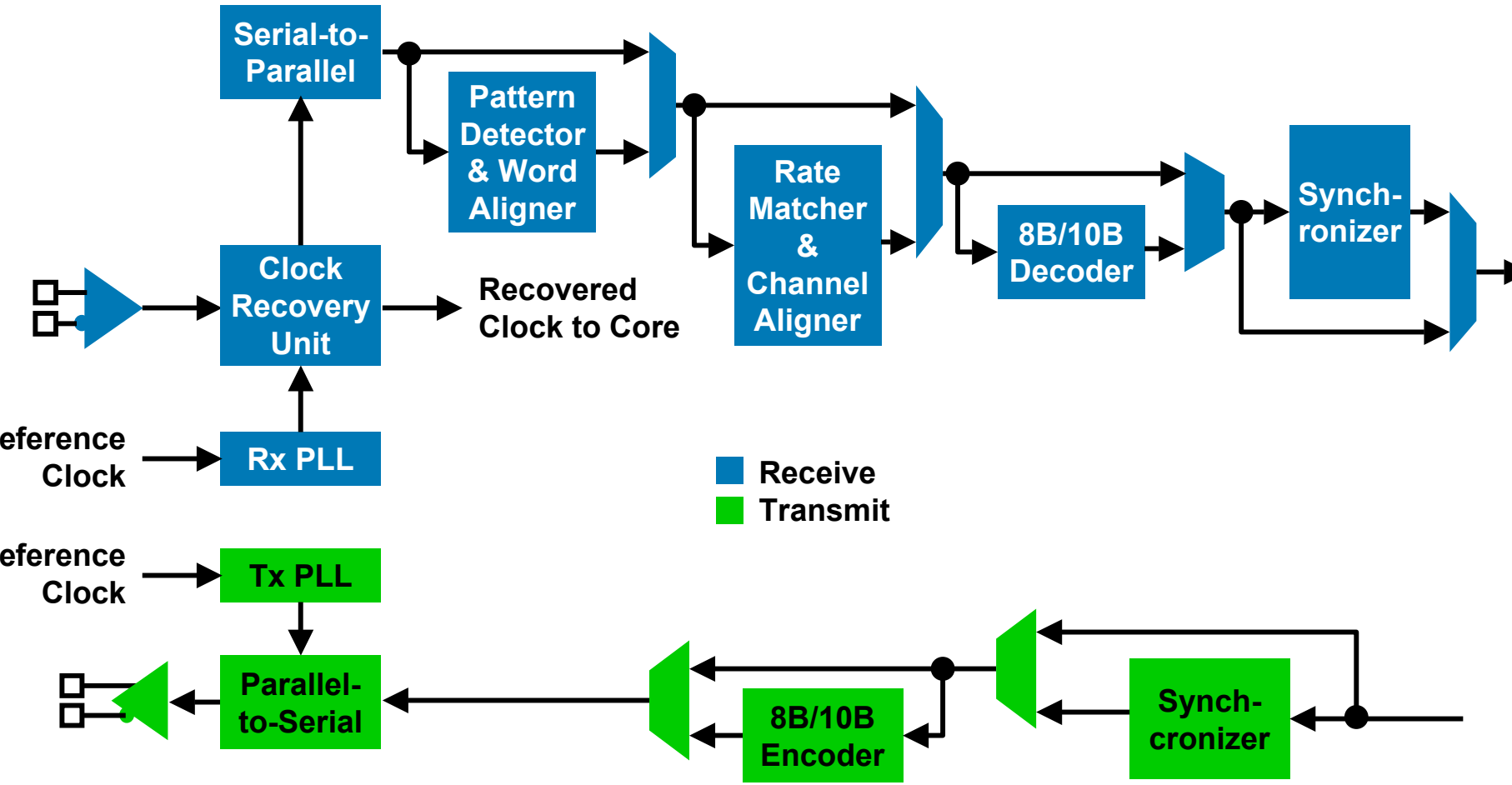
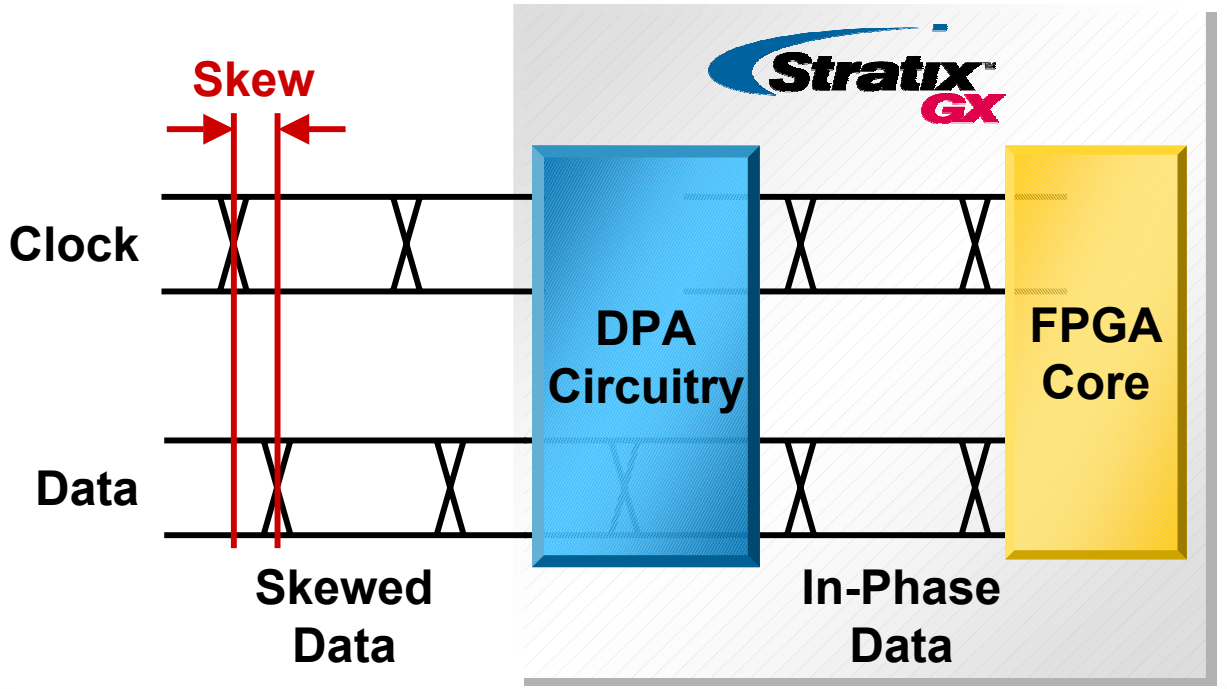
Stratix GX Transceiver Channel

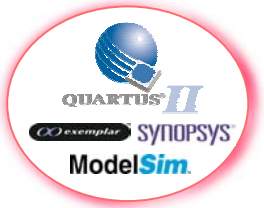


Dynamic Phase Alignment

- Real-Time Resolution of Channel-to-Channel & Clock-to-Channel Skew
- HyperTransport, 10G Ethernet XSBI, SPI-4.2, SFI-4, Parallel RapidIO & CSIX Streaming



Risk Reduction Throughout The Design Process



- PCB Guidelines
- Design Services
- Board Simulation

Product Delivery

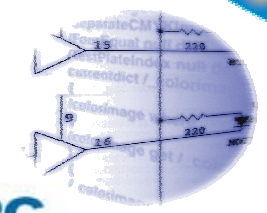
- Synthesis
- Place & Route
- Simulation

- IP Portfolio

Stratix™ GX

- Demo Kits
- Documentation

Product Concept



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The Stratix GX Device Family

Device	Logic Elements	Full-Duplex Transceiver Channels	Source-Synchronous Channels	M512 Blocks	M4K Blocks	M-RAM Blocks	DSP Blocks
EP1SGX10C	10,570	4	22	94	60	1	6
EP1SGX10D	10,570	8	22	94	60	1	6
EP1SGX25C	25,660	4	39	224	138	2	10
EP1SGX25D	25,660	8	39	224	138	2	10
EP1SGX25F	25,660	16	39	224	138	2	10
EP1SGX40D	41,250	8	45	384	183	4	14
EP1SGX40G	41,250	20	45	384	183	4	14

Supported in Quartus® II 2.1 Today!

CPLDs : Non Volatile, Instant On

MAX® 7000

- High-Performance Device Family
- 5.0-V, 3.3-V & 2.5-V Variations
- Feature-Rich Architecture
- PCI Compatible
- Industrial Temperature Grades

MAX® 3000

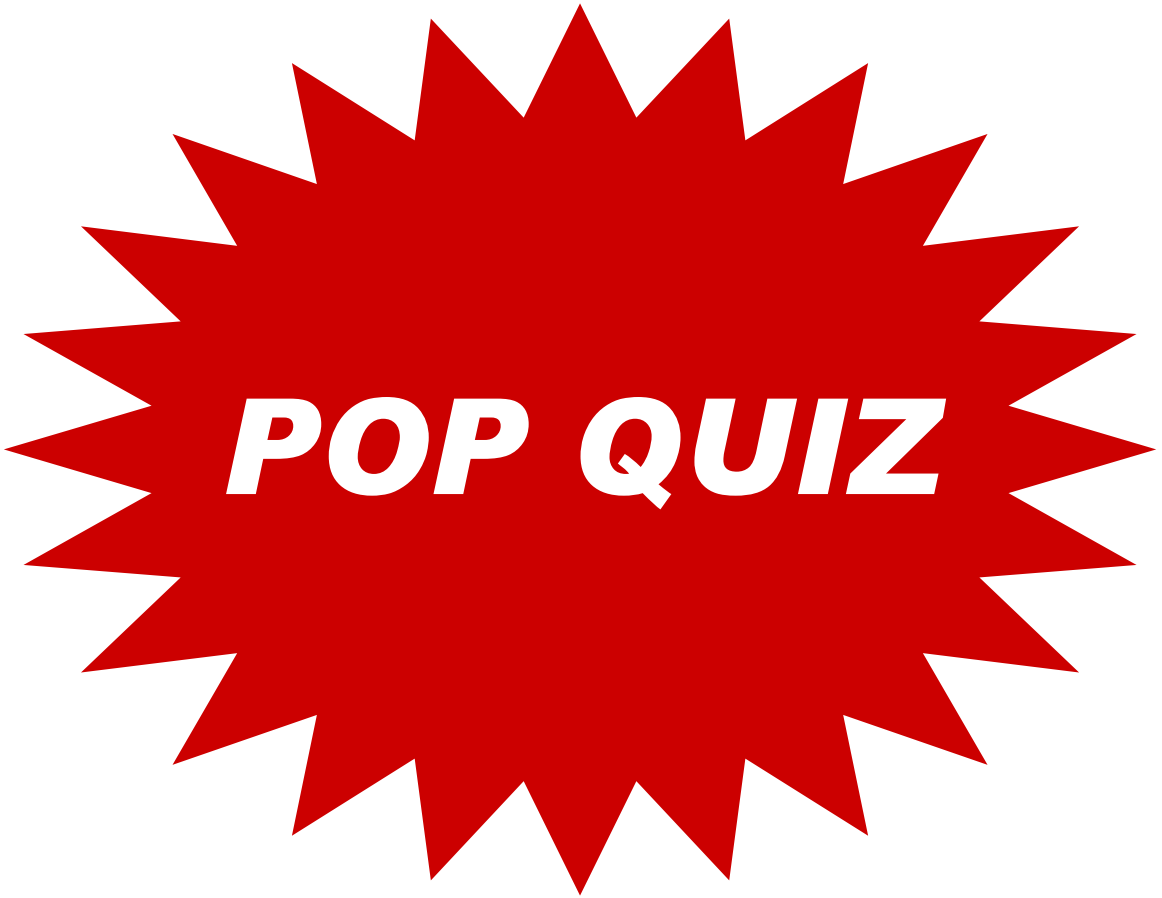
- Cost-Optimized Architecture
- Targeted Feature Set for Volume-Driven Applications
- PCI Compatible
- Low-Cost Package Options

MAX 7000 & MAX 3000 Device Overview

	MAX 3000A					MAX 7000A				
Parameter	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Useable Gates	600	1,250	2,500	5,000	10,000	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512	32	64	128	256	512
Maximum User I/O Pins	36	68	100	164	208	36	68	100	164	208
t_{PD} (ns)	4.5	4.5	5.0	7.5	7.5	4.5	4.5	5.0	5.5	7.5
f_{CNT} (MHz)	227	222	192	172	116	192	192	178	164	119
t_{SU} (ns)	2.9	2.8	3.3	3.9	5.6	2.5	2.5	2.5	2.5	3.0
t_{CO1} (ns)	3.0	3.1	3.4	3.5	4.7	2.8	2.8	3.0	3.2	4.5

The Right Products For SOPC Solutions

- Intense Focus on End Market Applications
  - Customer-Oriented Product Planning Process
- Useable Products with the Right Features
  - Fulfill Critical Design Requirements
    - Price
    - Performance
    - Capabilities


POP QUIZ

Quiz Question

다음 중 Stratix가 가진 기능이 아닌것은 ?

A) Tri-Matrix Memory
B) Embedded DSP Block
C) Terminator Technology
D) Embedded H/W Processor

TIME'S UP!

Quiz Answer

다음 중 Stratix가 가진 기능이 아닌것은 ?

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D) Embedded H/W Processor