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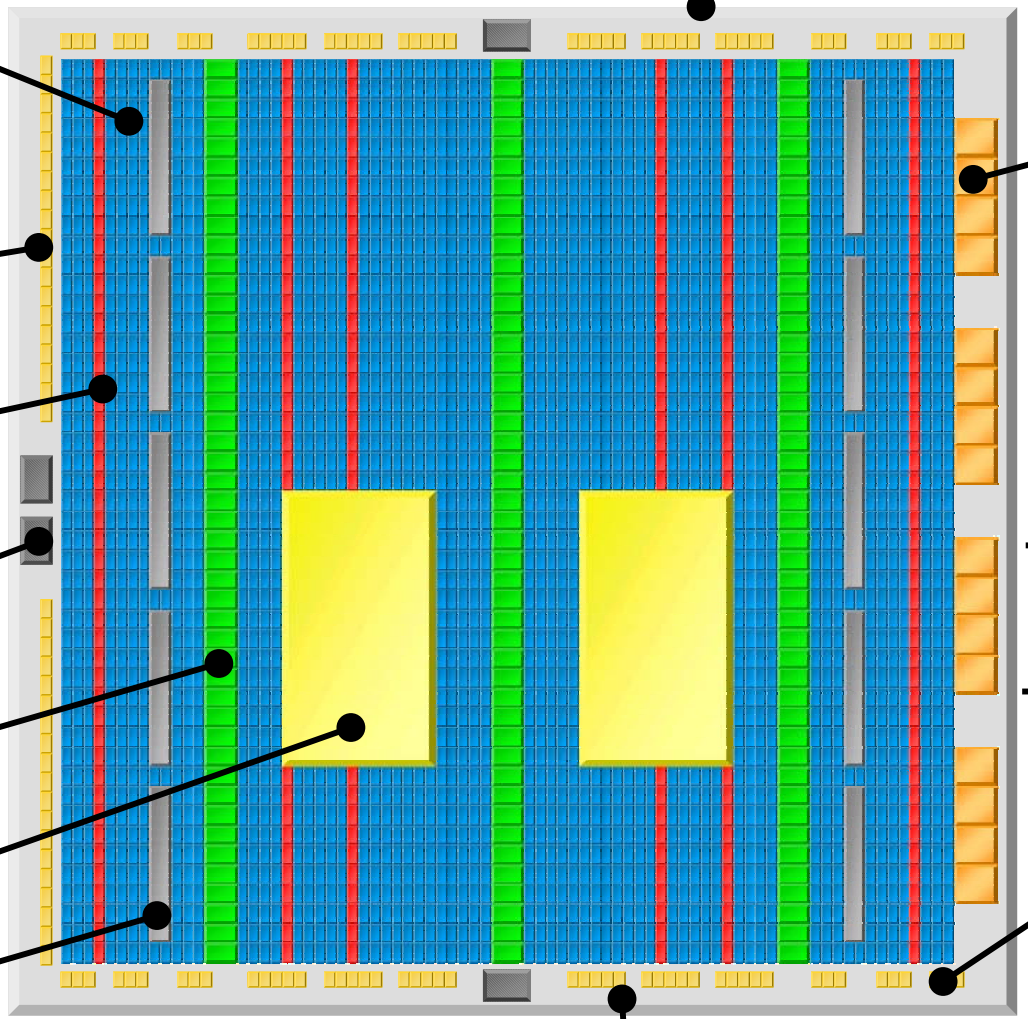
Implementing Switch Fabrics in FPGAs

ALTERA.

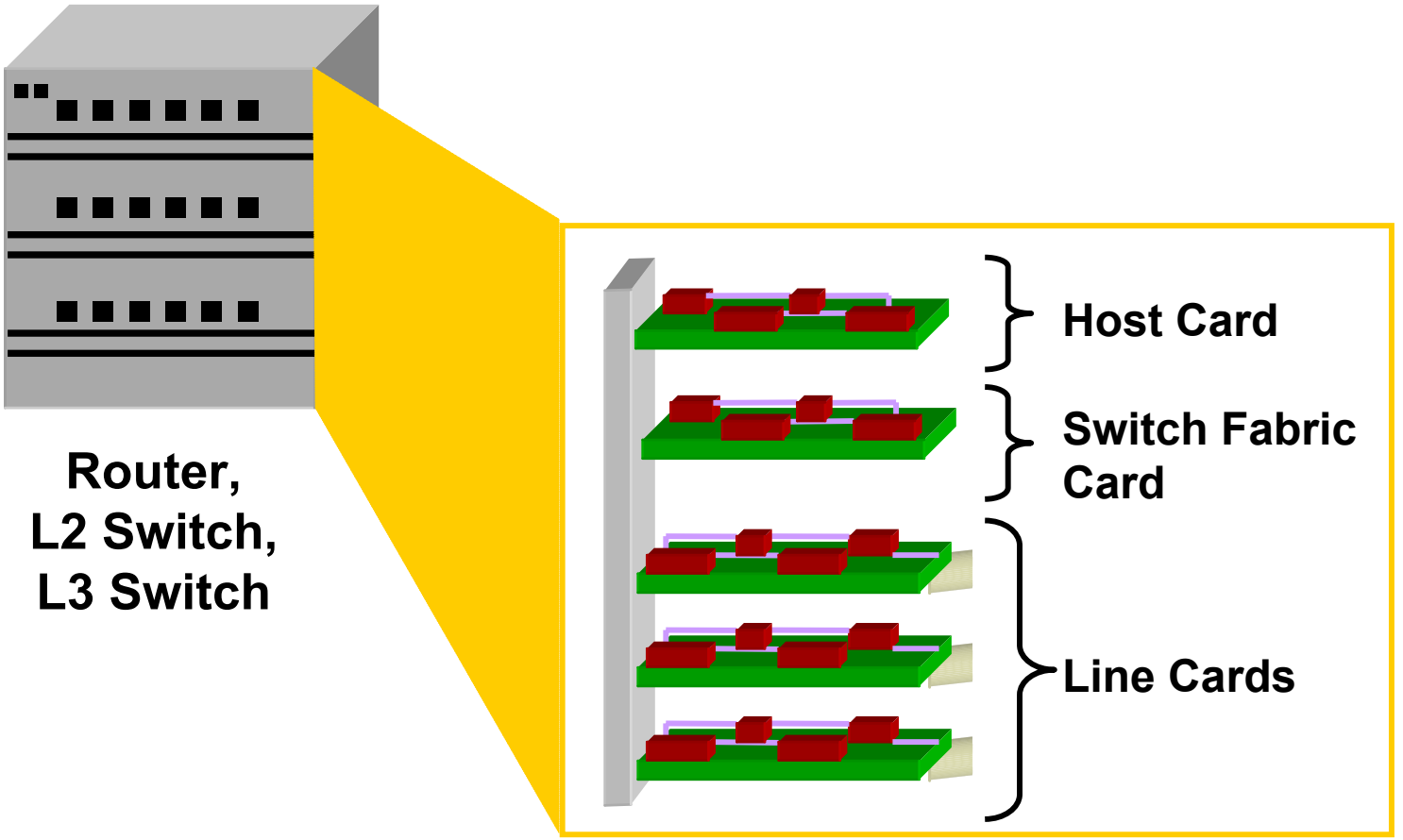
Agenda

- Stratix GX Introduction
- System Overview
- Centralized Switch Fabrics
- Distributed Switch Fabrics
- Summary

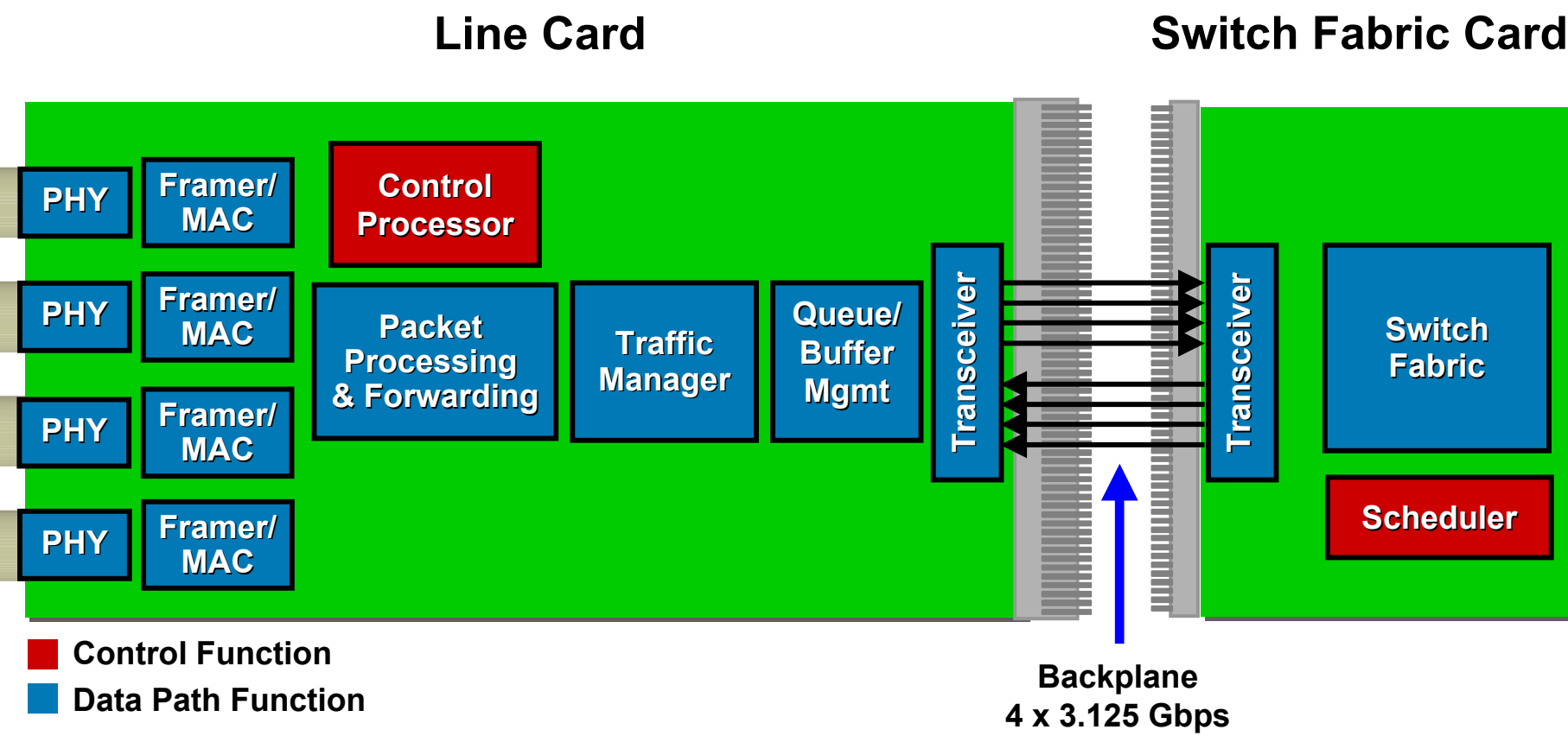
Stratix GX Introduction



Typical Networking Equipment

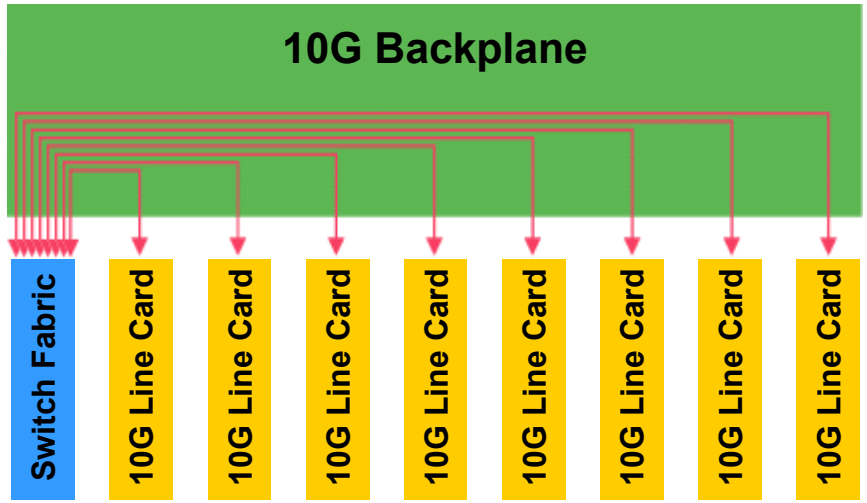


Typical Data Flow

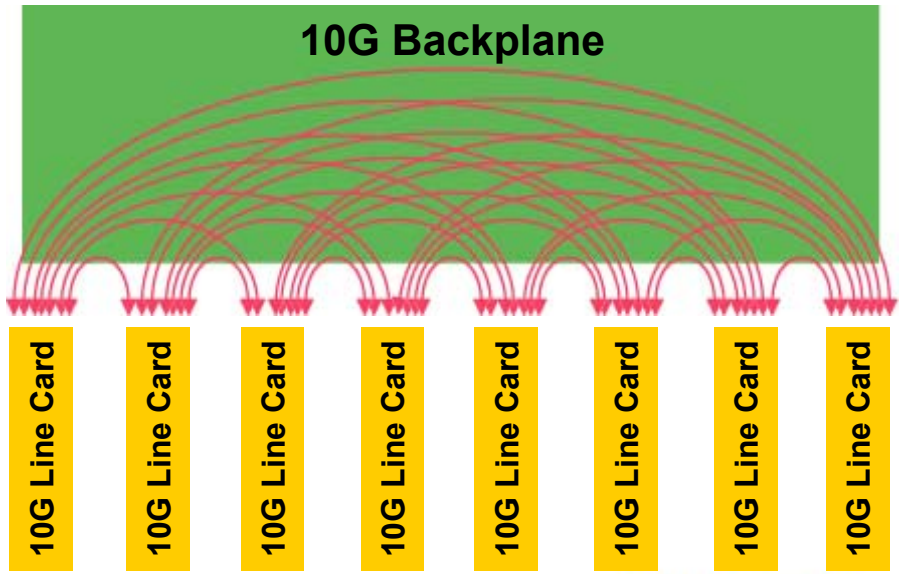


Backplane Architectures

- Centralized Switch Fabrics
  - **Each Line Card Connects to Switch Fabric Card**
  - **Switch Fabric Card Routes Data**
  - **Redundant Switch Fabric Cards Needed**



- Distributed Switch Fabrics
  - **Each Line Card Connects to Every Other Line Card**
  - **Switch Module on Each Line Card Routes Data**
  - **No Need for Redundancy**



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Centralized Switch Fabrics

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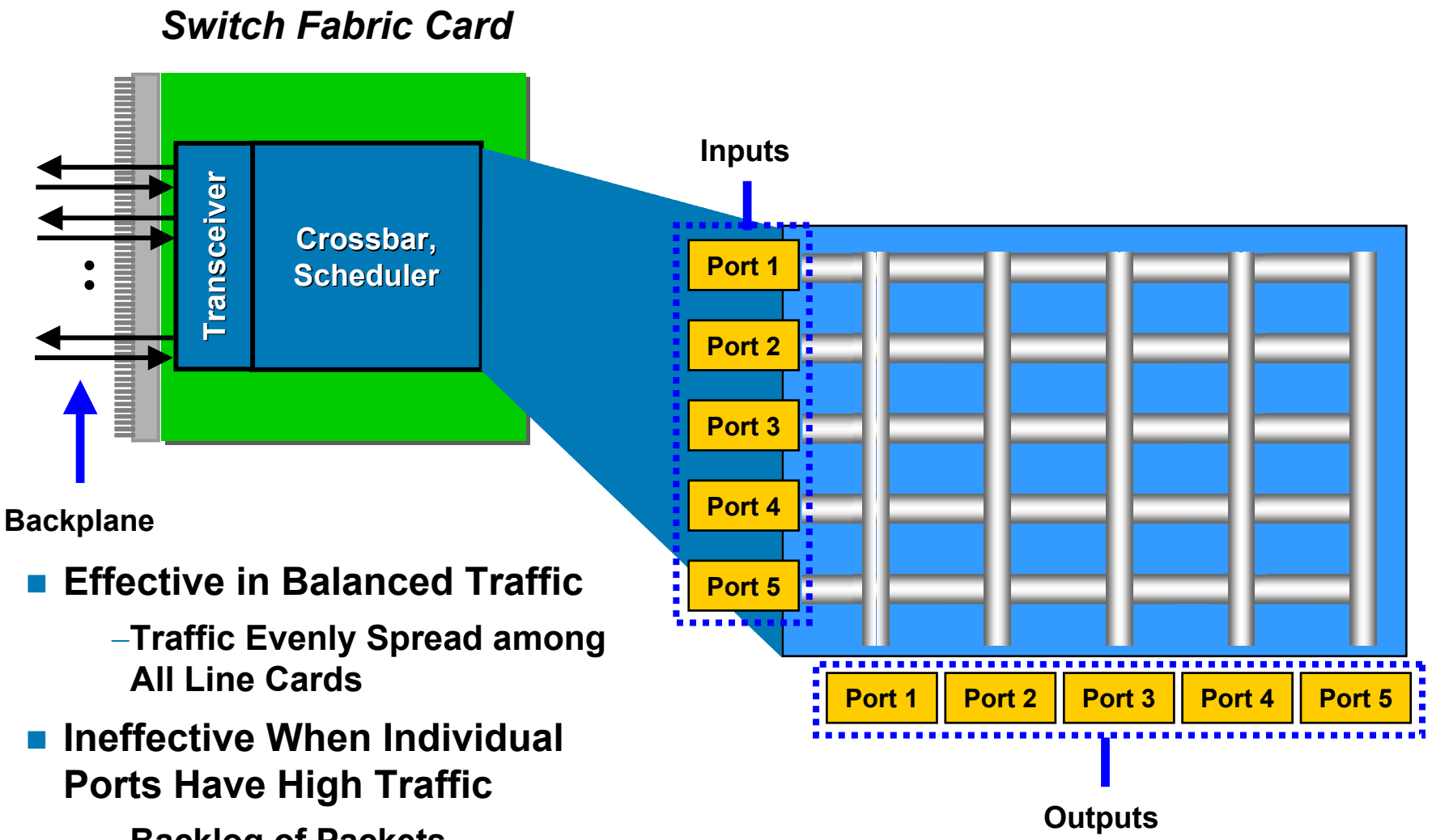
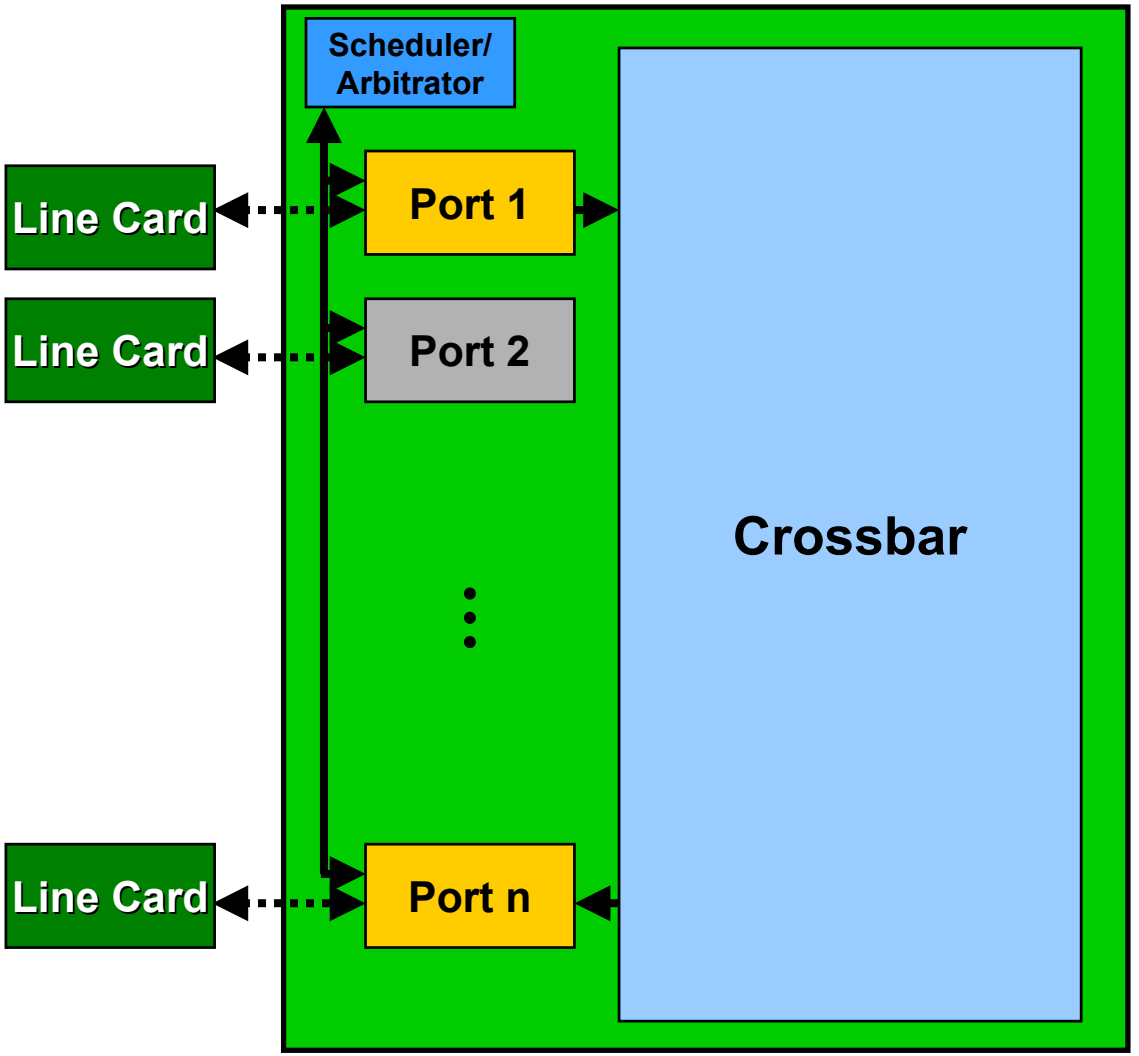
Centralized: Crossbar Fabrics

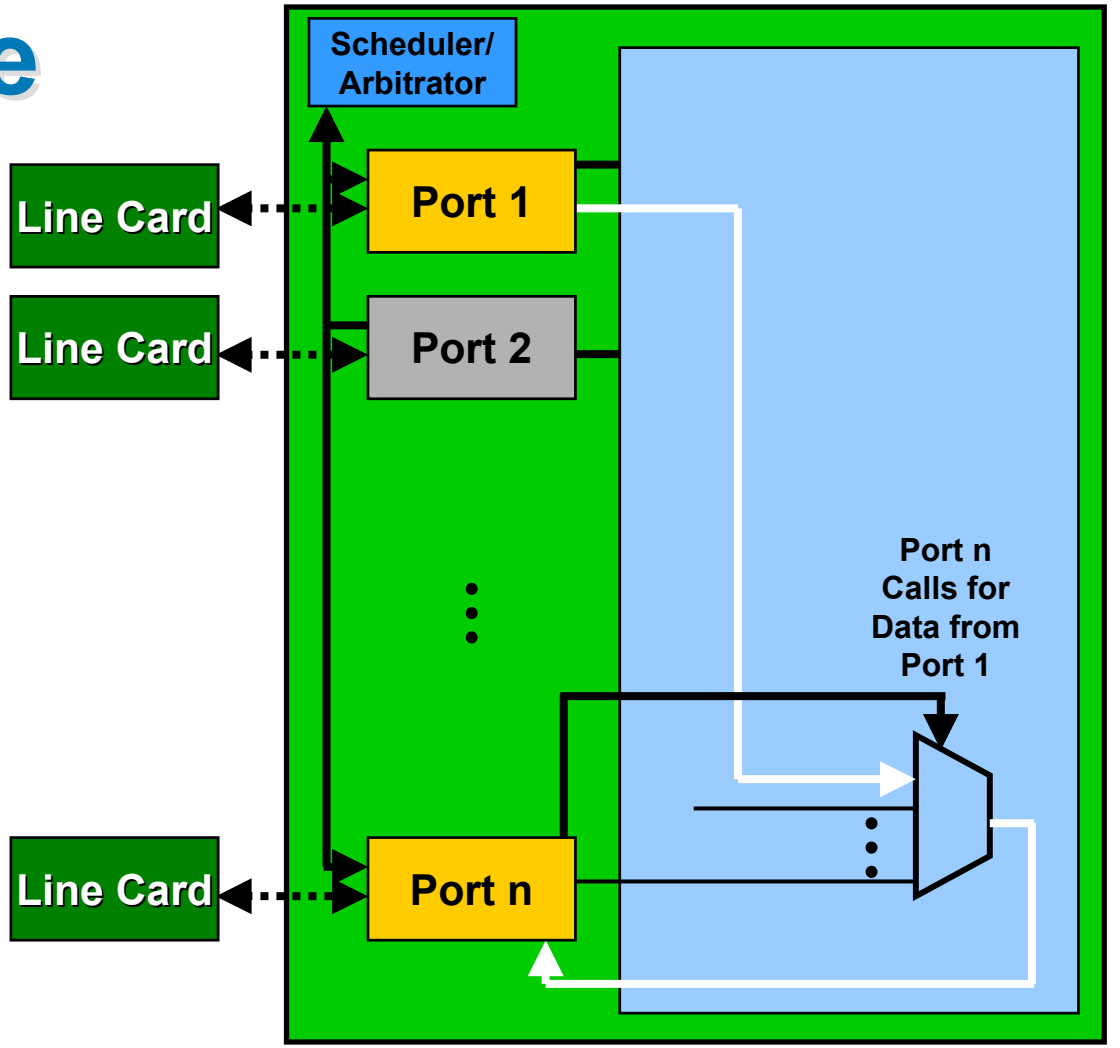


- Effective in Balanced Traffic
  - Traffic Evenly Spread among All Line Cards
- Ineffective When Individual Ports Have High Traffic
  - Backlog of Packets

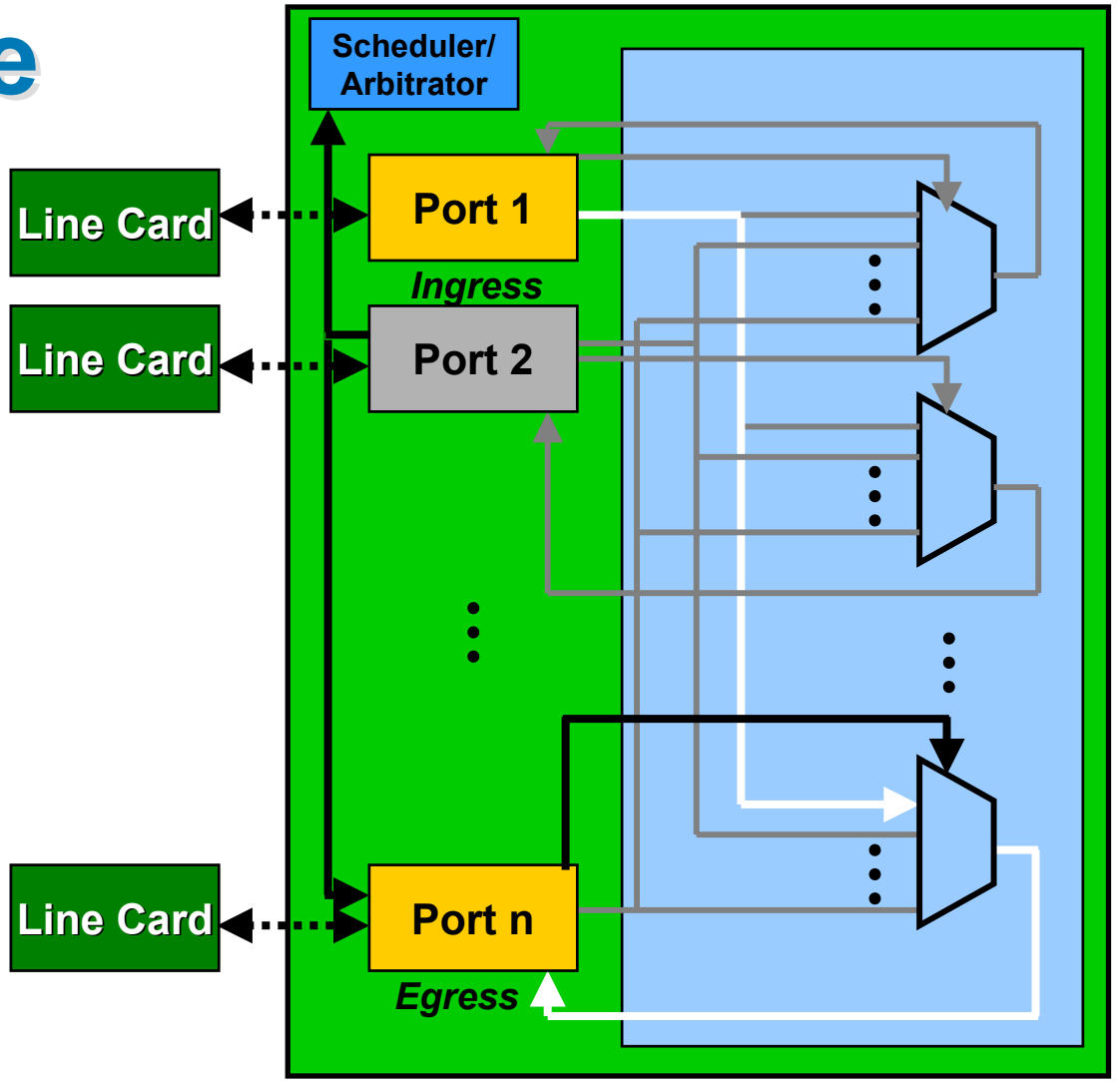
Crossbar Function



Crossbar Function – Reverse Route

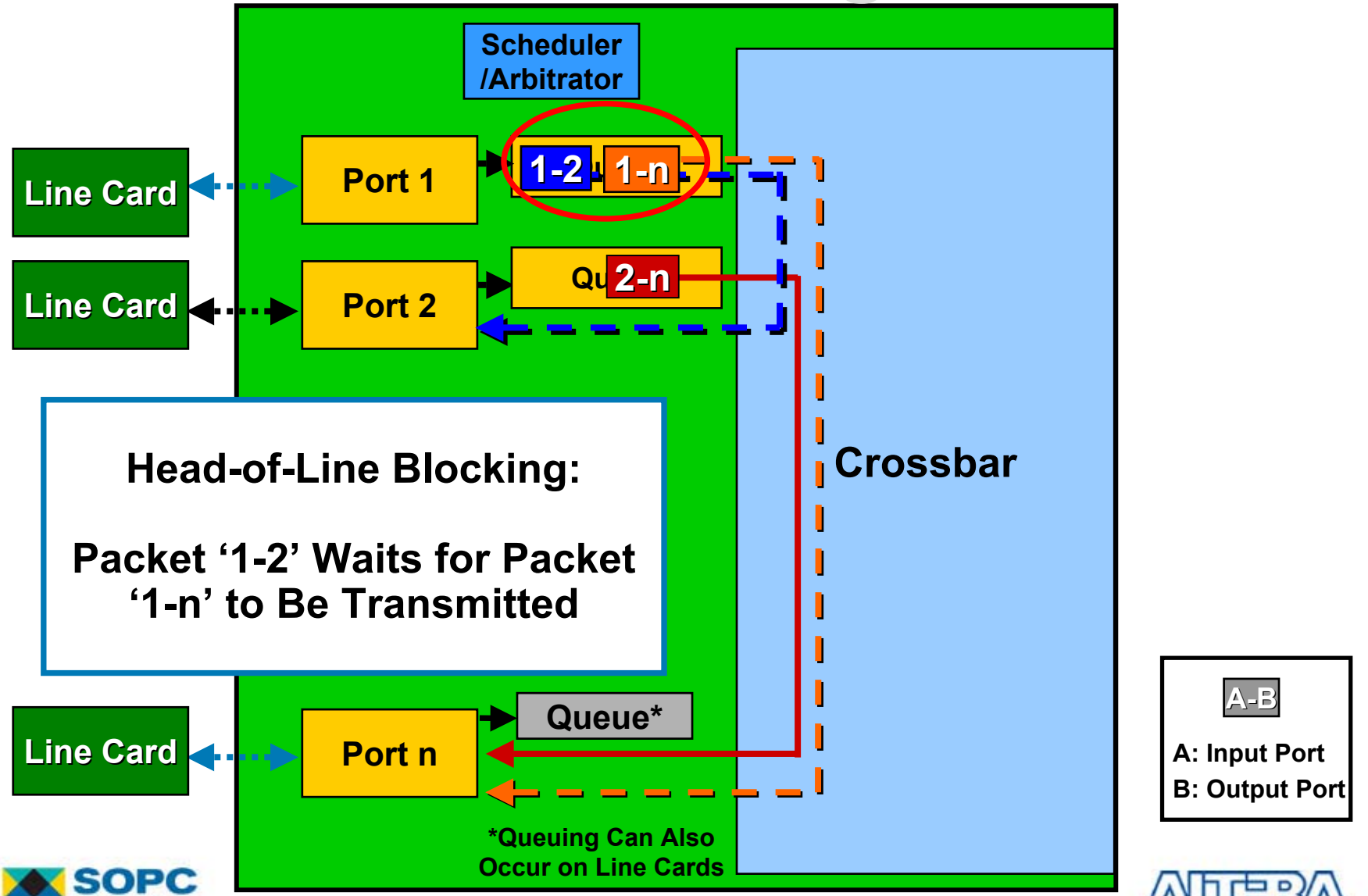


Crossbar Function – Reverse Route

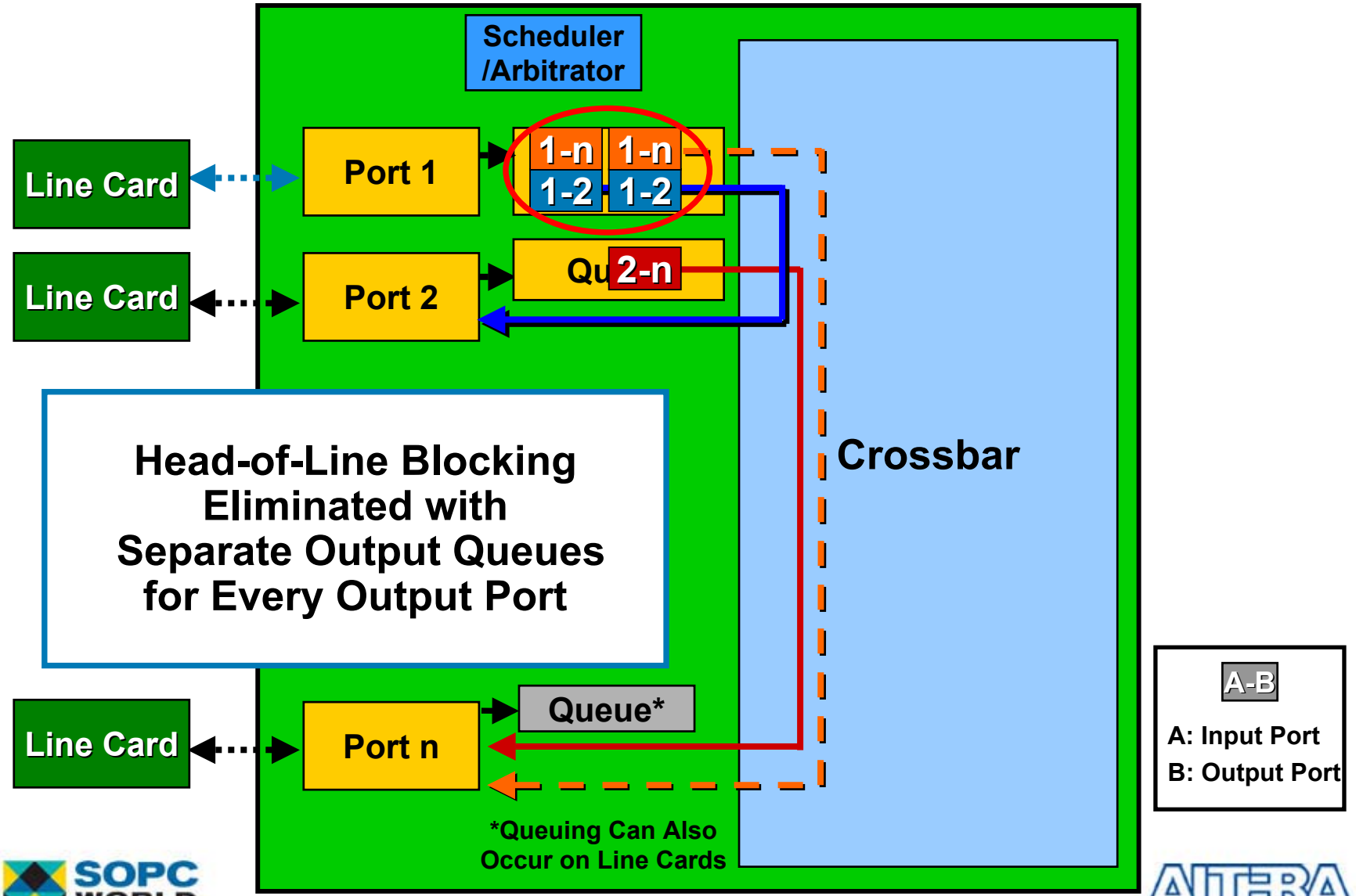


MUX Structure Repeated for All Ports

Head-of-Line Blocking Problem

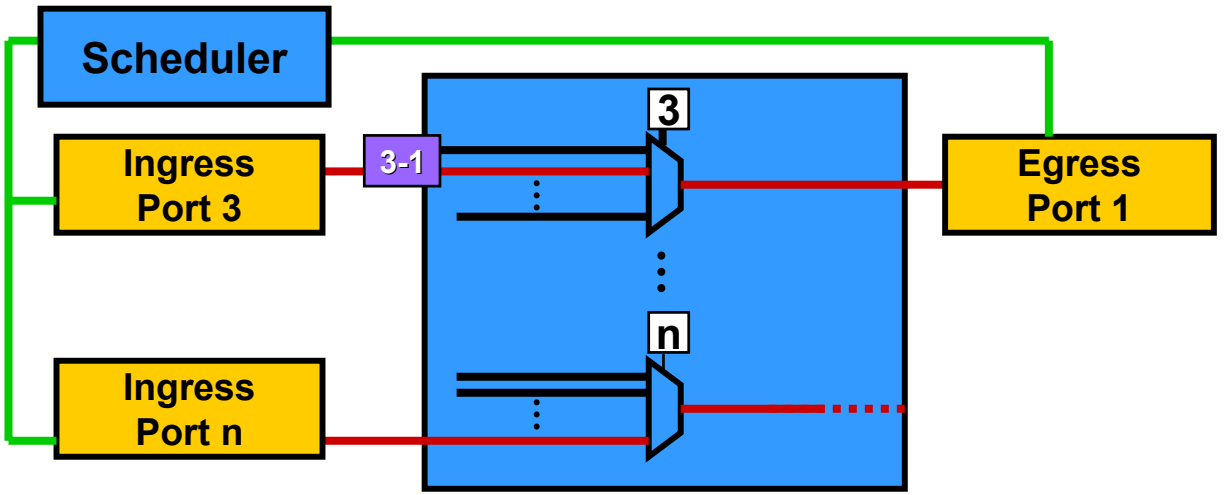


Virtual Output Queuing (VOQ)



Switch Fabric Scheduling Methods

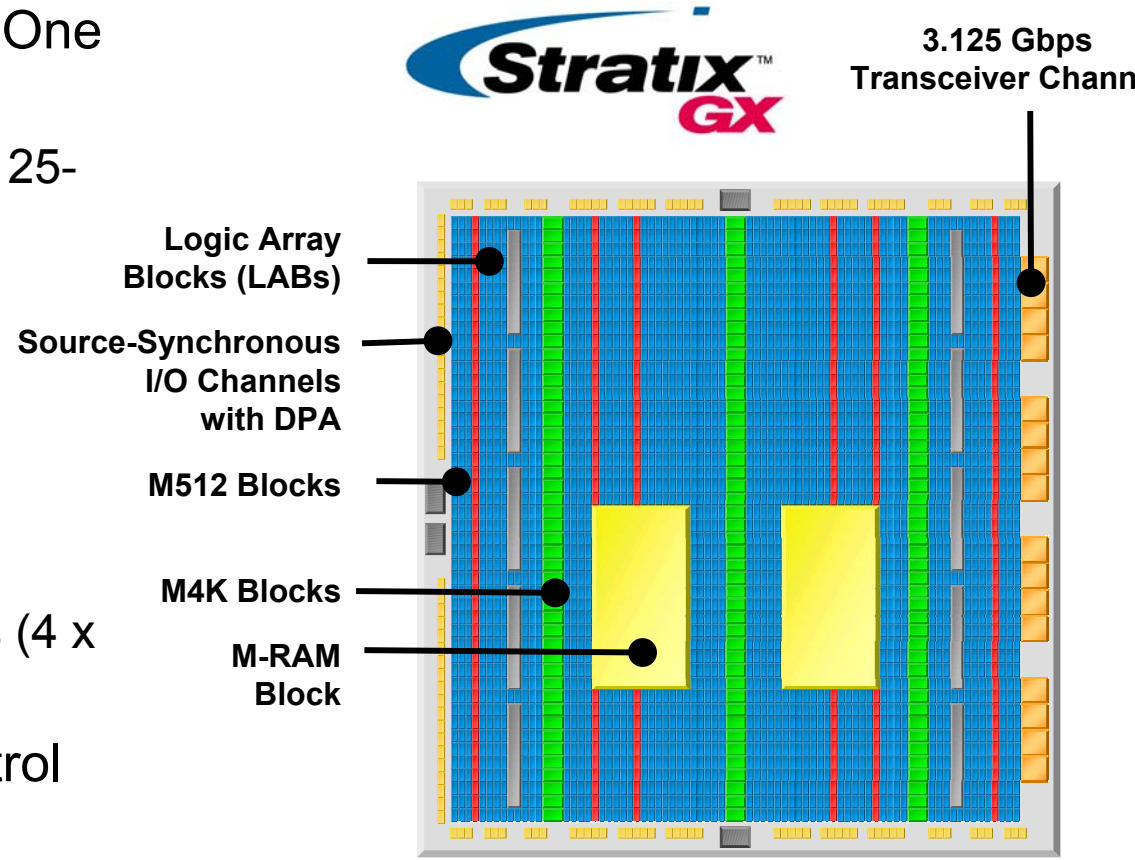
- Switch Fabric Operates on Time Slots
- Switch Fabric Must Be “Configured” During Each Time Slot



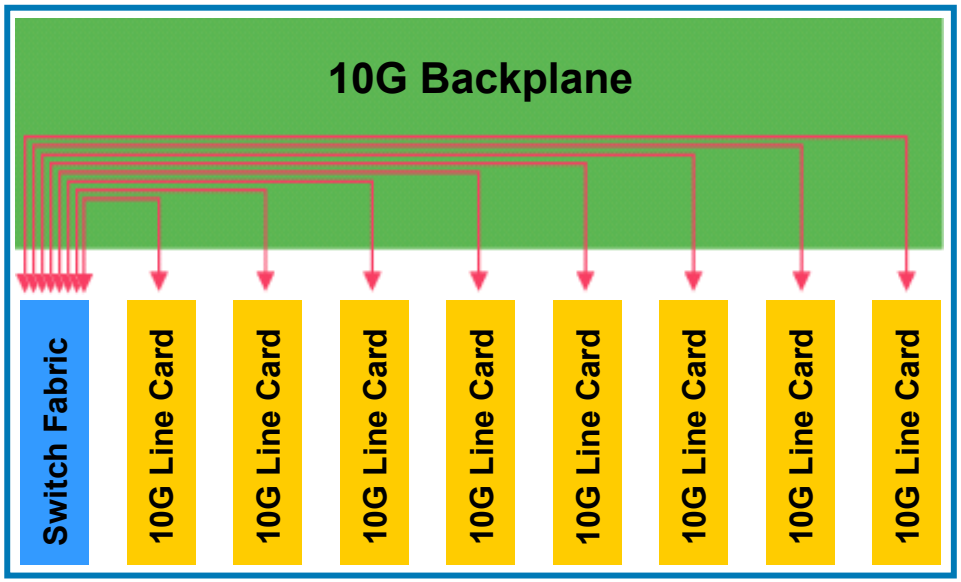
- Methods of Scheduling Packets/Cells for Switch Fabrics
  - SLIP, Islip, Parallel Iterative Matching (PIM) , Least Recently Used (LRU)

Stratix GX Devices for Crossbars

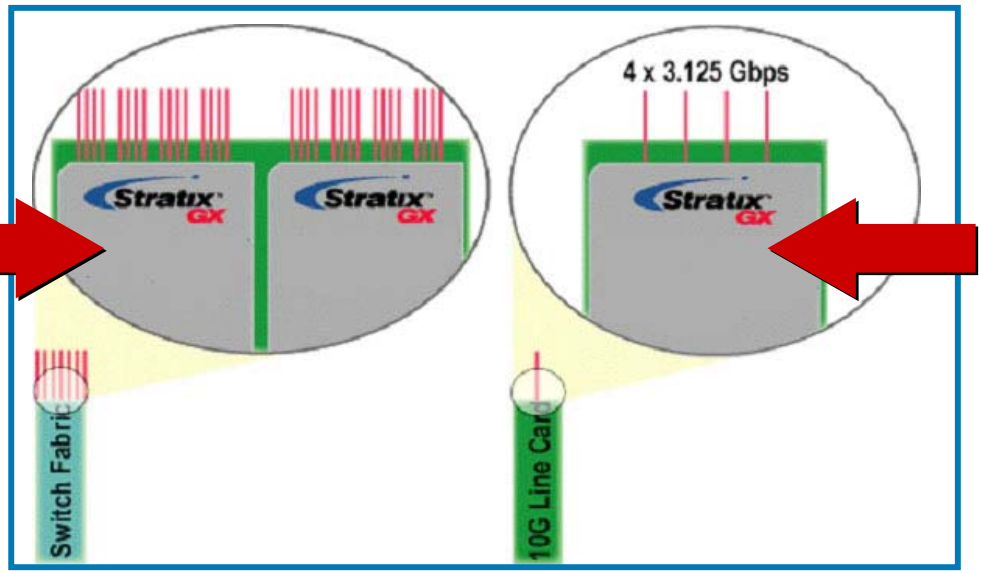
- Supports Many Links in One Device
  - Up to 20 Integrated 3.125-Gbps Transceivers
- Output Port Queuing
  - Up To 183 M4K RAM Blocks (183 x 4KBits)
- More Queuing
  - Up to 4 M-RAM Blocks (4 x 512 Kbits)
- Scheduling & Flow Control Functions
  - Over 41K Logic Elements (LEs)



Centralized Switch Fabric



- Backplane Transceiver
- Switch Fabric

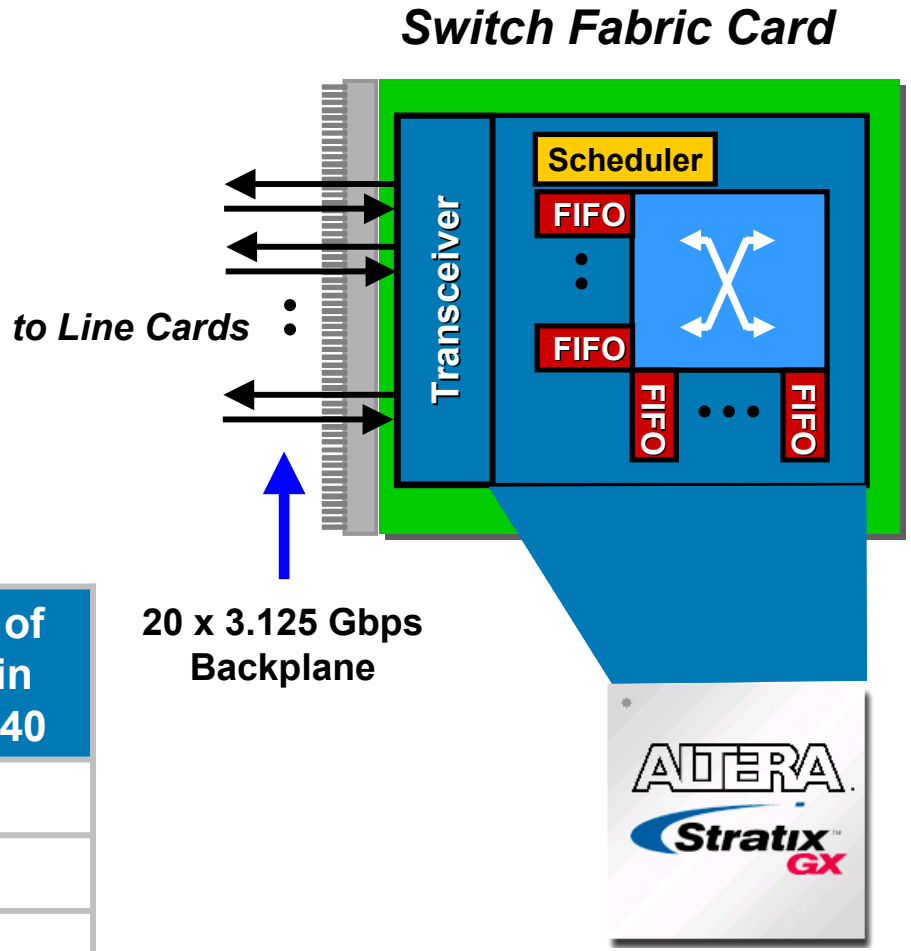


- Backplane Transceiver
- Queue/Buffer Managemer
- Traffic Management

Stratix GX Crossbar Implementation

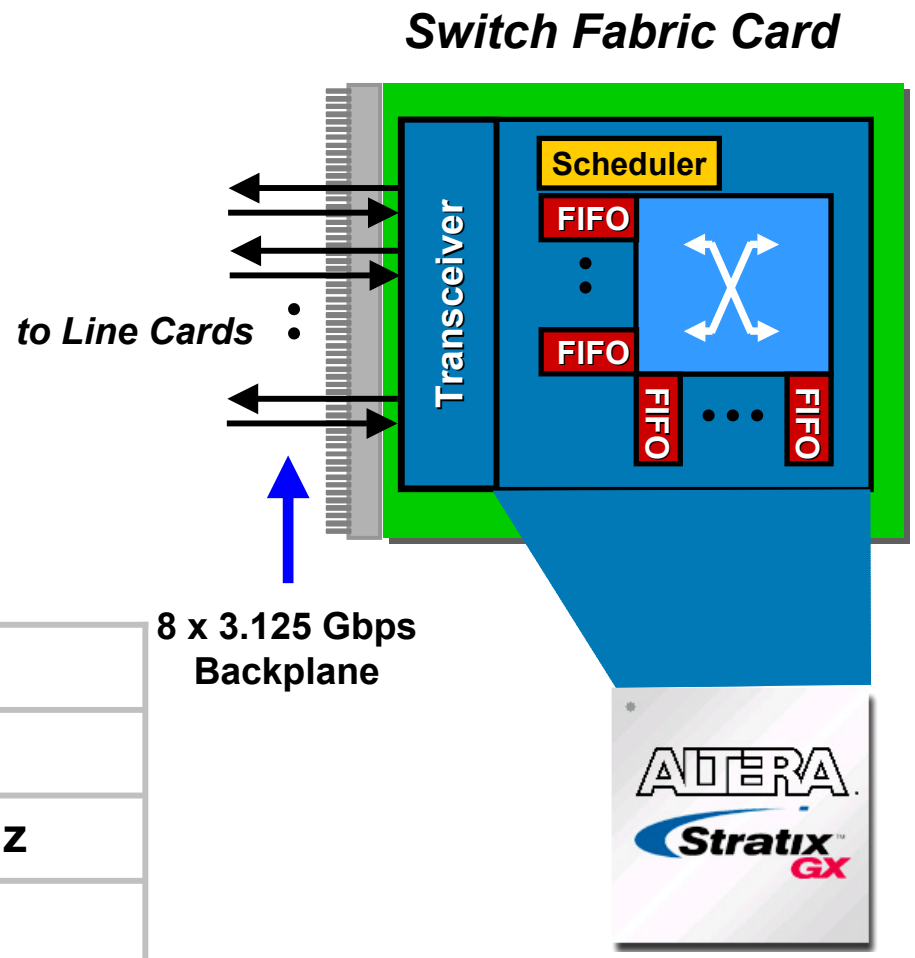
- Programmable Scheduler
  - Design to Your Traffic Pattern
- Integrated Transceiver, Crossbar & Scheduler
- Buffering Capabilities

RAM Block	Size	Number of Blocks in EP1SGX40
M512	512 Bits	384
M4K	4,096 Bits	183
M-RAM	512 KBits	4



Crossbar Sample Implementation

- 8x8 Crossbar Fabric
- Fixed Cell Size
- 16-Bit Data Path
- VOQ Depth: 8 Cells
- Output Queue Depth: 32 Cells
- Round Robin Scheduler

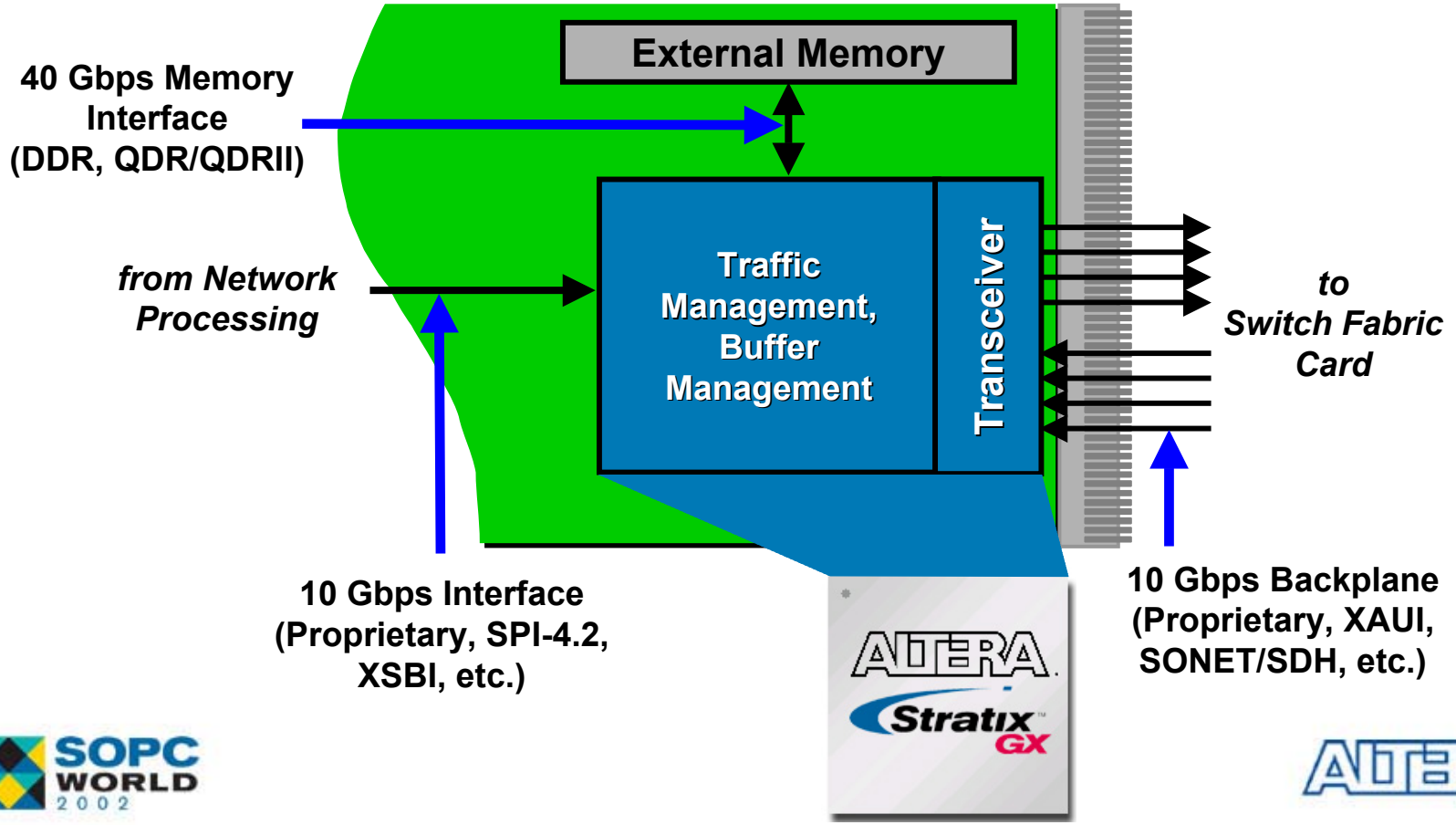


Design Results

M4K RAM Blocks	**96**
Logic Elements	**10K**
f_{MAX}	**160 MHz**
Transceiver Channels	**8**

Stratix GX Devices for Line Cards

- Programmable Traffic Manager
- Integrated Transceiver & Traffic Manager /Buffer Manager
- Superior Buffer Management Capabilities



Common Crossbar Design Needs

Needs	ASIC	Standard Part	Stratix™ GX
Customizable Scheduling, Buffering, & Fabric	✓		✓
Real-Time Design & Debug			✓
Design Updates/Corrections in Field			✓
Time-to-Market		✓	✓

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Distributed Switch Fabrics

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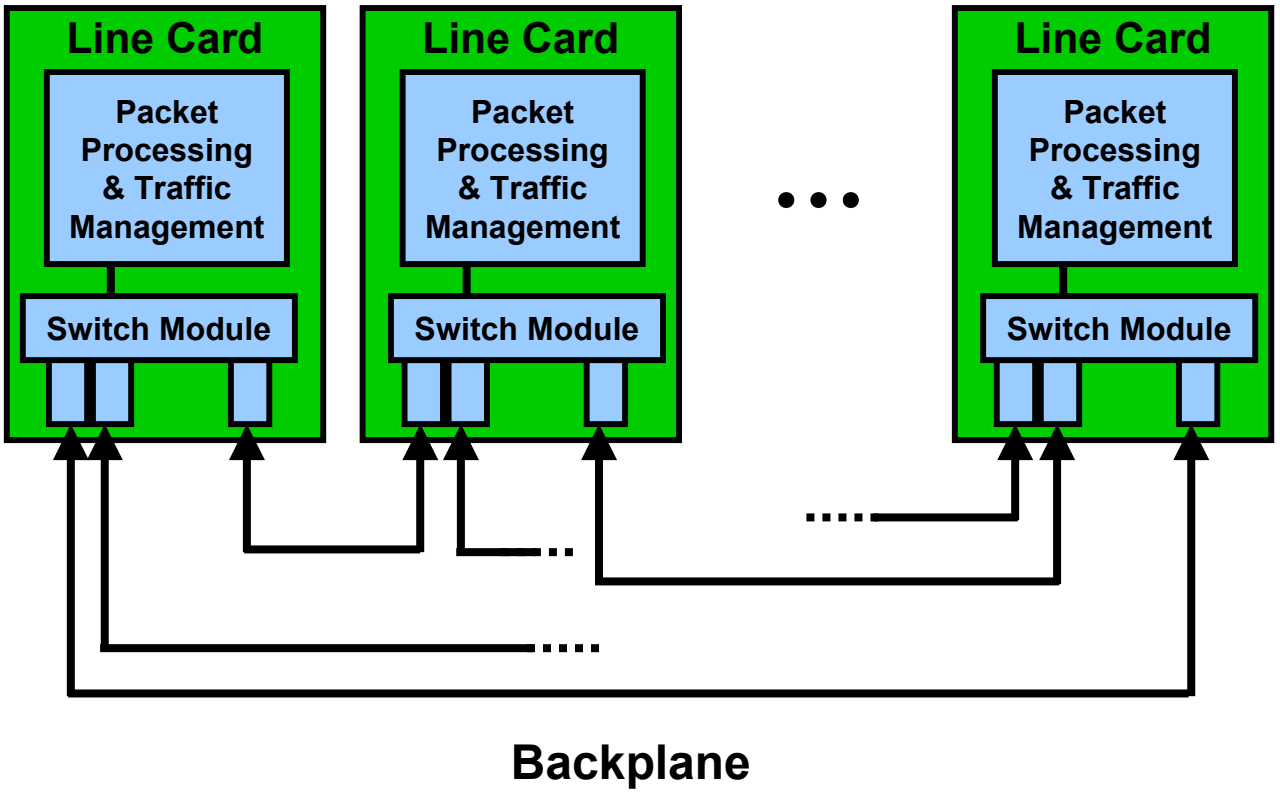
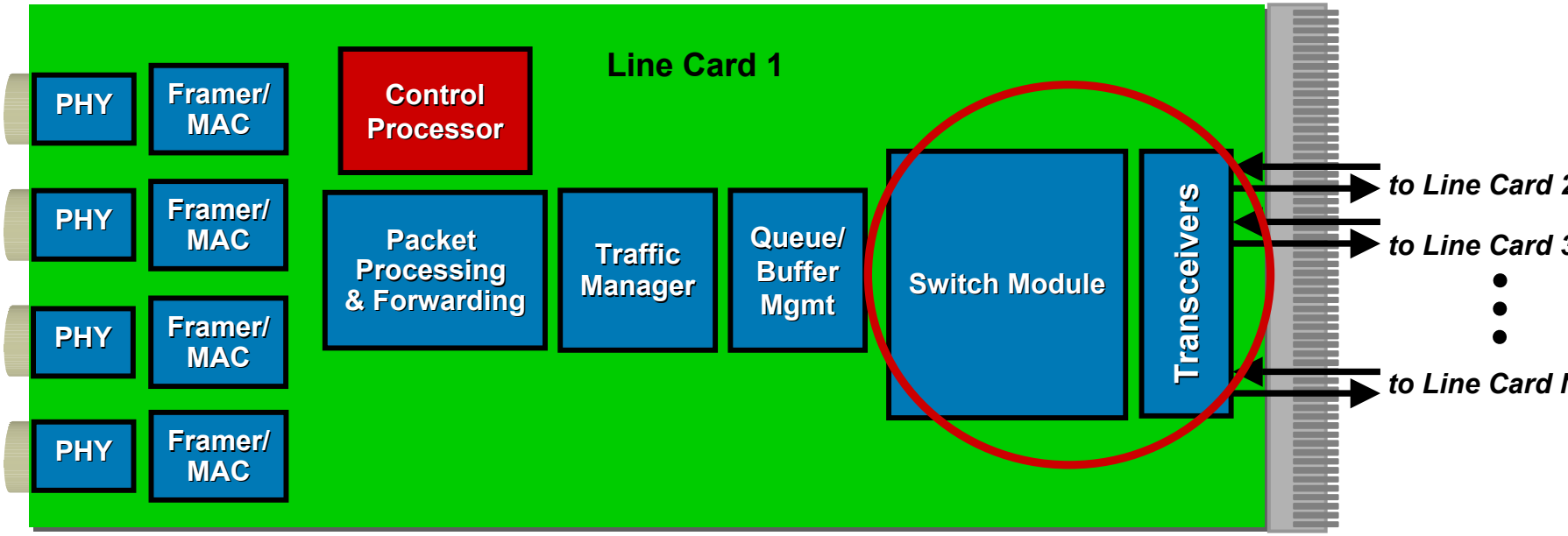
Distributed Switch Fabric

- Every Line Card Connects to Every Other Line Card via High-Speed Serial Links



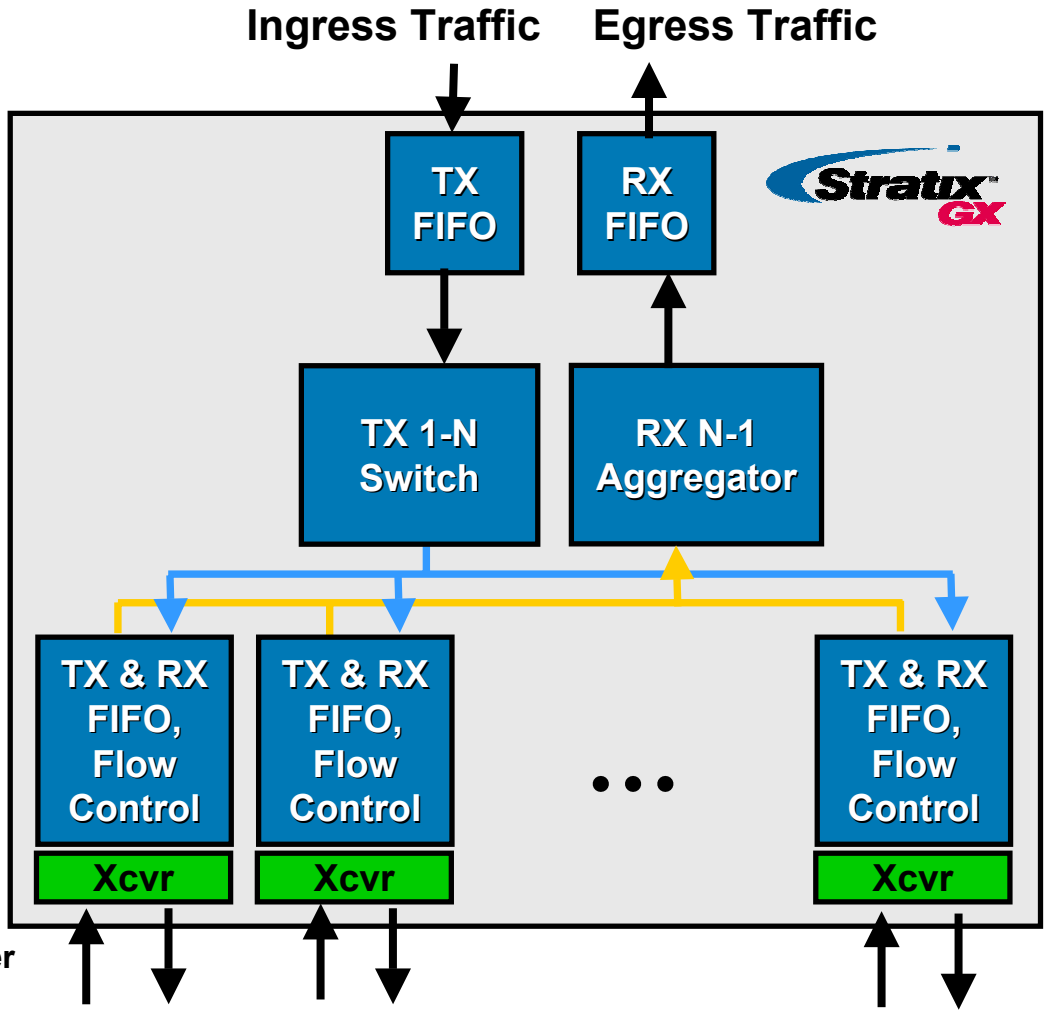
Typical Data Flow



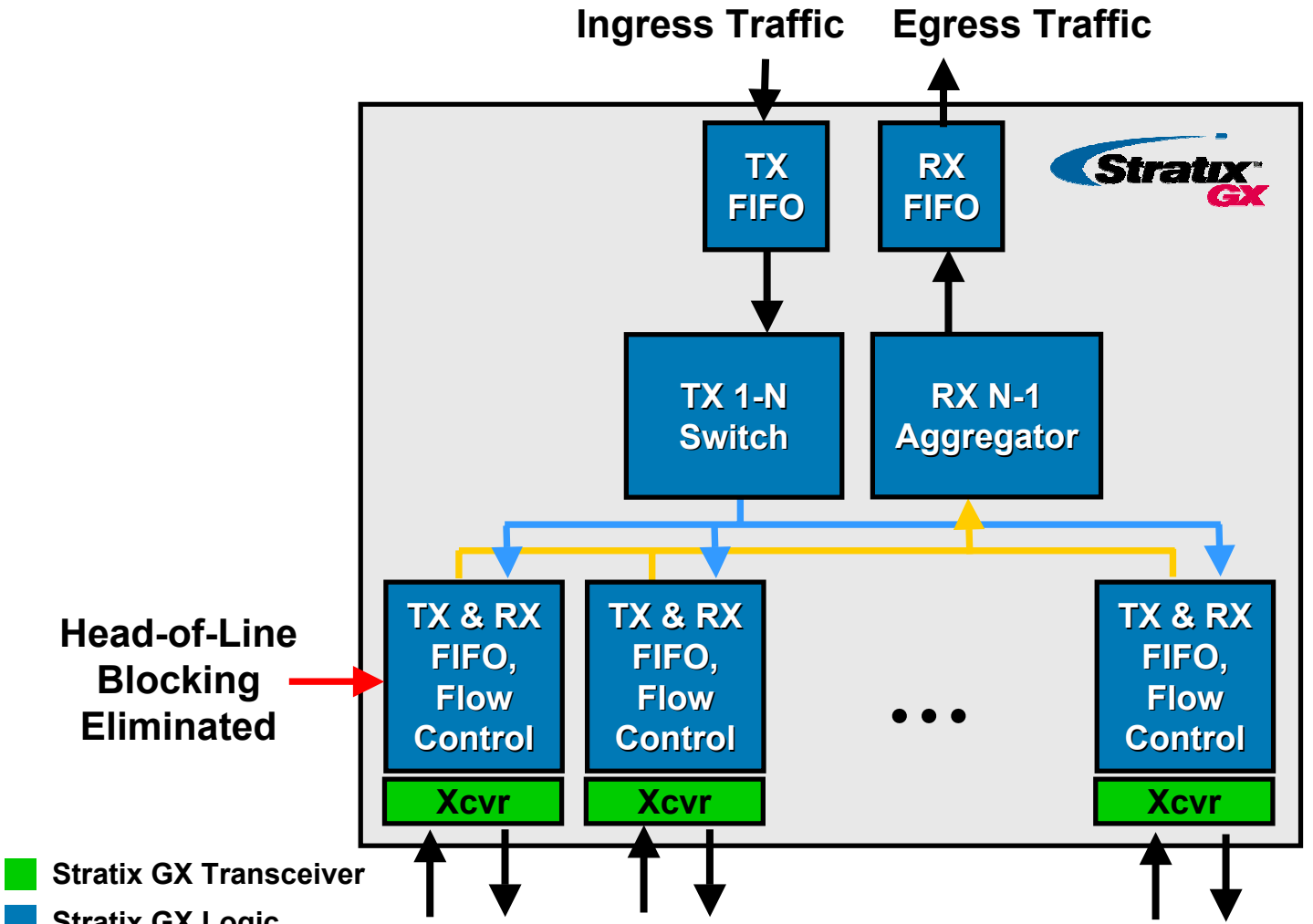
Control Function

Data Path Function

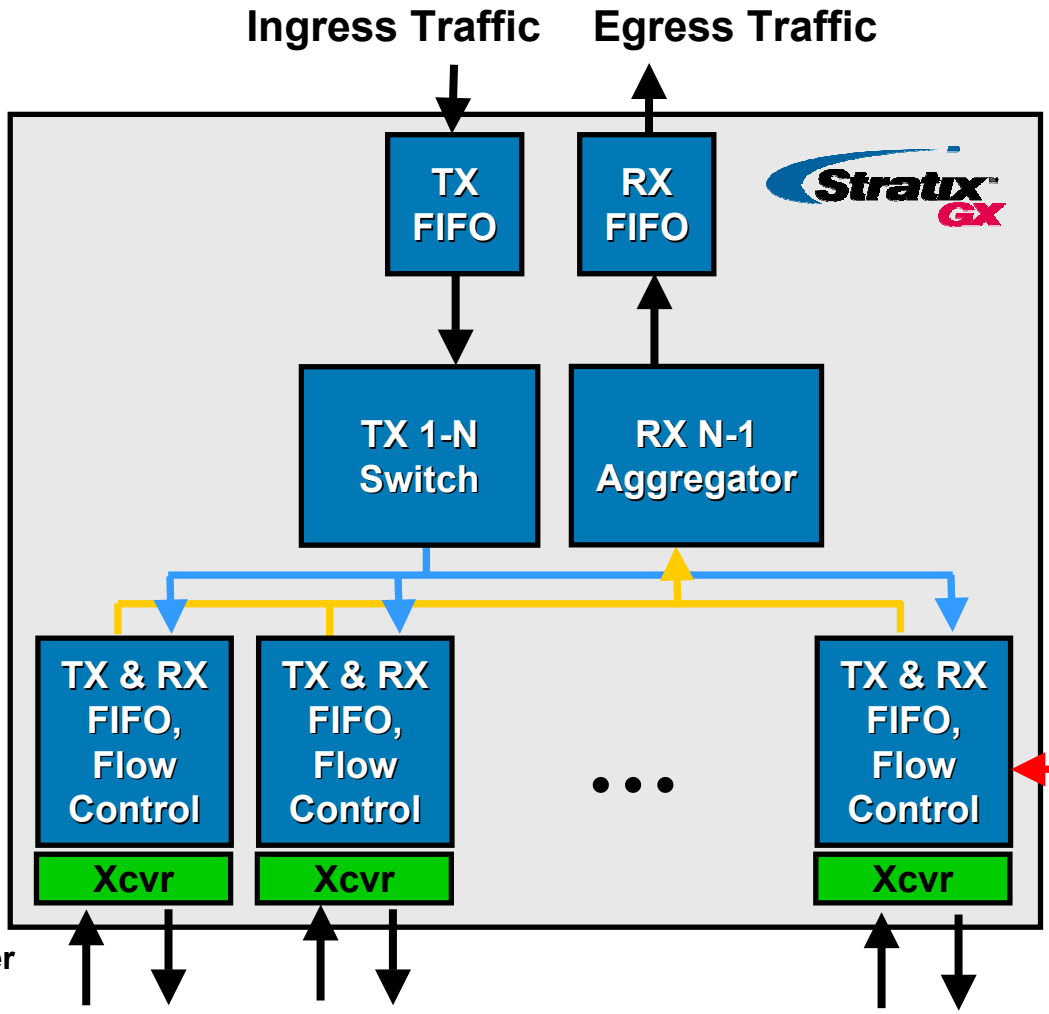
Distributed Switch Module



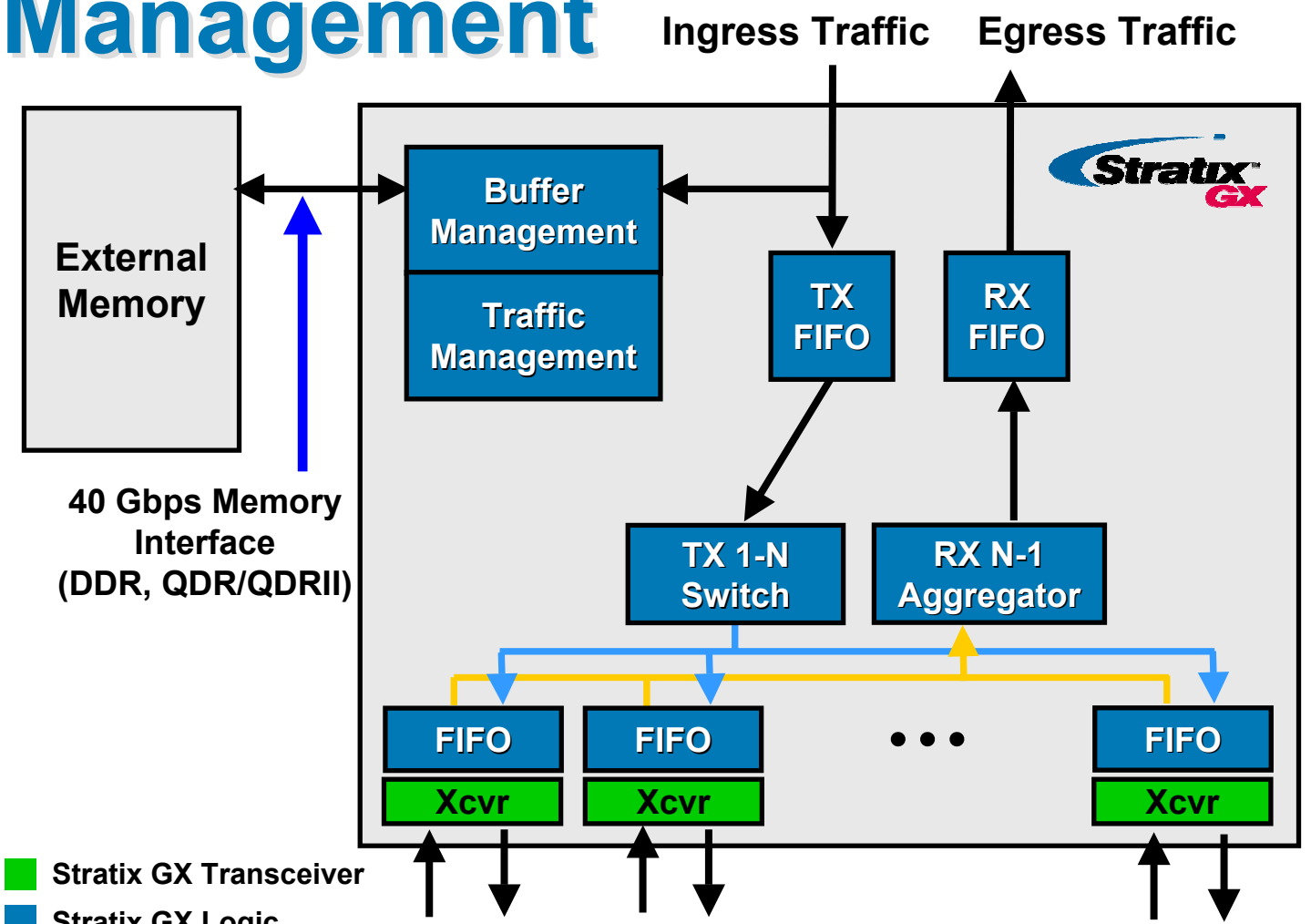
Distributed Switch Module



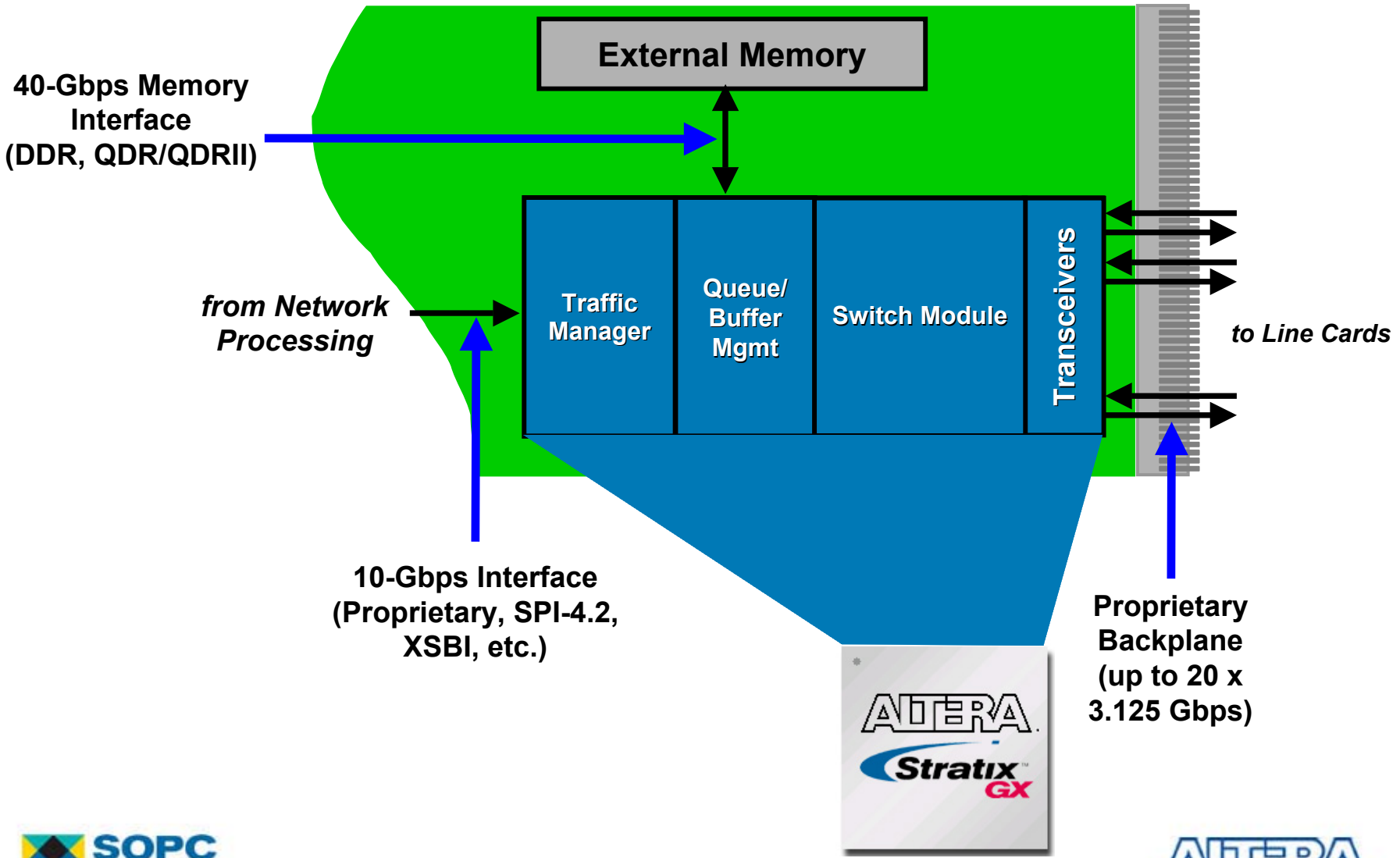
Distributed Switch Module



Integrated Traffic & Buffer Management

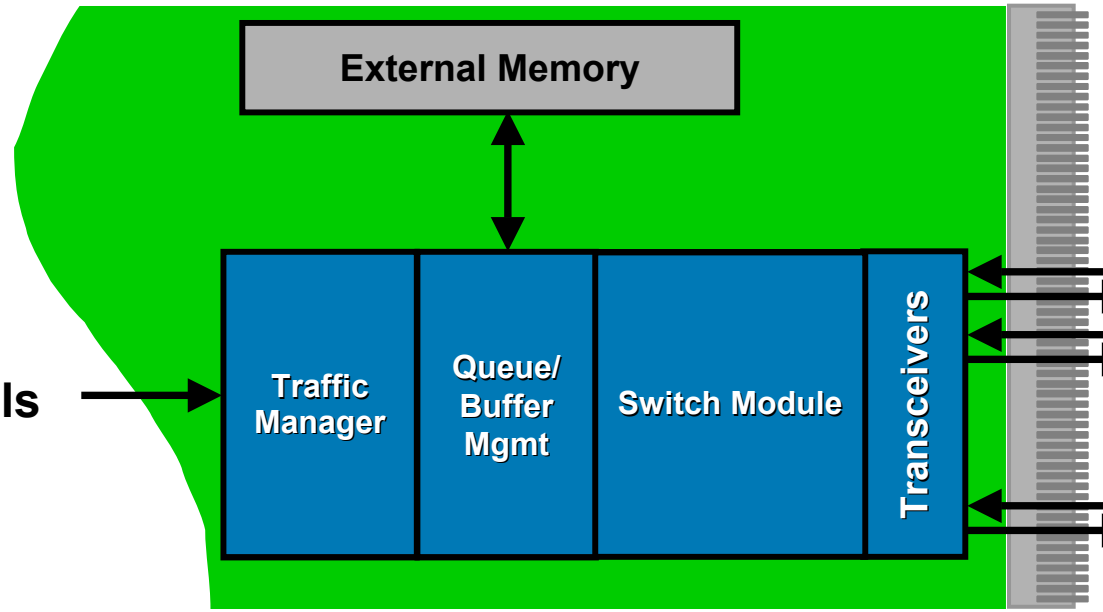


Stratix GX Solution



Distributed Switch Fabric Sample Implementation

- 16 Line Card System
- Fixed Cell Size
- 64-Bit Data Path
- FIFO Depth (Tx & Rx)
  - Line Side: 128 Cells
  - Backplane Side: 32 Cells
- Includes Buffer & Traffic Manager with External Memory Interface

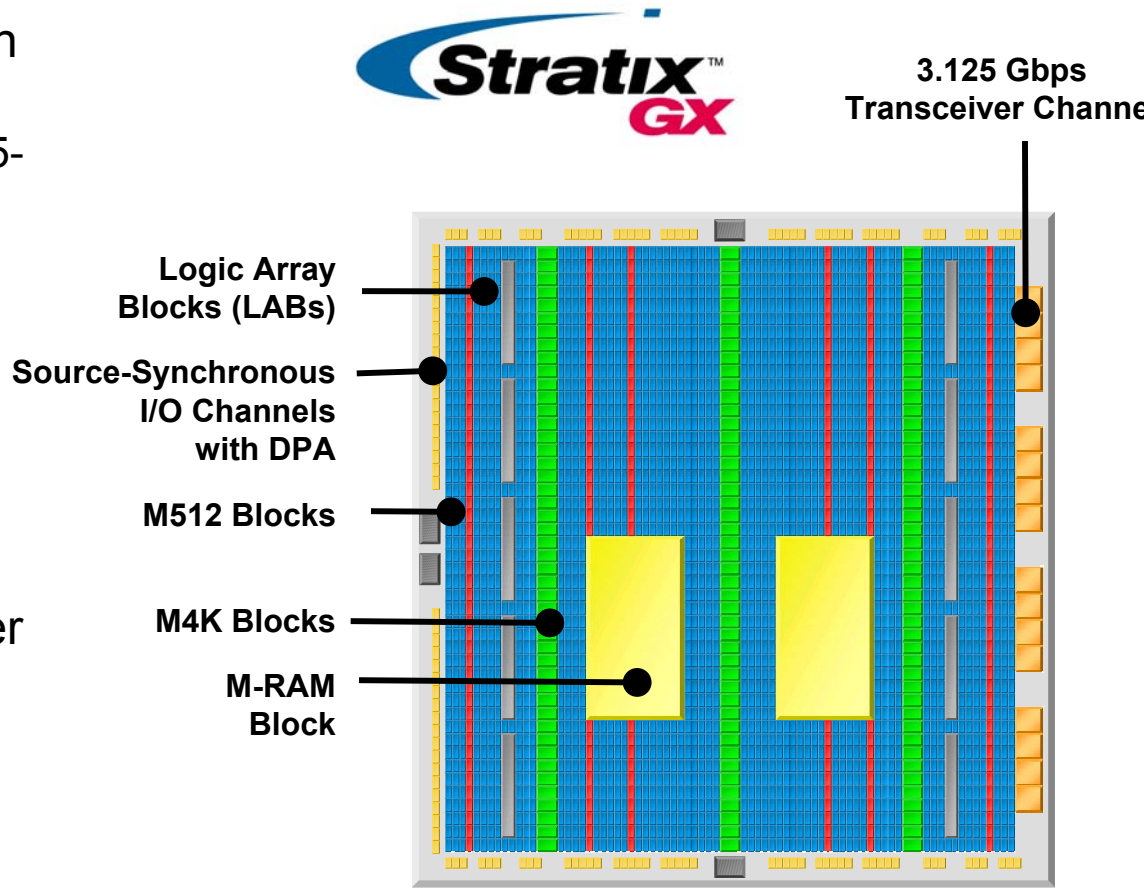


Design Results

M-RAM Block	1
M4K RAM Blocks	160
Logic Elements	35K
f_{MAX}	160 MHz
Transceiver Channels	16

Stratix GX for Distributed Switch Fabrics

- Can Support Many Links in One Device
  - Up to 20 Integrated 3.125-Gbps Transceivers
- Abundant Queuing Resources
  - Up to 183 M4K RAM Blocks (183 x 4KBits)
  - Up to 4 M-RAM Blocks (4 x 512 Kbits)
- Traffic Management, Buffer Management & Flow Control Functions
  - Over 41K LEs Available
  - Enhanced Memory Interface Support



Common Distributed Switch Fabric Design Needs

Needs	ASIC	Standard Part	Stratix GX
Customizable Traffic & Buffer Management	✓	N/A	✓
Customizable Scheduling, Buffering, & Switching	✓	N/A	✓
Real-Time Design & Debug		N/A	✓
Design Updates/Corrections in Field		N/A	✓
Time-to-Market		N/A	✓

Switch Fabrics:
Stratix GX Devices Deliver!

- Backplane Interface
  - Up to 20 Integrated 3.125-Gbps Transceivers
- High-Speed Chip-to-Chip Interfaces
  - 1-Gbps Source-Synchronous Channels with Dynamic Phase Alignment (DPA)
- Programmable Digital Functions
  - Stratix Device-Based Programmable Logic Architecture
- External Memory Buffering
  - DDR, FCRAM, SDR, ZBT, QDR/QDRII
- Internal Buffering
  - Over 400-KBytes of TriMatrix Memory
- Proprietary & Atypical Implementations
  - Designed to Provide Superior Flexibility