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Optimal Management of System Clock Networks

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Introduction

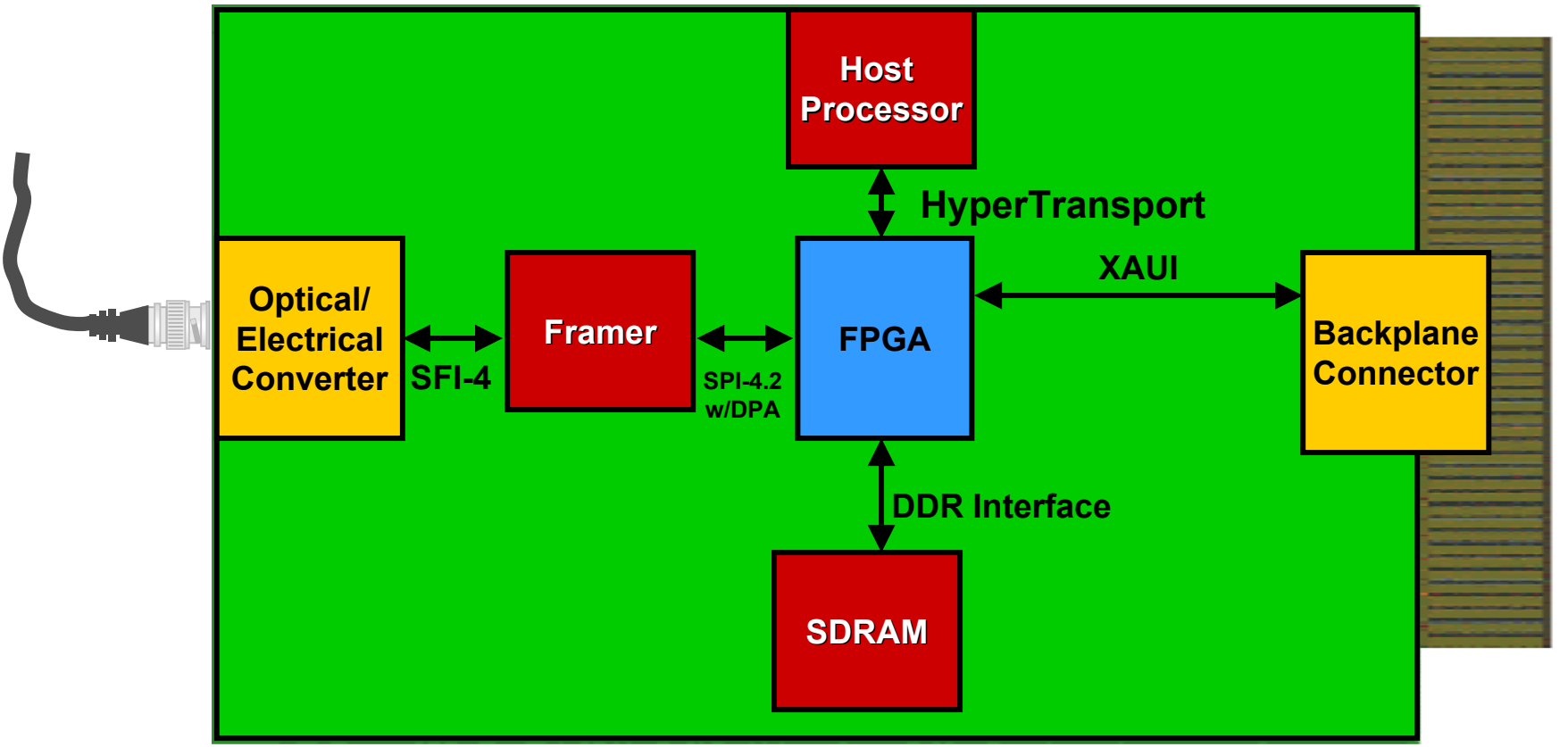
- System Clock Management Is More Challenging
  - No Longer One Synchronous Clock per System or Card
  - Must Design Source-Synchronous or CDR Interfaces with Multiple Clock Domains
- Higher Clock Speeds Increase Importance of Timing & Jitter Analysis

Agenda

- Examine Communications Line Card Design Examples
  - Identify & Solve Clocking Challenges
- Examine System Clocking Schemes
- Jitter Discussion

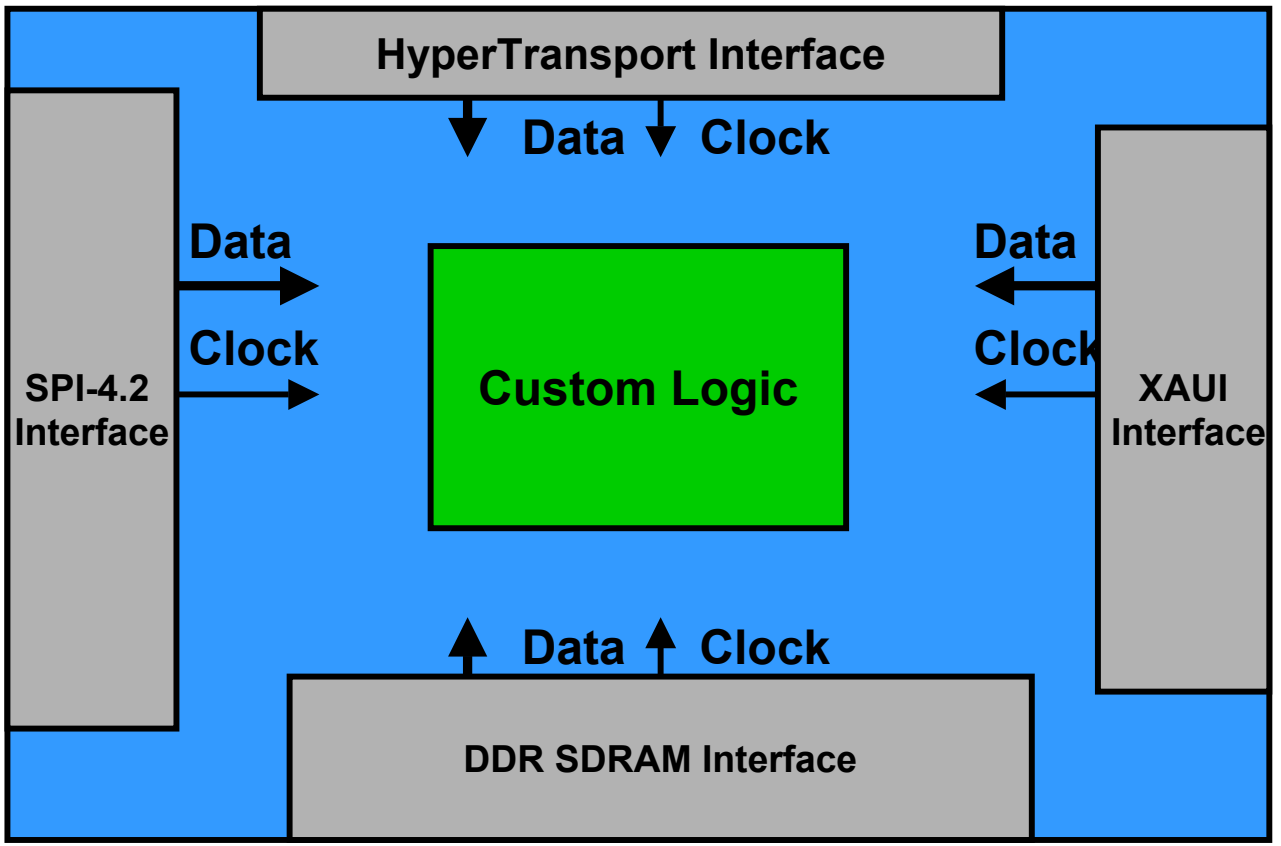
Line Card Example

- FPGA Takes on Central Interface Role



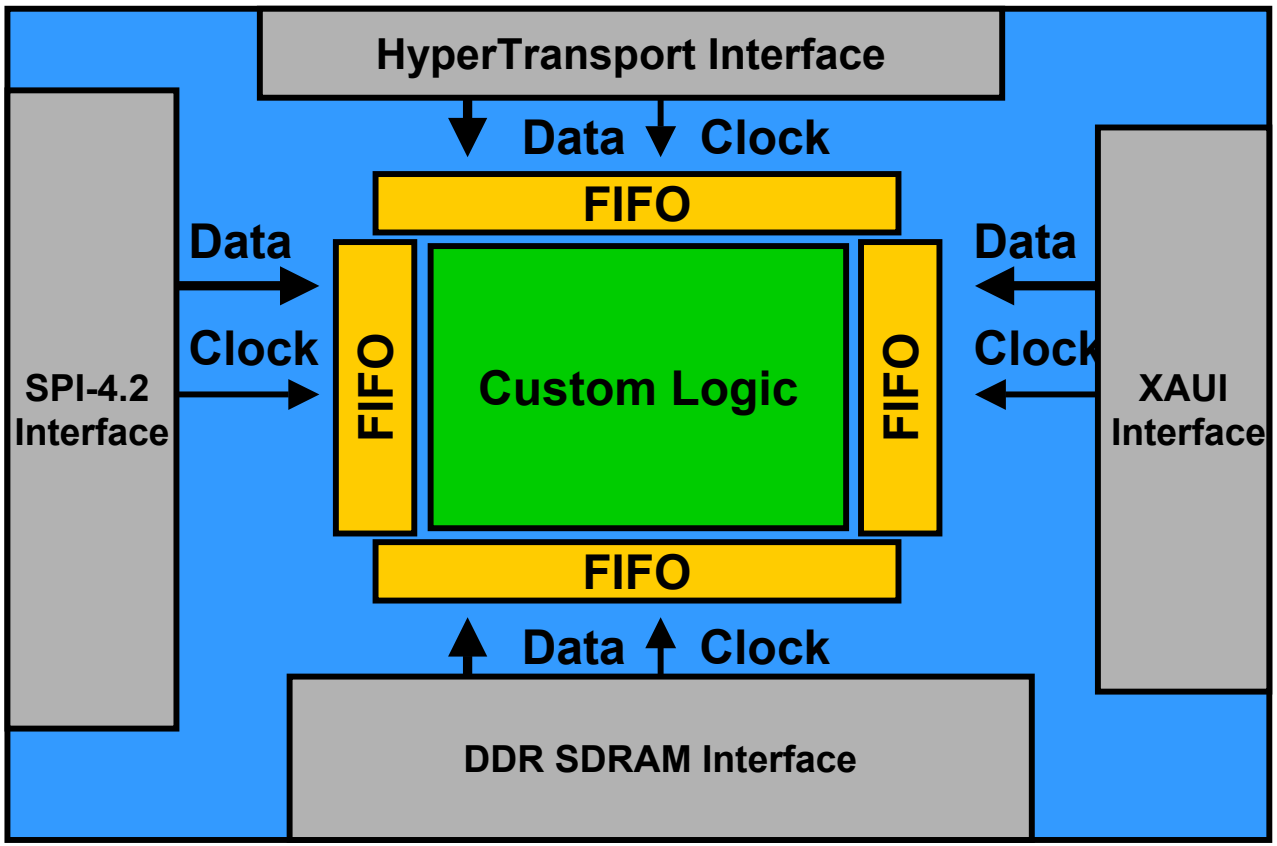
Line Card Example (Con't)

- FPGA Takes on Central Interface Role



Stratix Clocking Solutions

- Stratix™ Device Incorporates up to 48 Clock Trees
- Implement FIFOs with TriMatrix™ Memory

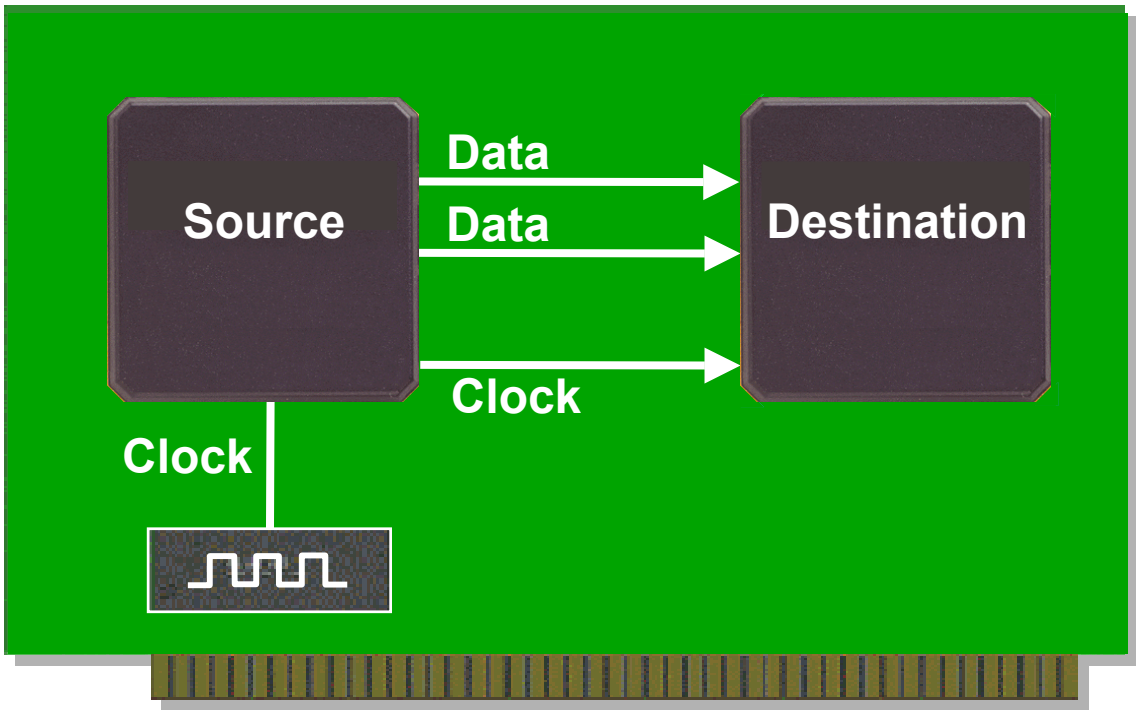


System Clock Schemes

- Source-Synchronous Interface
  - SFI-4 (SERDES-to-Framer Interface Level 4)
  - HyperTransport™ Technology
- Dynamic Phase Alignment (DPA)
  - SPI-4.2 (System Physical Interface Level 4.2)
- Clock-Data Recovery
  - XAUI (10 Gigabit Attachment Unit Interface)

Source-Synchronous Clocking

- Clock Signal Transmitted with Data
- Board Skew Reduces System Performance



Source-Synchronous Benefits

- Source-Synchronous Clocking Enables Data Transfer at High Speeds
  - Performance No Longer Limited by t_{CO}, t_{PD} & t_{SU}
  - Maximum Performance Factors
    - Edge Rate of Driver
    - Skew between Data Signals & Clock Signals

Source-Synchronous Drawbacks

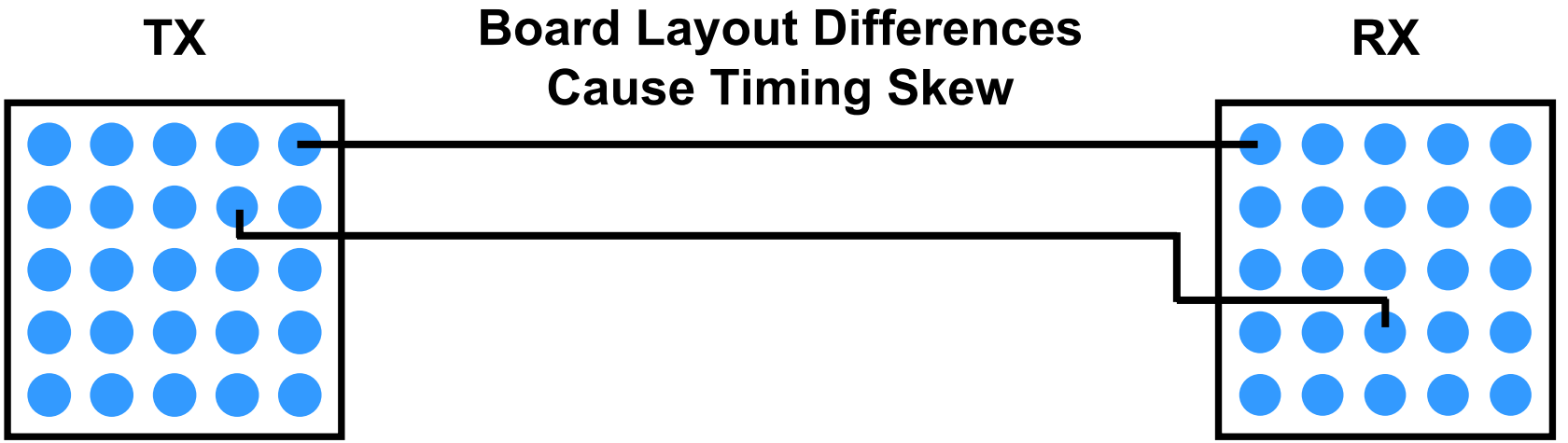
- Every Chip-to-Chip Data Transfer Introduces New Clock Domain
  - Receiver Must Manage Multiple Clock Domains
- Performance Affected by Board Skew
  - Skew Reduction Complicates Board Design

Source-Synchronous Interfaces

Transmission Line Type	Channel Data Rate	Clock
HyperTransport	1.6 Gbps	800 MHz
SFI-4	622 - 700+ MBPS	622 - 700+ MHz
SPI-4	622 - 832 MBPS	311 - 416 MHz
RapidIO	2.0 Gbps	1.0 GHz

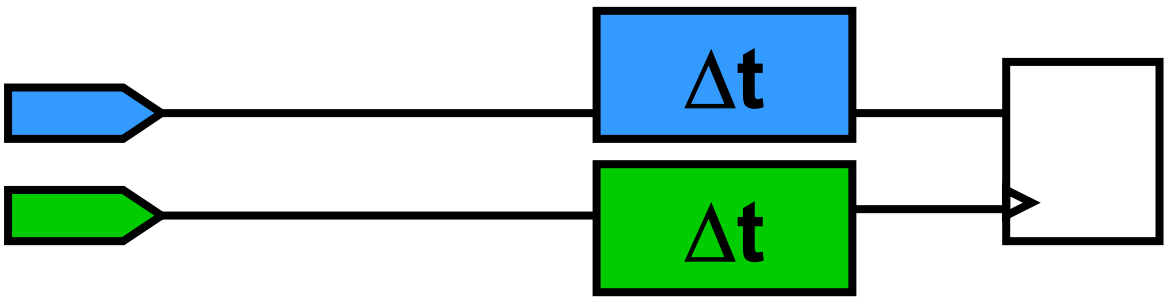
Need for DPA

- In Clock-Forwarding System, Clock-Data Skew Reduces Performance
- SPI-4.2
  - Sample Timing Budget Allocates 150 ps for Skew: ~1 Inch
  - Meeting Skew Spec May Require Vias
  - Connector Adds More Skew



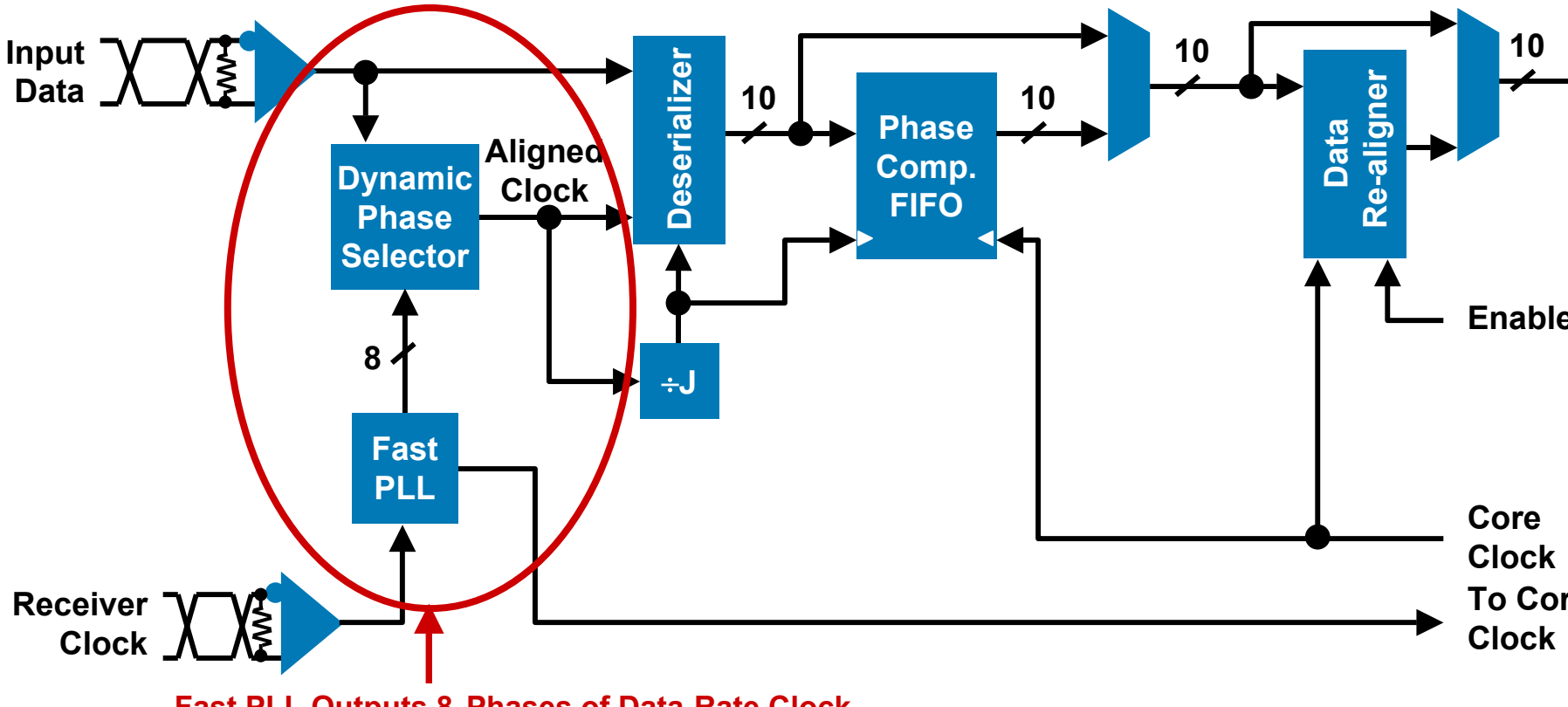
Dynamic Phase Alignment

- Receiver Self-Corrects for System Skew
  - Individual Adjustment for Each Channel
- May Align At Power-Up or Continuously
- Two Basic Approaches
  - **Vary Delay of Data** into Capture Register
  - **Vary Delay/Phase of Clock** Driving Capture Register
- Varying Clock Phase Is Best to Avoid PVT Effects



Stratix GX Solution

- DPA Implemented In Hard Circuitry
- Truly Dynamically Adjustable



Fast PLL Outputs 8 Phases of Data-Rate Clock

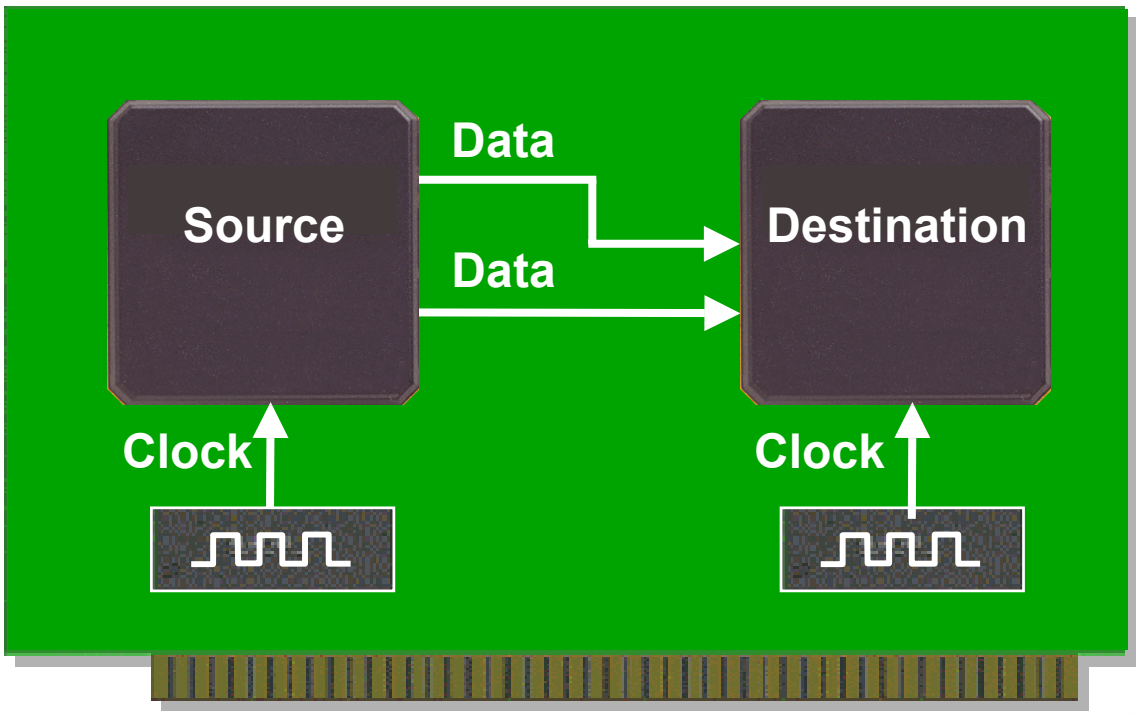
Dynamic Phase Selector Chooses Appropriate Phase Based on Input Data

DPA Applications

- SPI 4.2 Specification Includes DPA Option
- Other Source-Synchronous Interfaces Can Benefit
  - HyperTransport
  - RapidIO
  - Proprietary

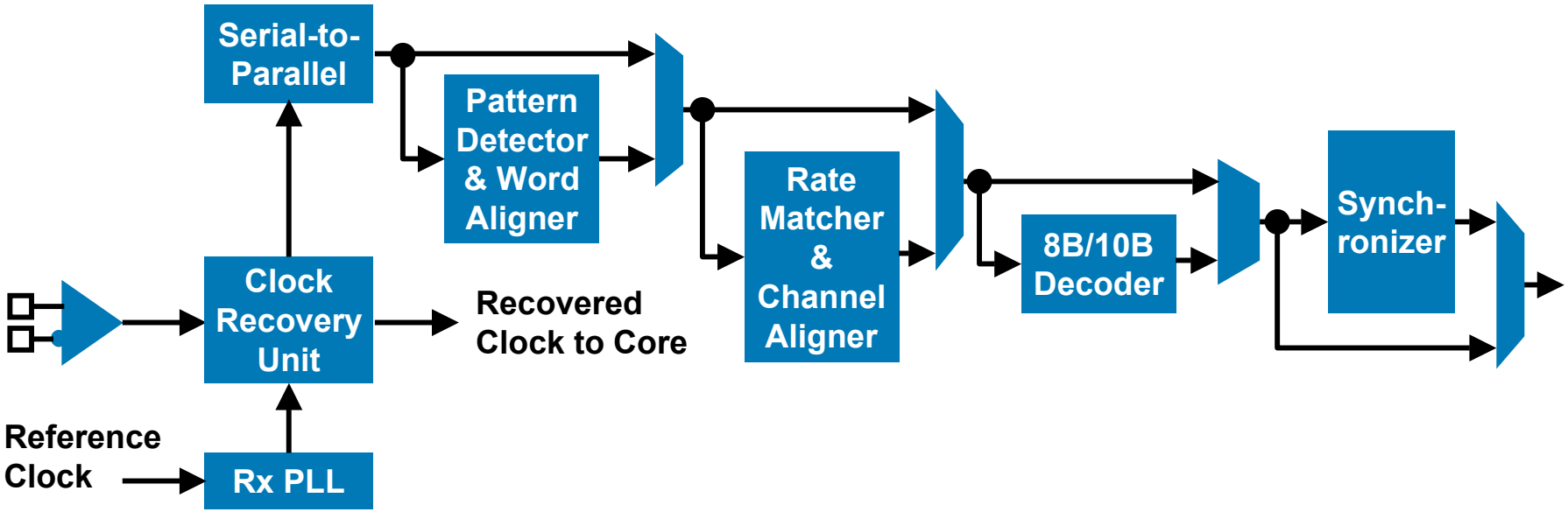
Clock Data Recovery (CDR)

- Reference Clock Is Used
- Trace Lengths Need Not Match
- Each Source & Destination May Have Individual Clock



Stratix GX CDR Implementation

- Clock Encoded into Data Stream
- PLL Recovers Clock from Data Transitions



Implements All Blocks Needed for XAUI PHY

CDR Benefits

- Receiver Recovers Individual Clocks from Each Incoming Data Channel
  - Each Channel Can Have Phase Variation
- Transmitters Can Operate on Multiple Crystals
  - Each Channel Can Have Limited Frequency Variation

CDR Drawbacks

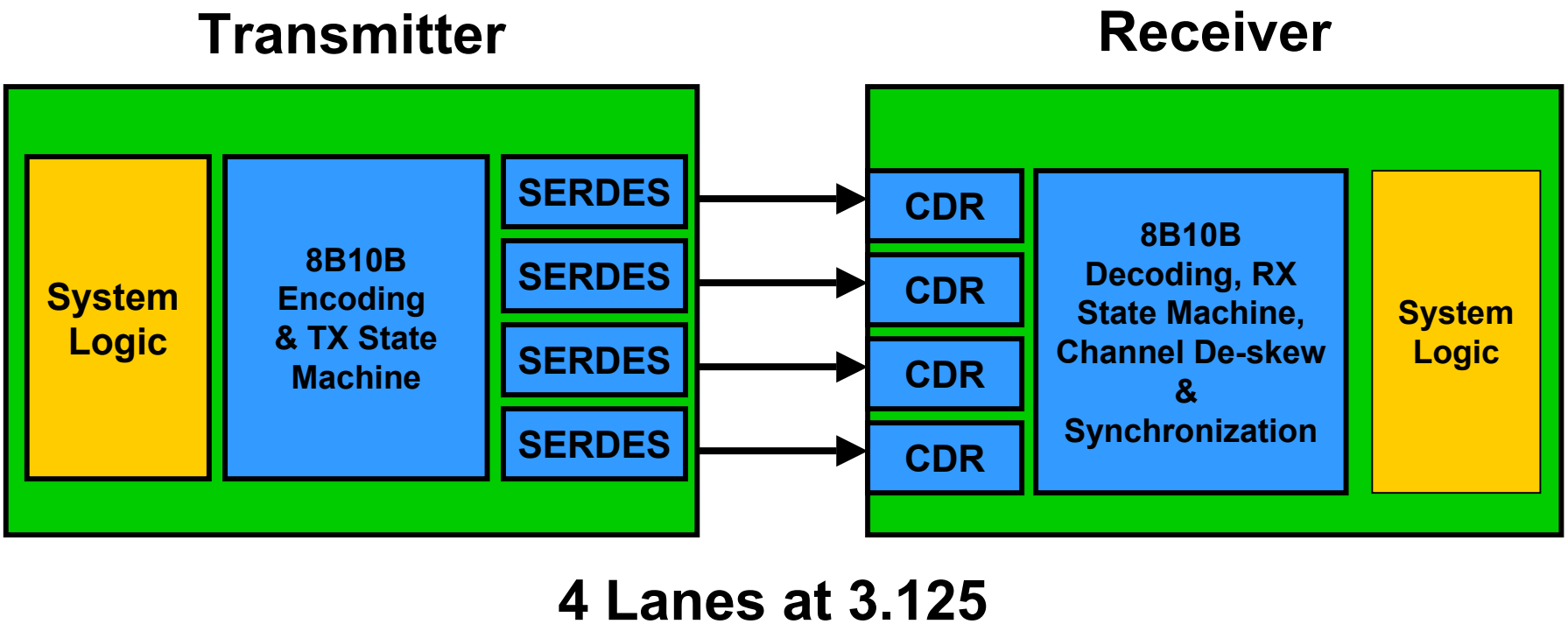
- Encoding Schemes Used to Ensure Maximum Run Length
  - Transitions Required for Clock Recovery
  - Some Data Channel Bandwidth Used to Encode the Data
  - 3.125-Gbit Bandwidth Used for 2.50-Gbit Data
- Data Buffering Required to Accommodate Frequency Variation
- Channel-to-Channel Alignment Logic Required

CDR Application: XAUI

- 10 Gigabit Attachment Unit Interface (XAUI)
- IEEE Specification 802.3
- Versatile Standard:
  - Chip-to-Chip via PCB
  - Board-to-Board via Backplane

XAUI Implementation

- Blue Boxes Ideally Implemented in Hard Logic in FPGA for Maximum Performance



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PLL Jitter Characteristics

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Jitter Classes

- Random
  - Probabilistic Timing Variations
  - Caused by Random Thermal Effects
- Deterministic
  - Repeatable Timing Variations
  - Caused by Specific Issues
    - Signal Modulation, Crosstalk

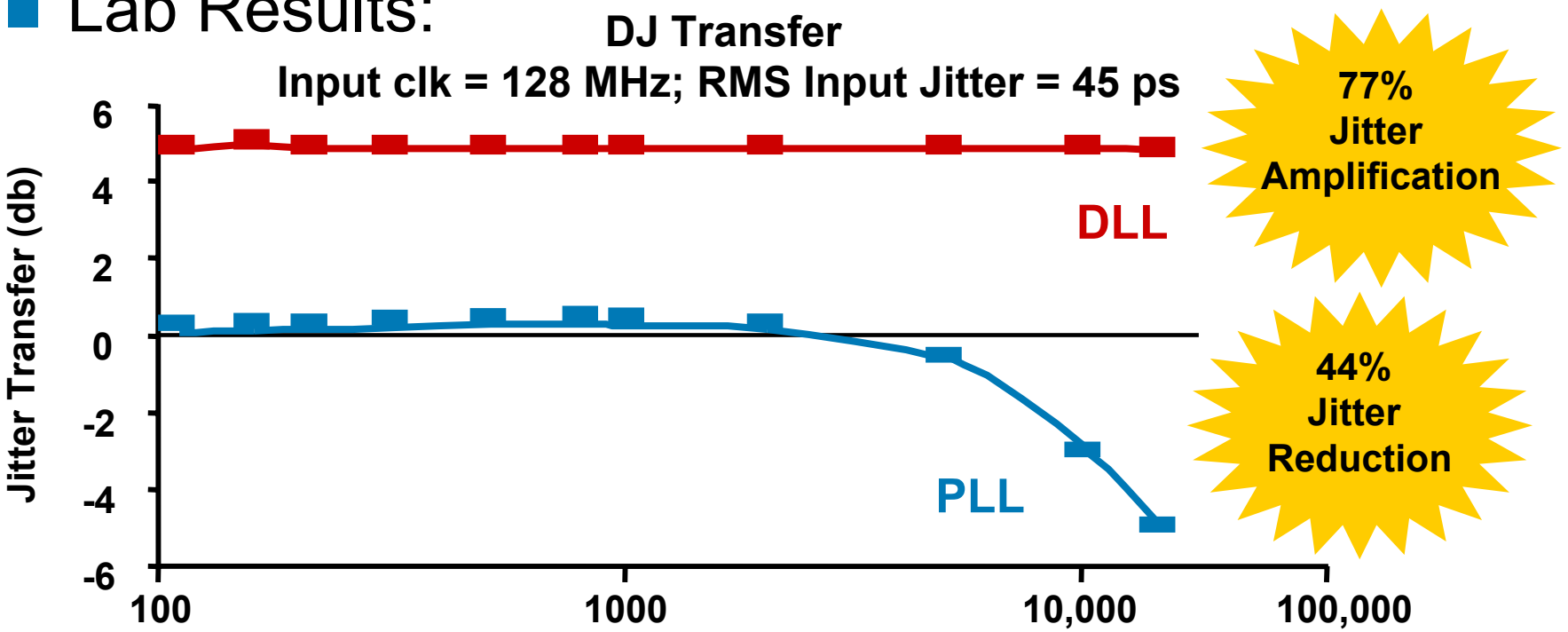
Total Jitter = Random + Deterministic

Jitter Transfer Definition

- Input Jitter May Be Reduced or Amplified
- Transfer Curve Shows Performance
  - > 0 dB: Amplification
  - < 0 dB: Reduction
- Deterministic & Random Jitter Transfer May Be Different

Deterministic Jitter Transfer

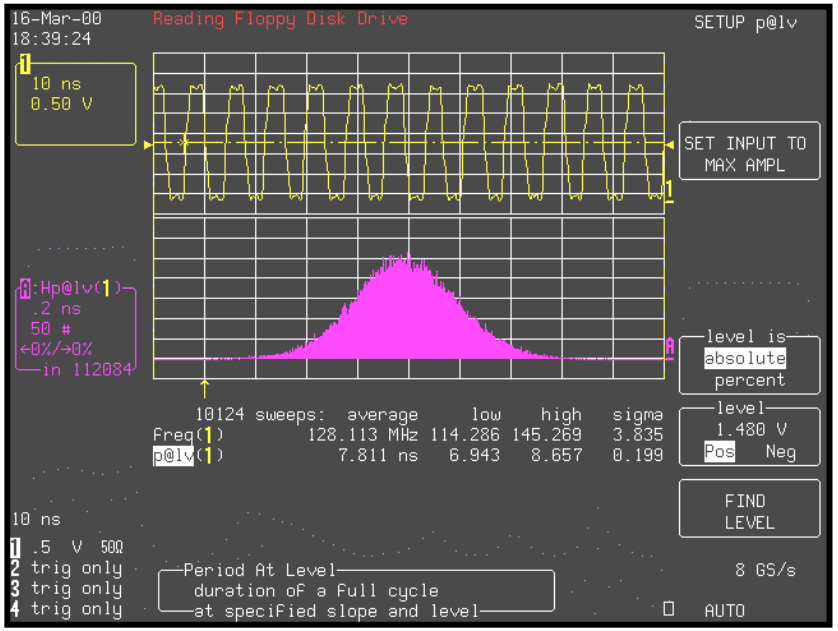
- PLL Can Reduce Deterministic Jitter
- Delay-Locked Loop (DLL) Amplifies Deterministic Jitter
- Lab Results:



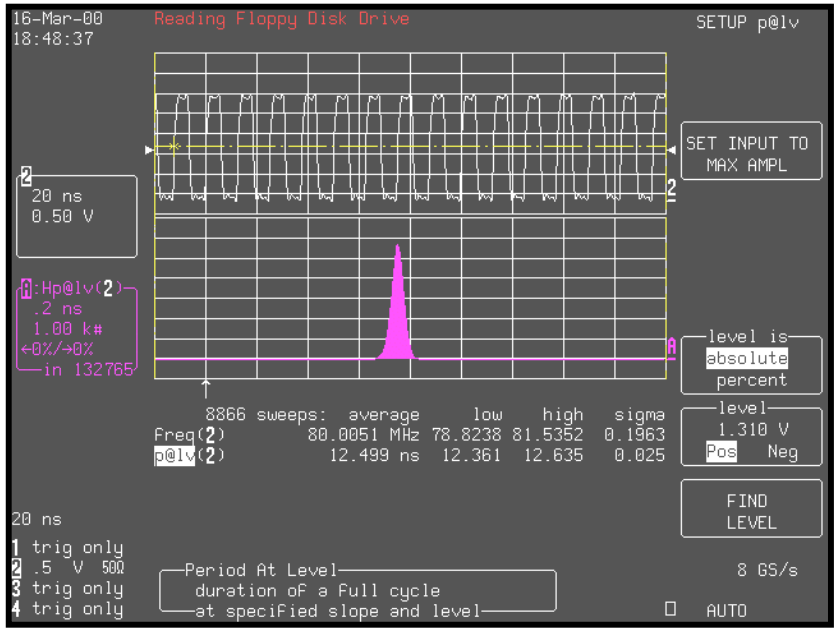
Random Jitter Transfer

- PLL Reduces Random Jitter

PLL Input Clock



PLL Output Clock



Jitter Summary

- Jitter Limits System Performance
- Use PLL To Reduce Jitter & Enhance System Timing Margin

Summary

- Advanced Systems Present Difficult Clock-Management Challenges
- Use Source-Synchronous, DPA, or CDR Interfaces to Achieve High-System Data Rates
- Consider Jitter Effect On System