



SOPC
WORLD
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MathWorks Integrated Design Solution

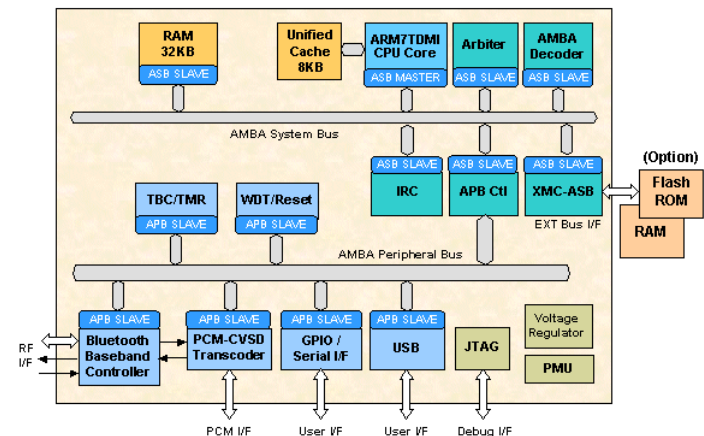
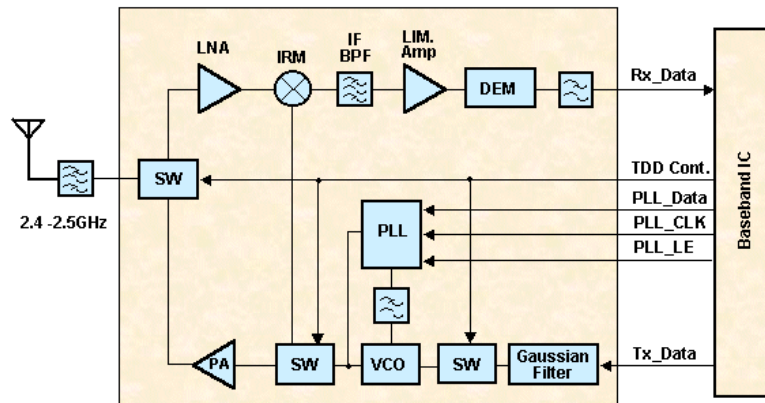
The MathWorks at a Glance

- Founded in 1984, privately held
- Headquarters in Natick, Massachusetts (near Boston)
- European offices in the UK, France, Germany, Switzerland, Italy, Spain, and Benelux region
- Over 1000 employees, including $\frac{1}{3}$ in product development
- More than 500,000 users in 100 countries, on all seven continents!



Today's System and IC Design Challenges

- Hardware: RF/Analog, Digital IC, FPGA
- Software: DSP, MAC, Control, Use interface
- Moving partitioning boundaries
 - Analog \leftrightarrow Digital IC \leftrightarrow FPGA \leftrightarrow DSP S/W \leftrightarrow Micro controller S/W
- Implementation specific tools lock your IP into one target type
 - Spice, HDL, ASM , C/C++

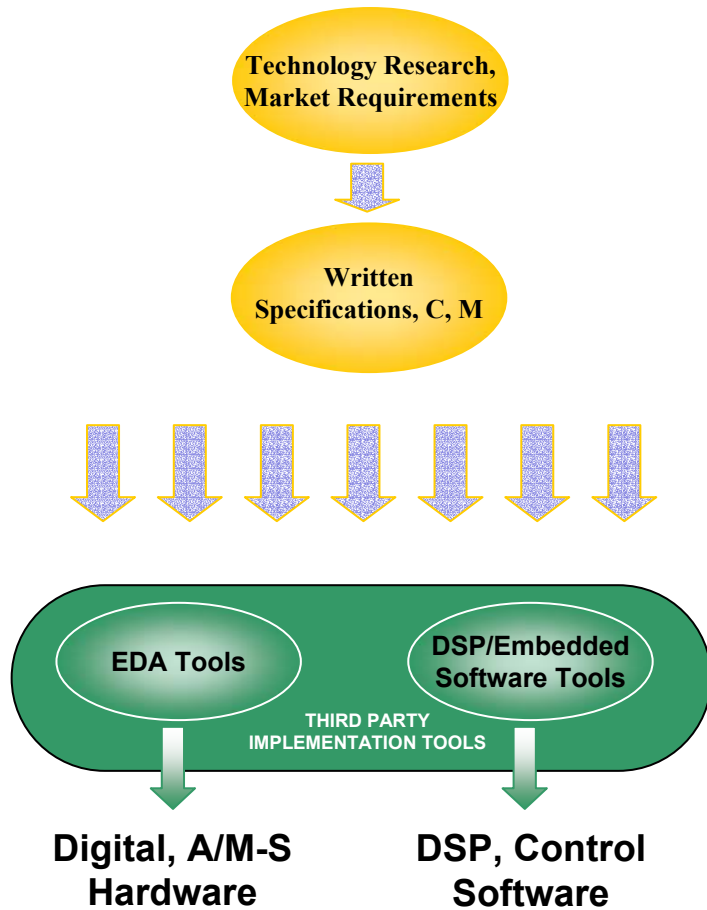


Today's Business and Organization Challenges

- Time-to-market pressure
 - A few months delay has huge revenue impact
- Team integration
 - Analog/Mixed-Signal, Digital hardware, DSP S/W, Control S/W teams
 - All speak a different language and communicate via written documents
- Increasing ASIC mask costs



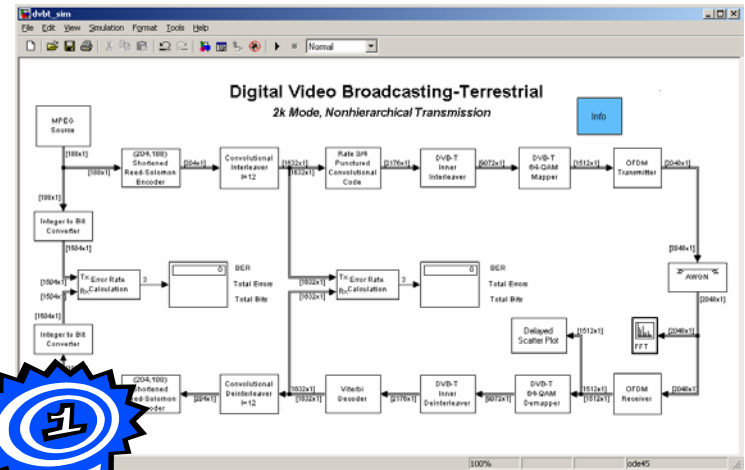
Traditional Flow: Little or No Early Simulation



- Technology research and market requirements
- Systems engineering
- Partition into components create written specifications for teams
- Minimal or no simulation. C, M
- Design failure risk high. Flaws detected late, during circuit level, RTL or C/ASM code design
- Risk of time-to-market delays

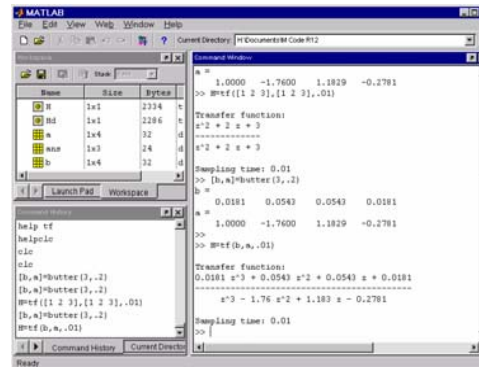
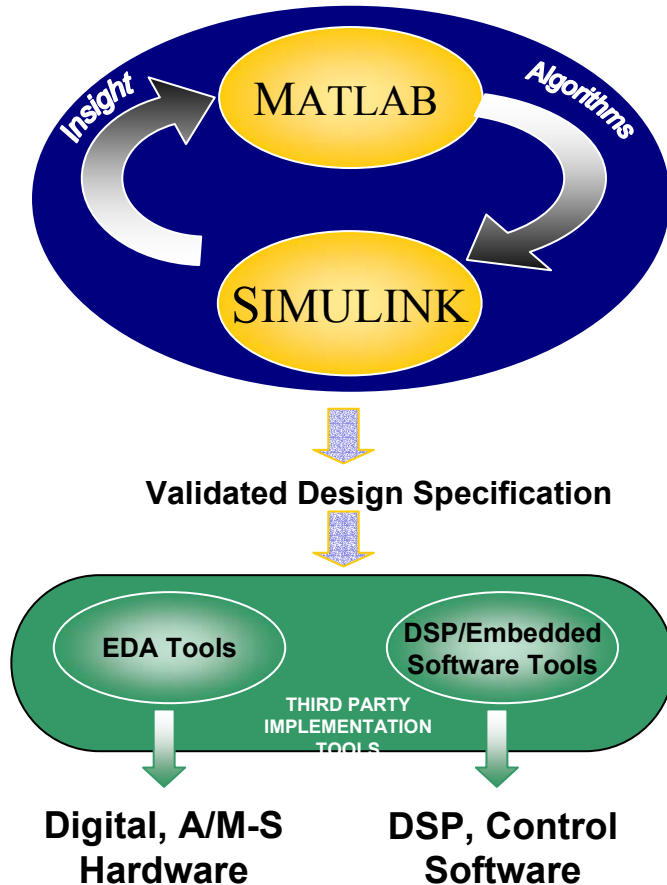
What if You Could...?

- Build a model of a complete system in minutes or days
- Simulate the behavior of the whole system before starting low-level design work?
 - Analog, digital and control together
 - Test for design flaws early
 - Trade-off architectures and parameter in minutes find best design
- Communicate your ideas and share with other teams?
- Keep your IP in an implementation neutral tool as long as possible?
- Only start development with a validated, fully tested design?



The MathWorks System-Level Solution

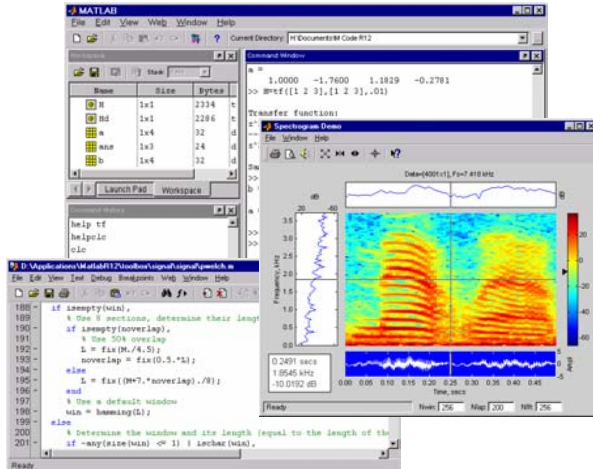
- MATLAB and Simulink
- Before circuit level, RTL or C/ASM code design
- Create a validated reference design



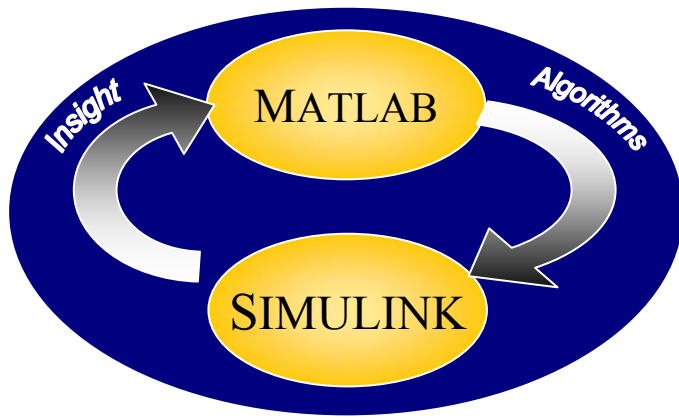
MATLAB

MATLAB

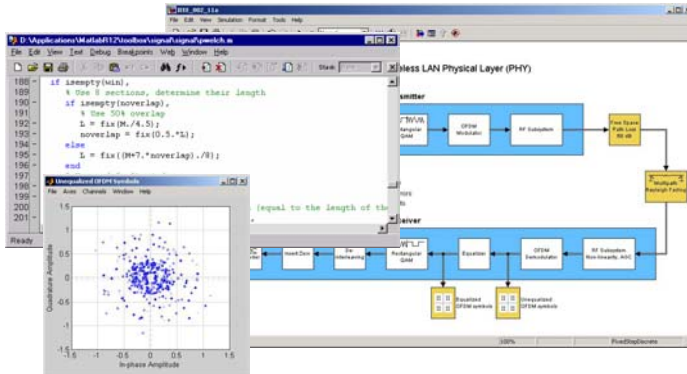
- Research new technology
- Perform mathematical modeling
- Development algorithms
- Acquire, visualize and analyze data



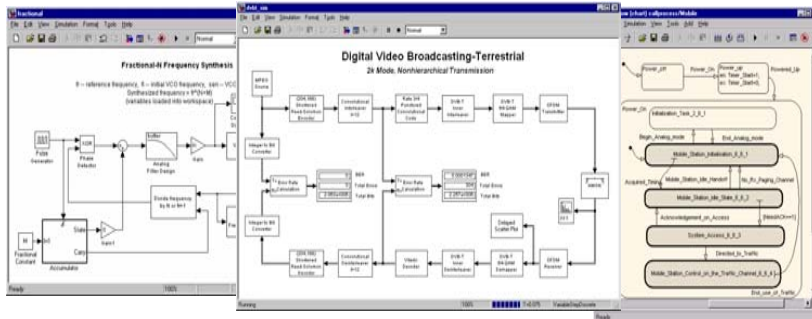
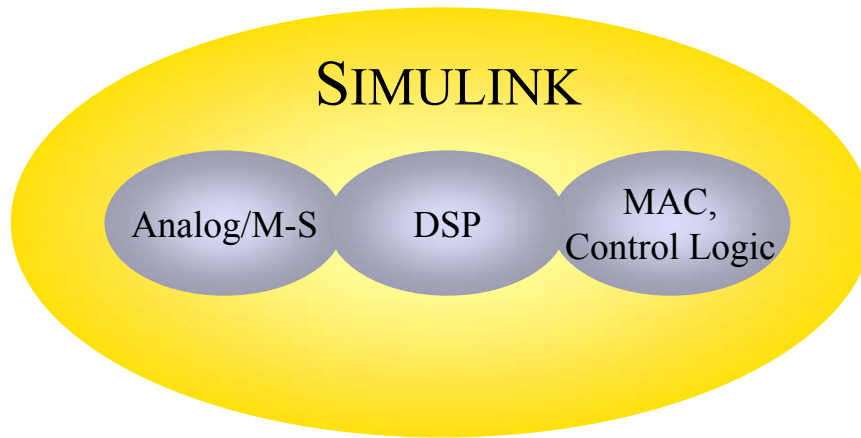
Simulink



- Graphically design architecture and simulate behavior of whole system. Bit-true cycle accurate.
- From libraries of pre-built blocks
- Import C or MATLAB Code
- Test, optimize, explore parameter and architecture trade-offs



Model Different Components



■ Analog/Mixed-Signal

- PLLs, data converters
- Continuous time, variable-step ODE solvers

■ DSP Baseband

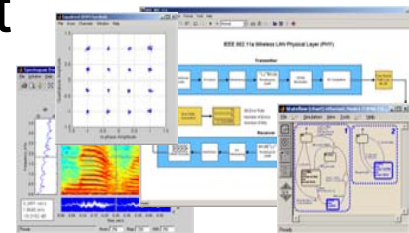
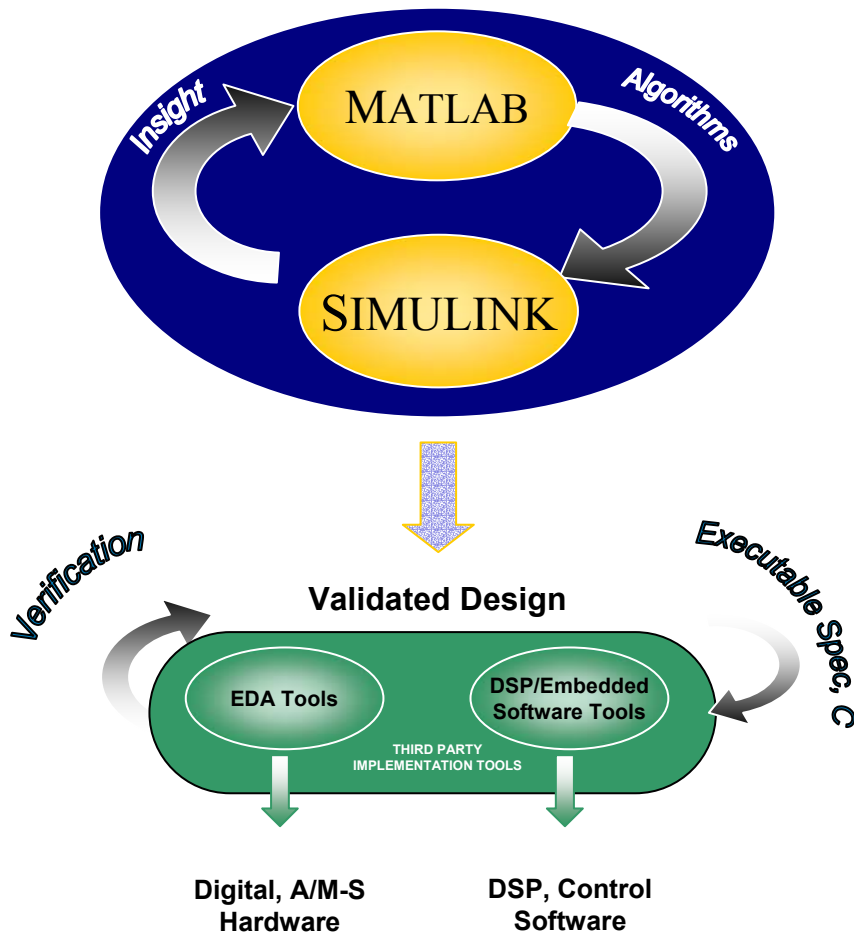
- Discrete time, fast frame-based processing. Bit-true cycle accurate.

■ MAC layer/Data Link Layer

- Simple protocols, acknowledgement schemes
- Reactive or event driven state machines
- With Stateflow

Use a Validated Design

- Create **validated design**
- Use as reference or executable specification to test low-level designs against
- Provide clear specifications
- Detect design flaws early
- Reduce design risk and time-to-market



Motorola's Wireless Subscriber Systems Group

■ Challenge

- Mixed-signal Phase-Locked Loop (PLL) design
- Cycle-to-cycle jitter and loop locking sensitivity
- SPICE/Verilog
- 100 μ secs: 2 hours

■ Solution

- Simulink
- Faster development time and simulation time
- 100 μ secs : 2.5 mins
- Sub-picosecond resolution

“The Simulink models exceeded our project specifications for required simulation speed. Accurate simulations can now be measured in minutes rather than hours or days.”

Yuan Yuan, Motorola

PHY Design Case Study: IEEE 802.11b

■ IEEE Standard Document

- 600 pages (11 + b appendix)
- 4 modes (1, 2, 5.5 and 11Mbps)

■ Components

- Framing and CRC
- Long/short preamble and sync
- Modulation and spreading
- Filtering
- Channel number selection (1-11)
- RF subsystems, Tx power, mask, power-on ramp



1Mbps Mode

- Modulation
 - DBPSK
- Spread
 - 11 chips Barker sequence per symbol
- Pulse shaping
 - 4/8 samples per chip
 - Root raised cosine
- Channel
 - AWGN

The leftmost chip shall be output first in time. The first chip shall be aligned at the start of a transmitted symbol. The symbol duration shall be exactly 11 chips long.

15.4.6.4 Modulation and channel data rates

Two modulation formats and data rates are specified for the DSSS PHY: a *basic access rate* and an *enhanced access rate*. The basic access rate shall be based on 1 Mbit/s DBPSK modulation. The DBPSK encoder is specified in Table 65. The enhanced access rate shall be based on 2 Mbit/s DQPSK. The DQPSK encoder is specified in Table 66. (In the tables, $\pm\theta$ shall be defined as counterclockwise rotation.)

Table 65—1 Mbit/s DBPSK encoding table

Bit input	Phase change ($\pm\theta$)
0	0
1	π

Table 66—2 Mbit/s DQPSK encoding table

Dibit pattern (d_0, d_1) d_0 is first in time	Phase change ($\pm\theta$)
00	0
01	$\pi/2$



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C/C++

```
Microsoft Visual C++ - [D:\... \sopc\source\main.cpp]
File Edit View Insert Project Build Tools Window Help
[Global] All global members main
Workspace browser: Source Headers Resources
//** Main loop
//*****
// Total number of bit errors
int errors = 0;
int bitsCompared = 0;
RandomBit rng; // Random bit generator

for (int i=0; i<packetCount; ++i) {
    Bits pktDesired = rng.nextNBits(packetLength);
    Bits pktIF = rng.nextNBits(16*packetLength);

    // At beginning of each packet, reset phase for desired signal to zero
    // set a random phase difference and time delay for interference signal
    txDesiredPtr->reset();
    txIFPtr->reset();
    double delPhase = Random::drand();
    txIFPtr->reset();
    txIFPtr->usePhase(delPhase);
    rxDesiredPtr->reset();

    int Td = 0;
    if (bitrateDes == bitrateIF) {
        Td = Random::irand(nSamples);
    }
    Signal sigIF(nSamples+Td);

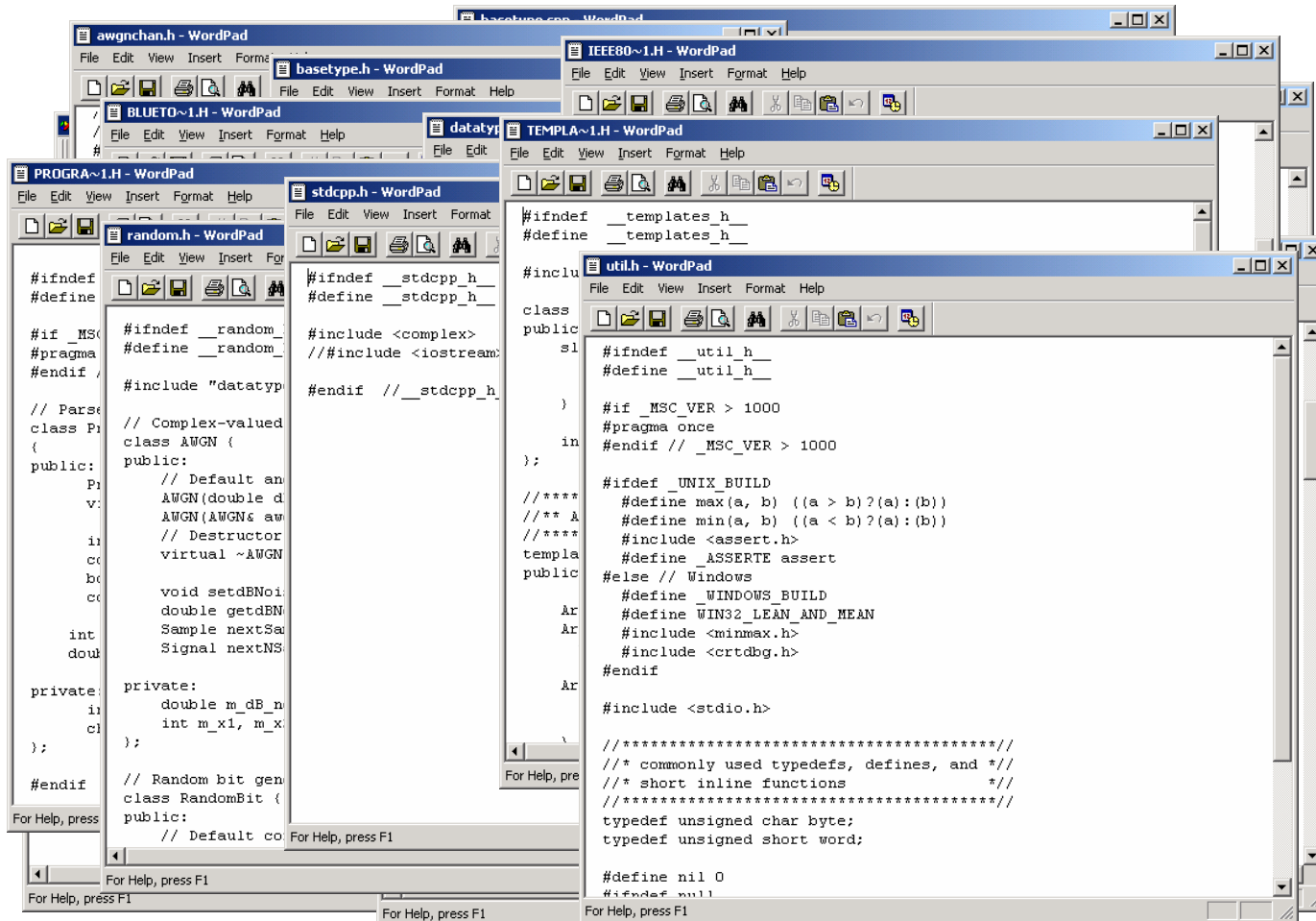
    for (int j=0; j<packetLength; j += nBitsDes, k += nBitsIF) {
        // Delay interference signal by Td samples
        sigIF[slice(Td, nSamples, 1)] = j * twiIFPtr->transmit(pktIF[slice(k, nBitsIF, 1)], dfreq);
        sigIF.set(j * twiIFPtr->transmit(pktIF[slice(k, nBitsIF, 1)], dfreq), Td, Td+nSamples-1);
        // Transmit desired signal
        Signal sigDesired = txDesiredPtr->transmit(pktDesired[slice(j, nBitsDes, 1)], 0);
        // Compute channel output
        Signal sigOut = awgn_process(sigDesired, sigIF[slice(0, nSamples, 1)]);
        // Decode channel output into received bits
        Bits rxBits = rxDesiredPtr->receive(sigOut);
        if ((j >= sysDelay) && (j<(packetLength-stopAt))) {
            errors += bitErrors(rxBits, pktDesired[slice(j-sysDelay, nBitsDes, 1)]);
            bitsCompared += nBitsDes;
        } else if ((j == 0) && (bitrateDes == 1)) {
```

NIST 802.11b and Bluetooth C/C++ Code



- w3.antd.nist.gov/wctg/bluetooth/btint.html
- Bluetooth and 802.11b
- 802.11b
 - Random bits
 - 1 or 11Mbps modulation and spreading
 - Filtering
- Bluetooth
 - Random bits
 - Modulation
 - Filtering

C/C++ Code: 17 Files, 1500-2000 lines



The image shows a collection of overlapping WordPad windows, each displaying a different C/C++ header file. The windows are titled as follows: awgnchan.h, basetype.h, IEEE80~1.H, BLUEETO~1.H, datatyp, TEMPLA~1.H, PROGRA~1.H, stdcpp.h, random.h, and util.h. The code in these files includes preprocessor directives like #ifndef, #define, #include, and #endif, as well as C++ class definitions and function prototypes. For example, the 'util.h' window shows a class 'public' and various macros for max, min, and assert. The 'stdcpp.h' window shows a class 'stdcpp_h' and includes for <complex> and <iostream>. The 'random.h' window shows a class 'RandomBit' and a function 'RandomBit'. The 'basetype.h' window shows a class 'AWGN' and a function 'setdBNoi'. The 'IEEE80~1.H' window shows a class 'IEEE80~1' and a function 'IEEE80~1'. The 'BLUEETO~1.H' window shows a class 'BLUEETO~1' and a function 'BLUEETO~1'. The 'awgnchan.h' window shows a class 'awgnchan' and a function 'awgnchan'. The 'PROGRA~1.H' window shows a class 'PROGRA~1' and a function 'PROGRA~1'. The 'datatyp' window shows a class 'datatyp' and a function 'datatyp'. The 'TEMPLA~1.H' window shows a class 'TEMPLA~1' and a function 'TEMPLA~1'. The 'stdcpp.h' window shows a class 'stdcpp_h' and a function 'stdcpp_h'. The 'random.h' window shows a class 'RandomBit' and a function 'RandomBit'. The 'util.h' window shows a class 'public' and various macros for max, min, and assert.



C/C++ Code: Build, Run, Debug, and Change

- Build and run
 - Bug: File I/O
- Speed
 - 7 secs for 100 packets
- Time to create
 - 400 days @ 5 lines/day
 - 40 days @ 50 lines/day
- Removing Bluetooth
 - Difficult. Many implicit dependencies

The screenshot shows the Microsoft Visual C++ IDE. The top window displays the source files for the 'btint' project, including 'awgnchan.cpp', 'basetype.cpp', 'bluetooth.cpp', 'ieee802_11b.cpp', 'main.cpp', 'programargs.cpp', and 'random.cpp'. The bottom window shows the output of the build process, including the compilation of these files and the execution of 'btint.exe'. The output text is as follows:

```
Deleting intermediate files and output files for project 'btint - Win32 Release'.
Configuration: btint - Win32 Release
Compiling
awgnchan.cpp
basetype.cpp
bluetooth.cpp
ieee802_11b.cpp
main.cpp
programargs.cpp
random.cpp
Linking
Creating browse info fi
btint.exe - 0 error(s).
```

The bottom window also shows the output of the program execution:

```
Desired signal transmitter/receiver: BT.
Interference transmitter: 802.11.
Number of packets = 1.
Packet length = 160.
Frequency offset (MHz) = 4
Carrier-to-interference ratio (dB) = 100.
Carrier-to-noise ratio (dB) = 300.
Number of bit errors = 0.
BER = 0.00e+000.
Press any key to continue.
```

D:\>btint -c 100 -d 802.11 -i BT -EbNo 6

S/W Demonstration

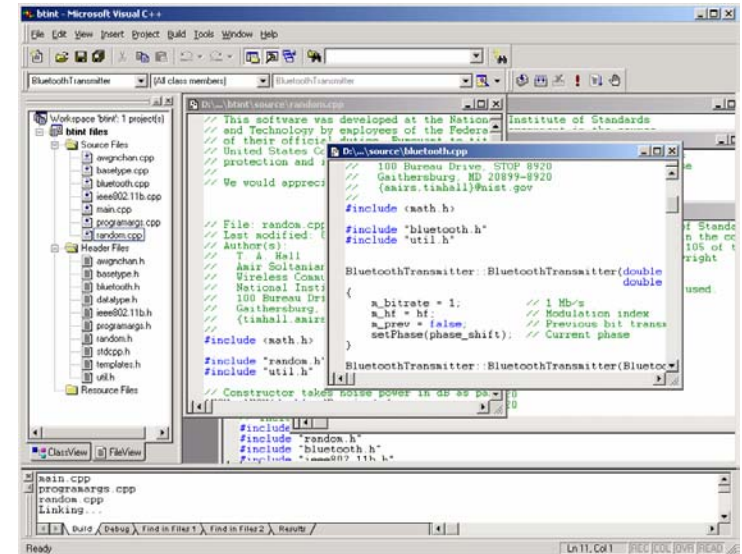
C/C++ Pros and Cons

■ Pros

- Ubiquitous
- Fast to execute
- Data type options

■ Cons

- No canned DSP/Comm functions
- Can't visualize signals
- Too low-level, lots of housekeeping
- Error prone design entry, implicit interdependencies
- Slow to iterate, debug and make changes

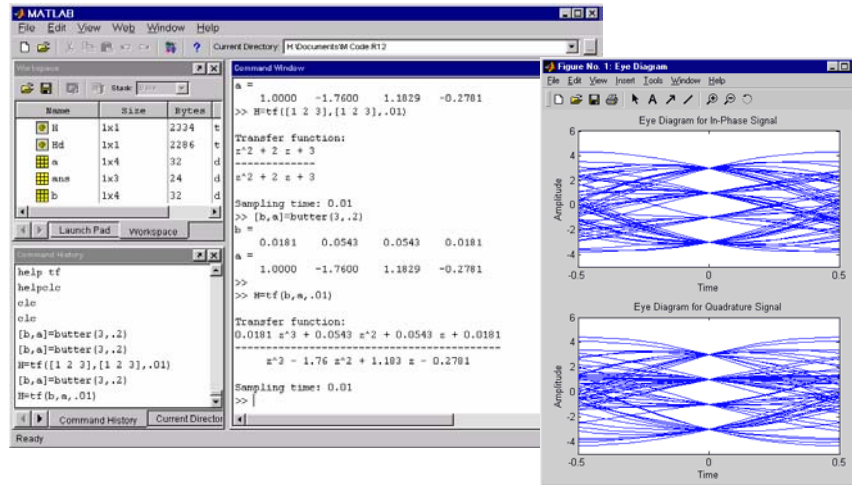




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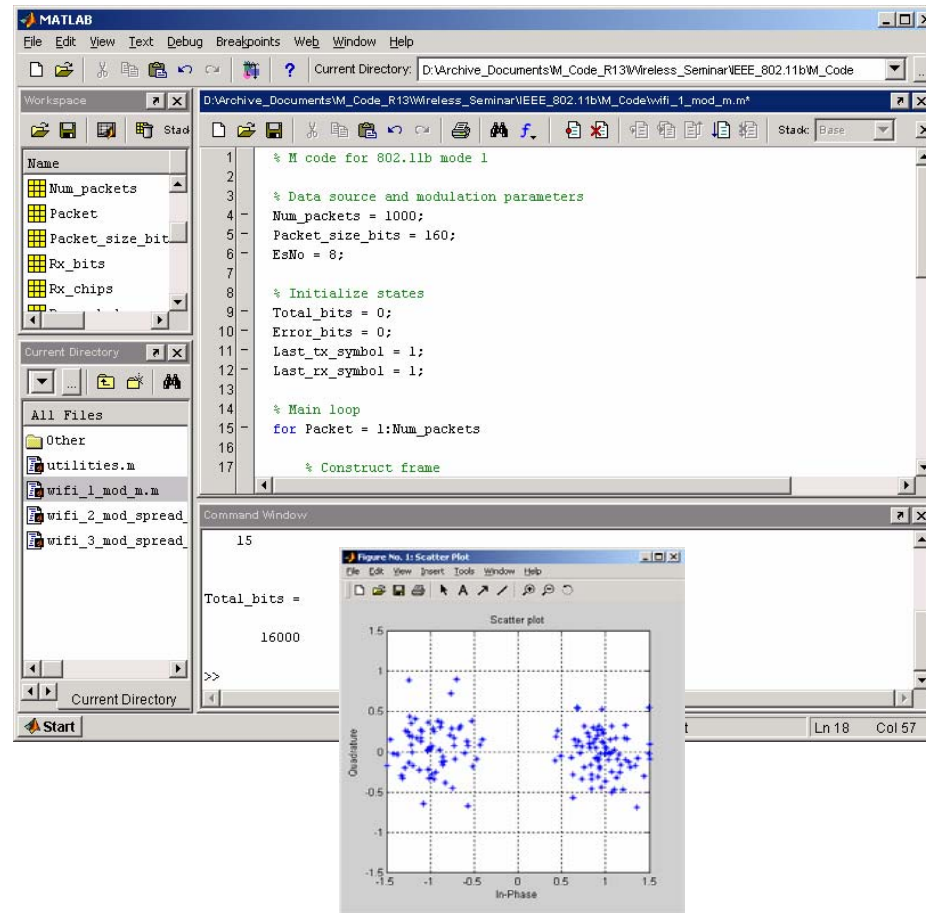


MATLAB



802.11b: M Code

- Using MATLAB
 - Generating bits
 - Symbols and noise
 - `scatterplot(Rx_symbols)`
- 802.11 Tx lines of code
 - One single file 52 lines
 - Modulation (3 lines)
 - Spreading (1 line)
- Speed
 - 2 secs for 100 packets
- Find the bug



S/W Demonstration: Build and show

MATLAB Vs C/C++: Spreading and Upsampling

■ C Code

```
Bits spread=addChips(diffOut[slice(i,1)]);

Bits
IEEE802_11b_Transmitter::addChips(const Bits& input) {
    Bits spreadOut(input.size()*Ns,false);
    for (int i=0;i<input.size();++i){
        for(int j=0; j<11; ++j) {
            spreadOut[i*Ns+4*j]= m_chip[j]^input[i];
        }
    }
    return spreadOut;
}
```

■ M Code

```
Tx_chips=reshape(Barker*Tx_symbols',[],1);
Tx_samples(1:Samples_per_chip:end)=Tx_chips;
```

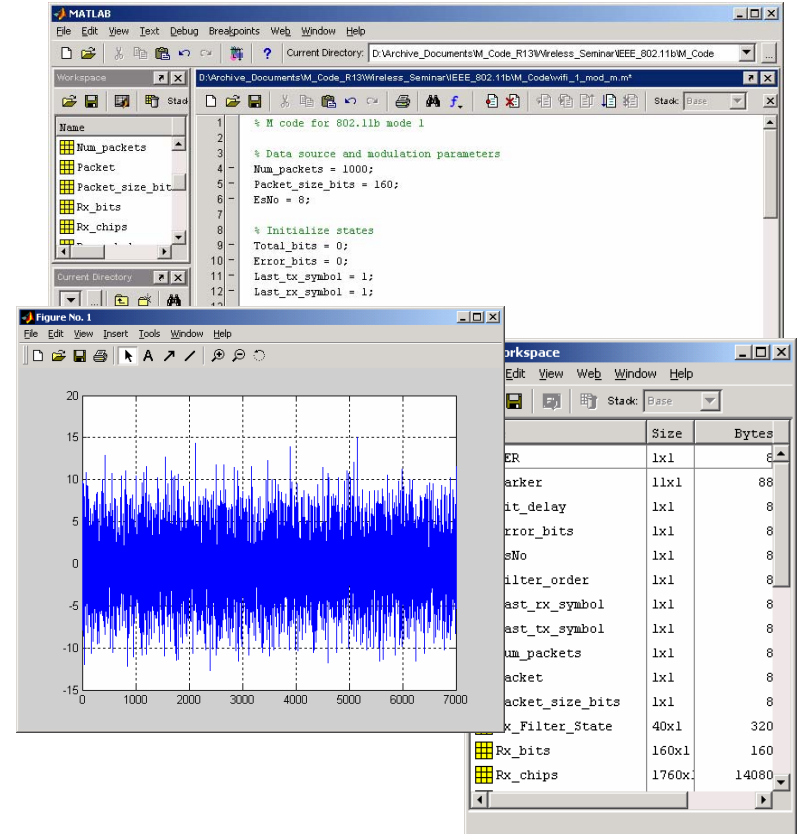
MATLAB Pros and Cons

■ Pros

- Interactive
- Easy signal visualization
- Canned common functions
- Faster development

■ Cons

- Limited data types
- Limited low-level control
- Less memory efficient
- Slower to execute for scalars, loops before R13



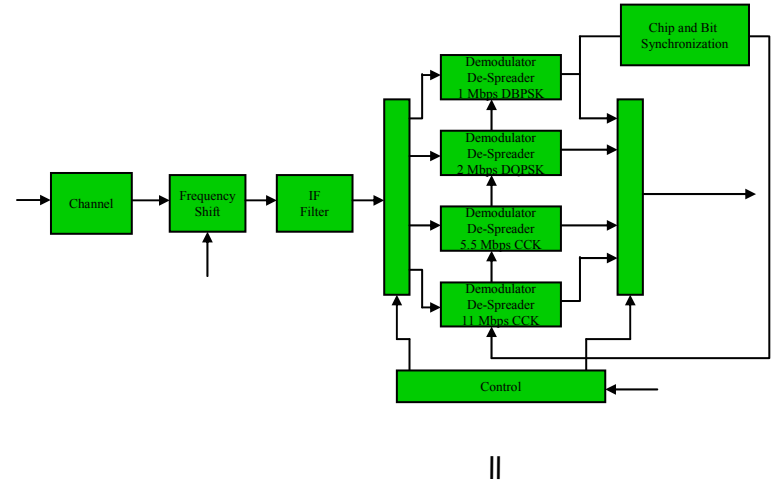
Limitations of C and M for System Design

■ No architecture information

- Can only model a pipeline
- Can't describe a real system

■ No timing information

- Can only model uniform F_s
- Difficult to model delays
- Must manually handle state
- Can't model A/M-S
- Difficult to model Rx algorithms



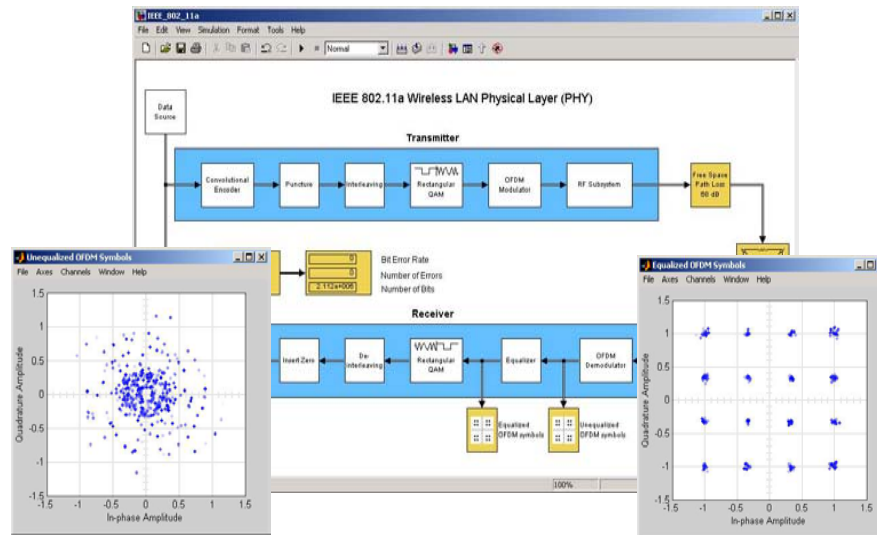
```
% M code for 802.11b mode 1
1
2
3
4 % Data source, channel and modulation parameters
5 Num_packets=100;
6 Packet_size_bits=100;
7 E_bN0=0;
8
9 % Spreading parameters
10 Backer=[1 -1 1 -1 1 -1 1 -1 -1 -1 -1];
11 Spreading_rate=length(Backer);
12
13 % Filter parameters
14 Samples_per_chip=4; % Samples_per_chip to add delay rate vary
15 Bit_delay=1;
16 Filter_order=40; % Multiple of 4
17
18 % Filter coefficients
19 Tx_Filter_state=ones(1,1); % Full filter with n = 1 symbol
20 Rx_Filter_state=ones(1,1); % Full filter with n = 1 symbol
21
22 % Rx chip delay state
23 Tx_chip_delayed_state=0;
24 Tx_state_delayed_state=ones(1,1); % Full filter with n = 1 symbol
25
26 % Initialization states
27 Total_bits=0;
```



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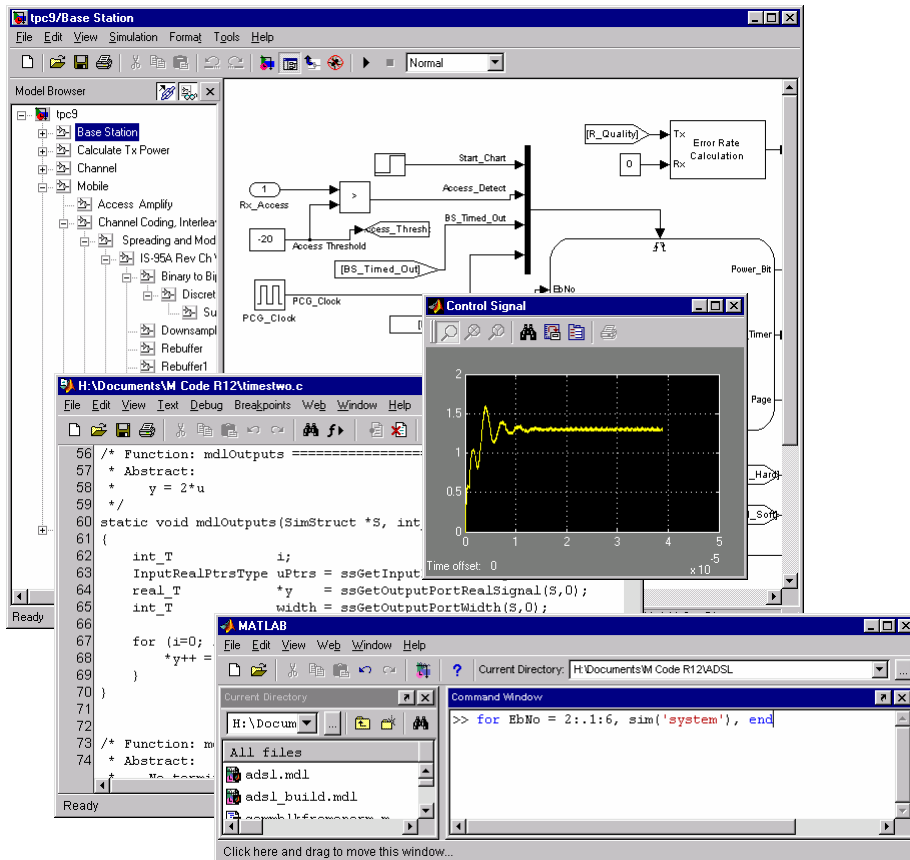


Simulink

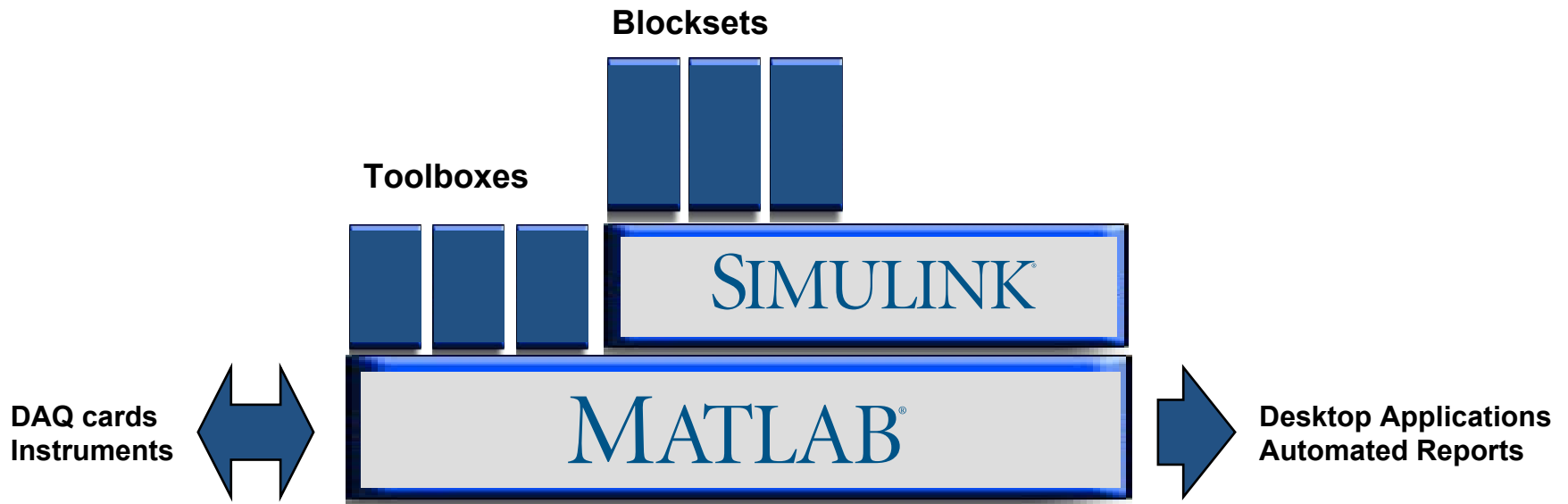


Simulink

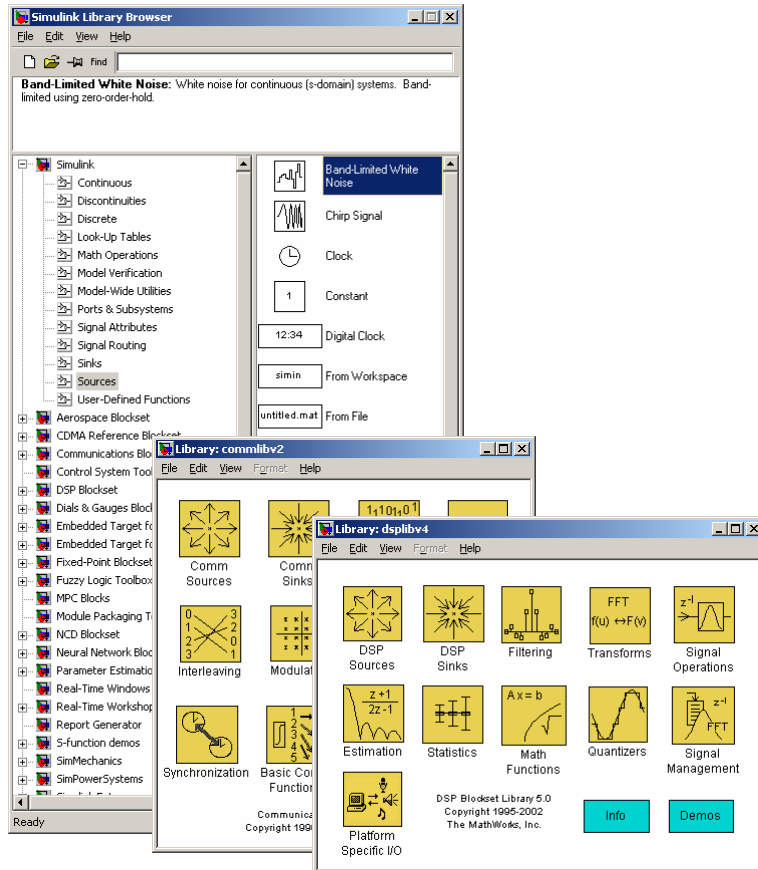
- Hierarchical block diagram design and simulation tool
- Digital, analog/mixed signal and event driven
- Visualize Signals
- Co-develop with C code
- Integrated with MATLAB



Simulink in The MATLAB Environment



The Simulink Block Libraries



■ Simulink

- Sources and sinks
- Continuous and Discrete
- Math, Non-Linear
- Look-up tables, user functions
- Subsystems, verification

■ DSP Blockset

- Sub libraries

■ Communications Blockset

- Sub libraries

■ Fixed-Point Blockset

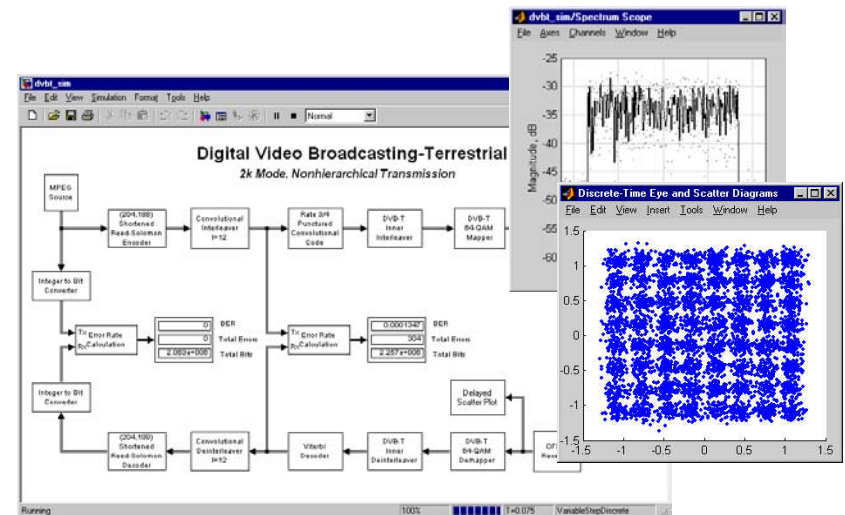
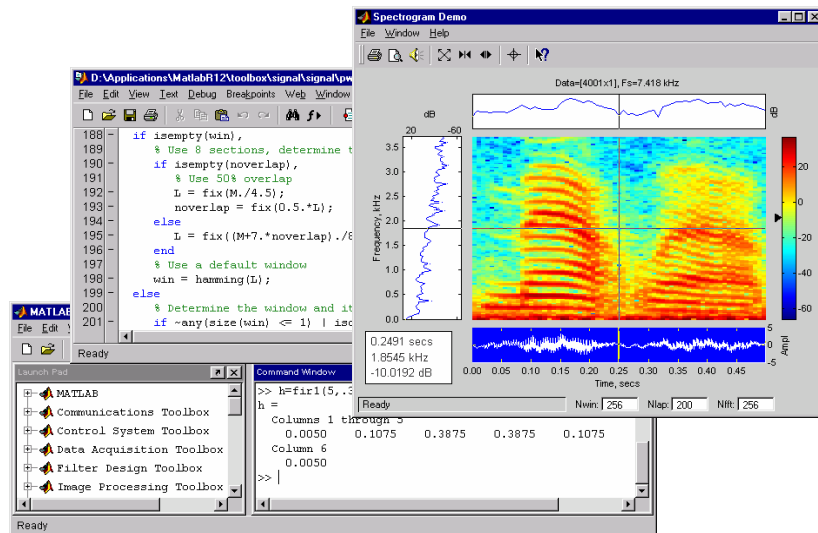
■ Power-Systems Blockset

■ Incremental development

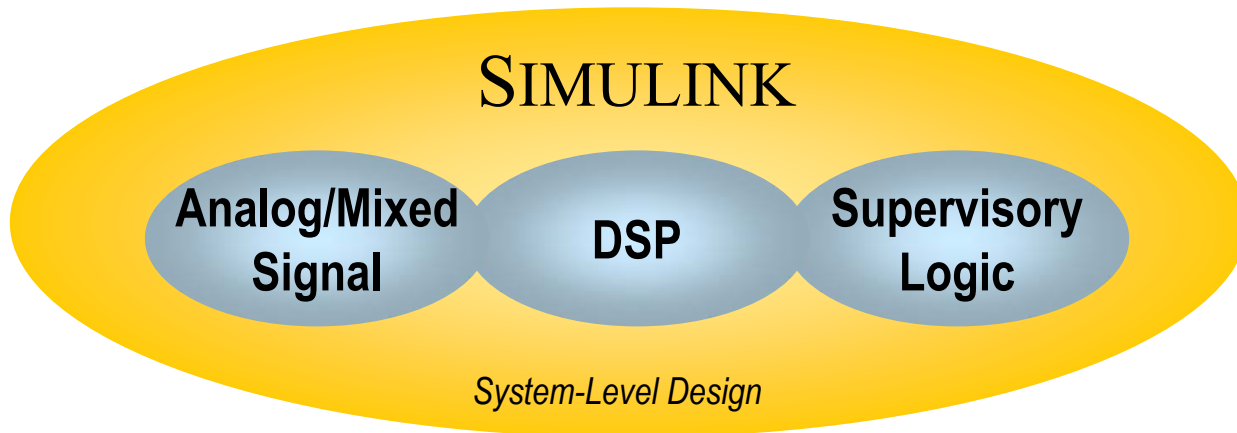
S/W Demonstration: Build

The MathWorks products for DSP and Communications

- Accelerating engineering design and discovery
- MATLAB for algorithm development and analysis
- Simulink for system-level design



MathWorks Integrated Design Solution



Common tool for all design teams
Simulate component interactions
Test behavior of whole system
No re-design necessary

Modeling system components

SIMULINK

Analog/M-S

DSP

Control Logic

■ Analog/Mixed-Signal

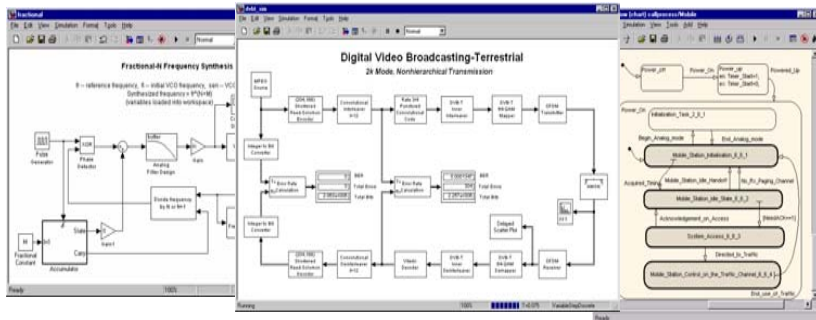
- E.g. PLLs, data converters
- Continuous time, variable-step ODE solvers

■ DSP

- E.g. Baseband processing, speech processing
- Discrete time, fast frame-based processing. Bit-true cycle accurate.

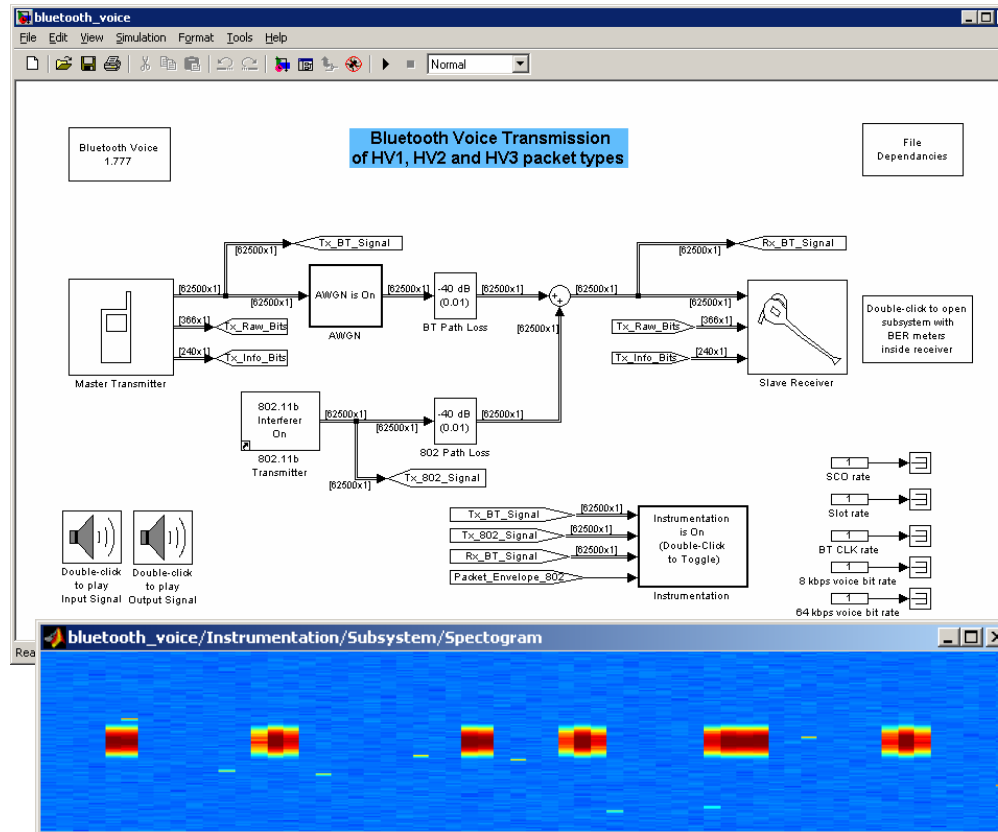
■ Control Logic

- E.g. MAC layer, acknowledgement schemes
- Reactive or event driven state machines



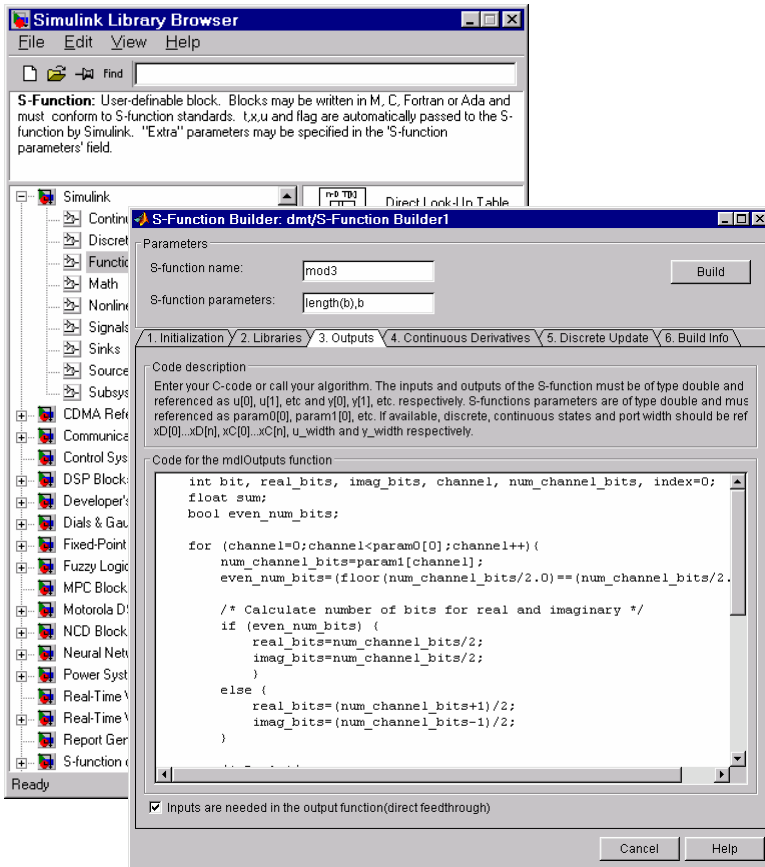
End-to-end systems

- Digital and analog operations such as coding, interleaving and modulation
- Channel models, error coding, sources, sinks
- Multiple rates for frames, symbols, bit and sample rates
- Synchronization
- Performance testing
- Analog, digital, hybrid, and event-driven simulation



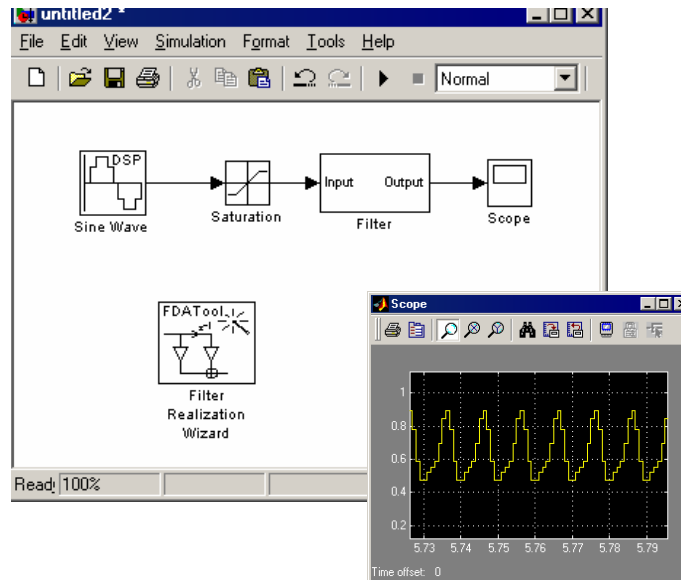
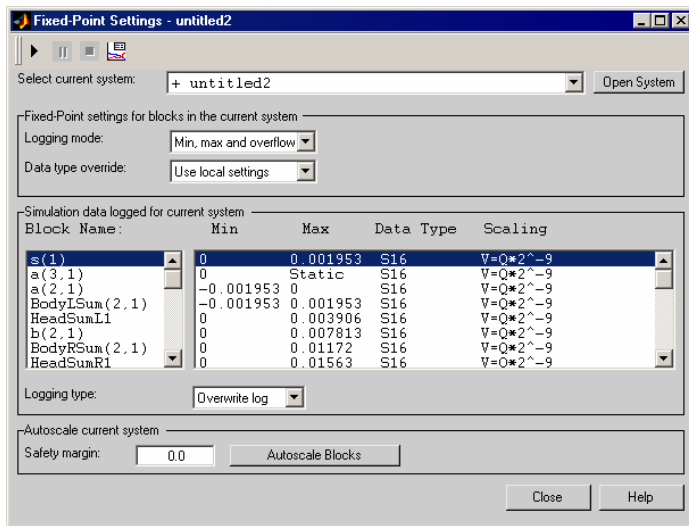
Co-develop with C Code

- S-function block in Simulink
 - API to specify outputs, state, parameters and sample-times
- S-function builder in Simulink
 - GUI to enter C Code
 - Predefined variables for input, output and states



Fixed Point Simulation

- New integrated fixed point in core Simulink (R13)
- User-definable data types
- Analysis tools
 - log min, max, overflows block-by-block
- Floating point override options



Links to implementation

■ Real-Time Workshop

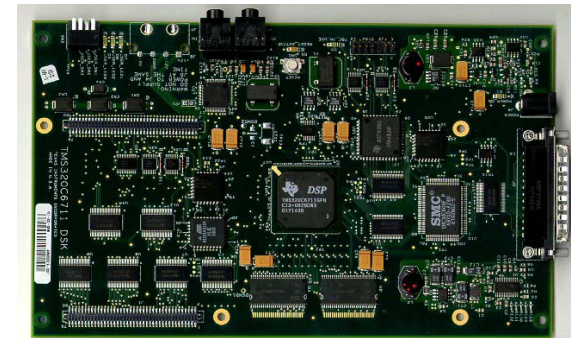
- Automatically generates ANSI C from Simulink
- Customizable code
- Rapid Prototyping

■ Embedded Targets

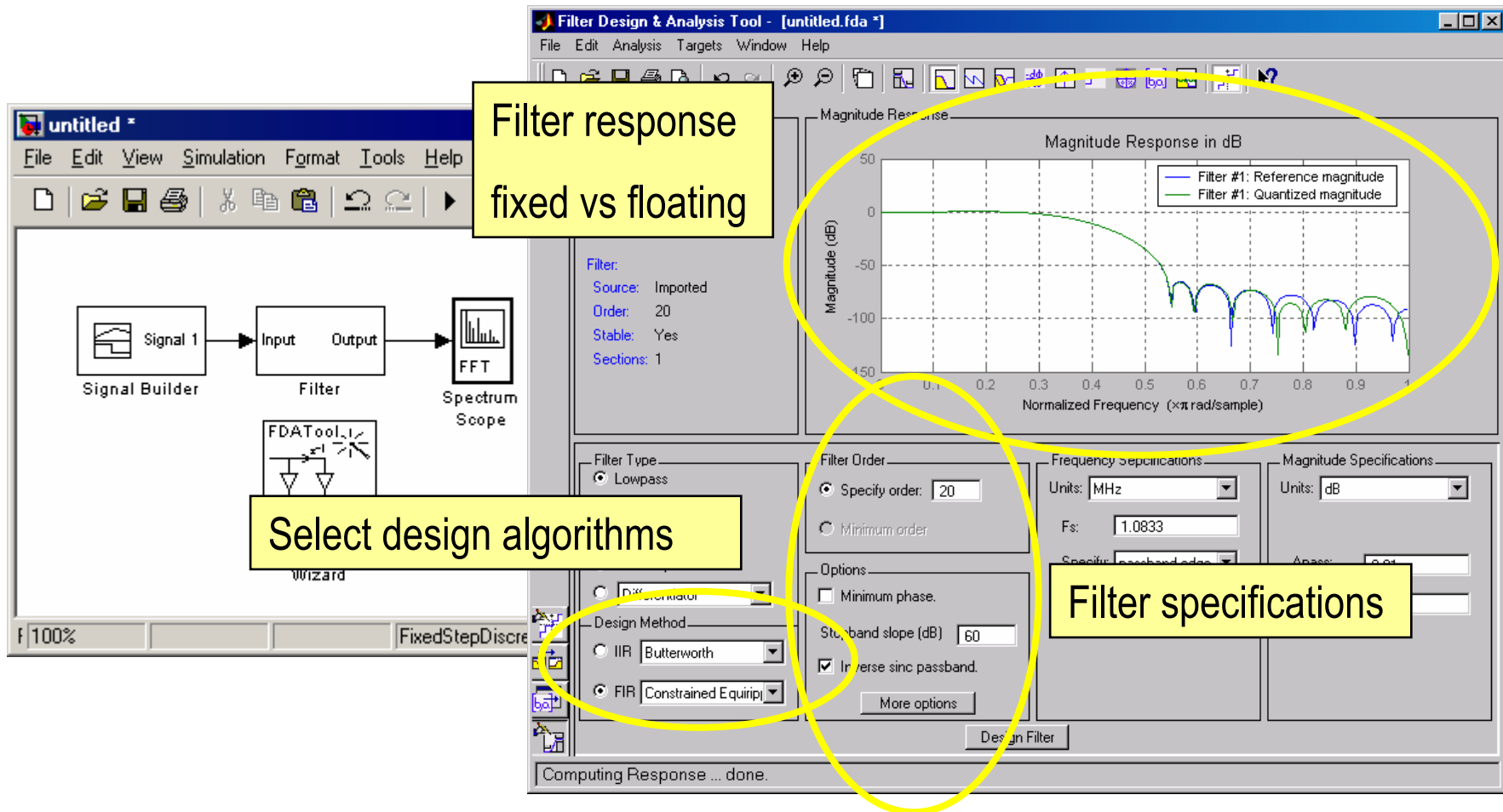
- TI C6000
- Motorola MPC555

■ Altera DSP Builder

- Bit-true and cycle-true Simulink library for common functions
- Automatic HDL code generation from a Simulink model
- Available from Altera



FIR Filter Design: demo



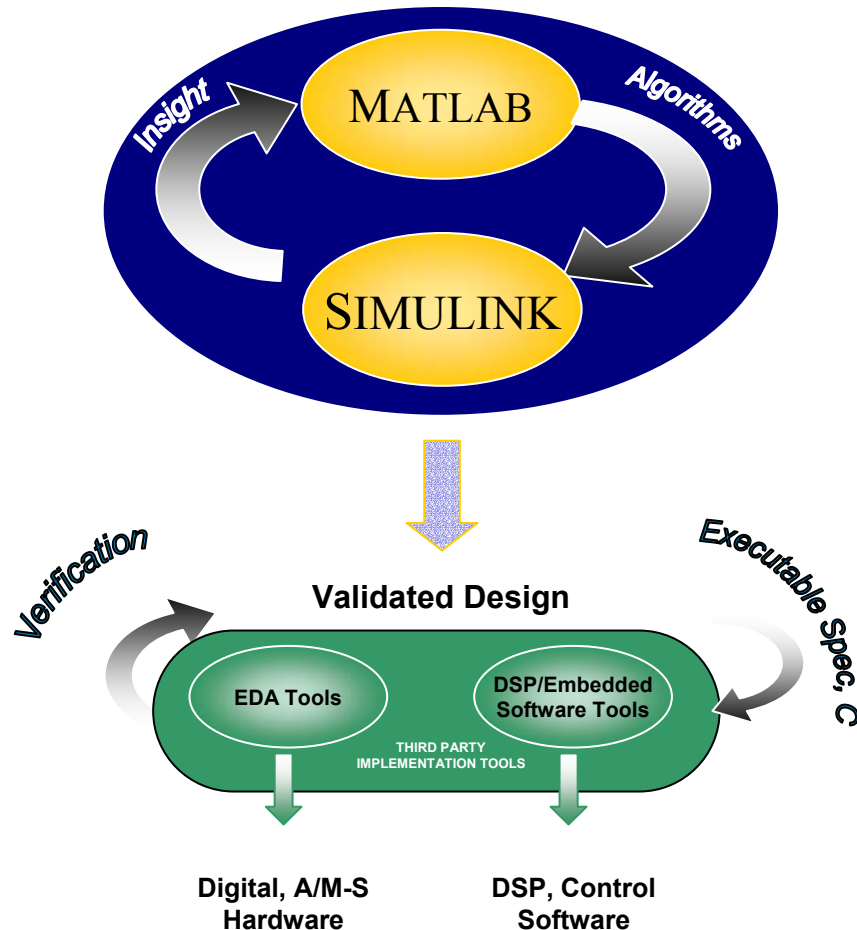


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Summary

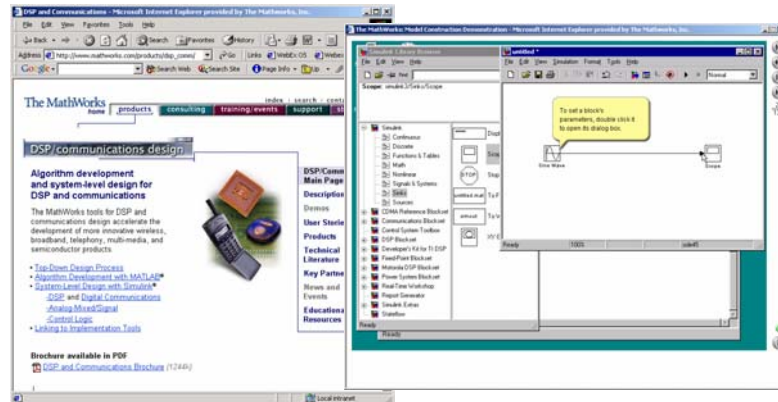
MATLAB and Simulink



- Create validated design
- Use as reference or executable specification to test low-level designs against
- Provide clear specifications
- Detect design flaws early
- Reduce risk and time-to-market

Further Information on Products and Services

- Product information and animated demonstrations
 - www.mathworks.com/products/dsp_comm
- Events
 - www.mathworks.com/dsp_events
 - Regular on-line software demonstrations



MATLAB Central

- www.mathworks.com/matlabcentral
- MathWorks and user contributed models

