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Synplicity®

Incremental Synthesis

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In the next 45 minutes . . .

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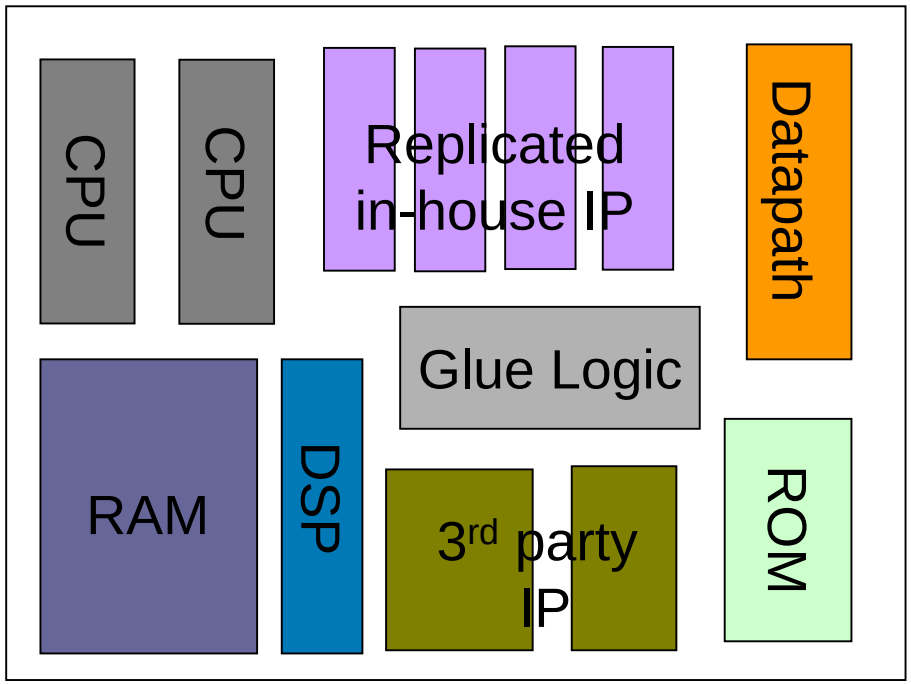
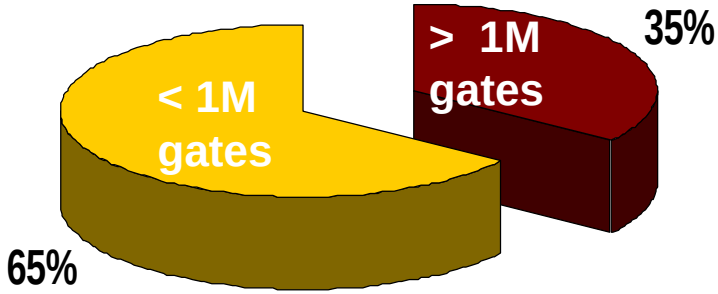
- SOPC designs – The Challenge for FPGA Synthesis
- The Top-Down ‘v’ Bottom-Up Trade-off.
- Introducing MultiPoint™ Synthesis
  - Unlimited Capacity
  - Fast
  - Incremental
- Demonstration of Synplify Pro V7.2 including the Multipoint technology

The SOPC Challenge for Synthesis



Size of designs being done today



How do you integrate, analyze and optimize your multi-million gate design?

Source:Dataquest 2001 (ASIC gates)

Flow choices for SOPC . . .

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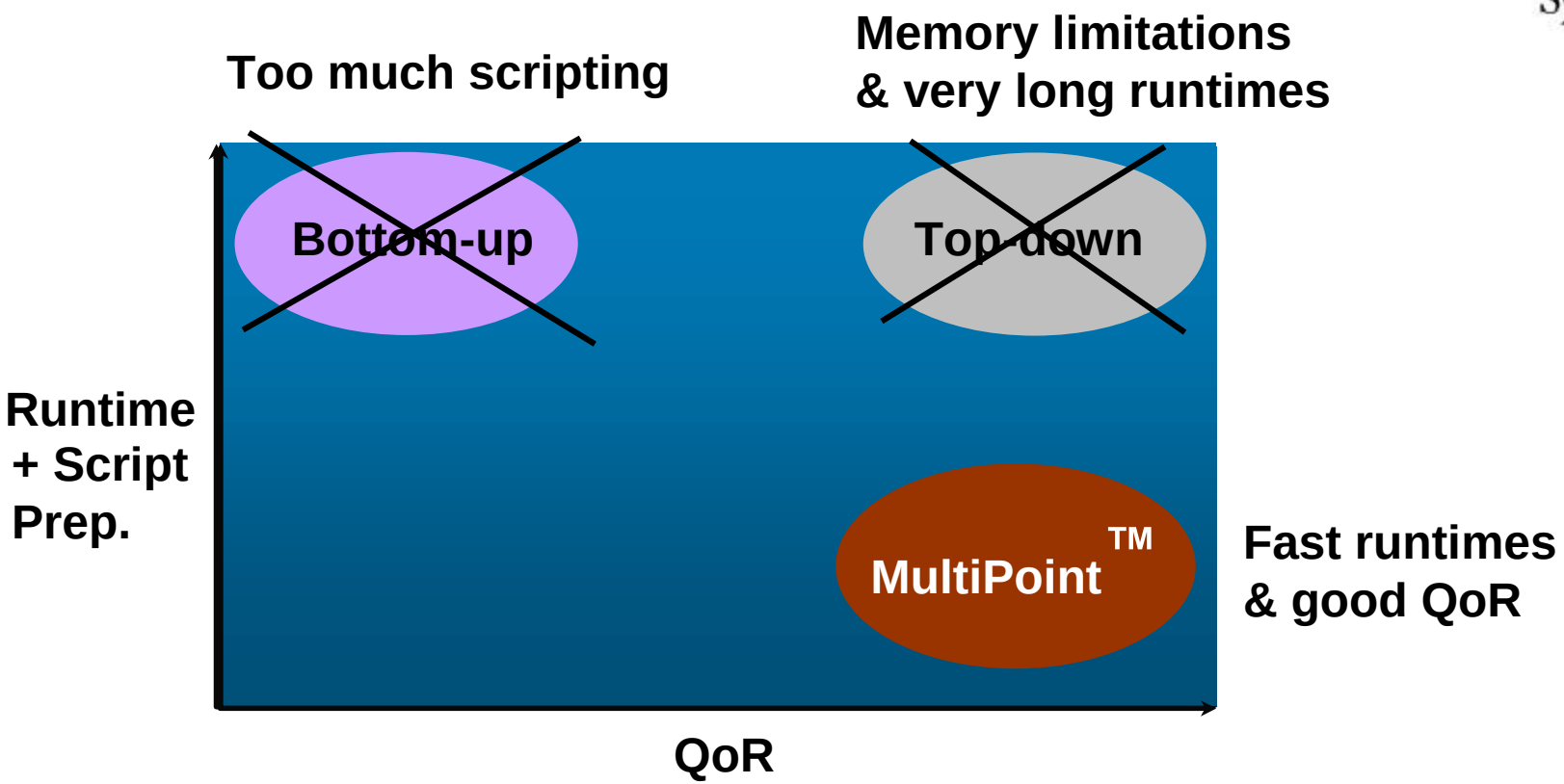
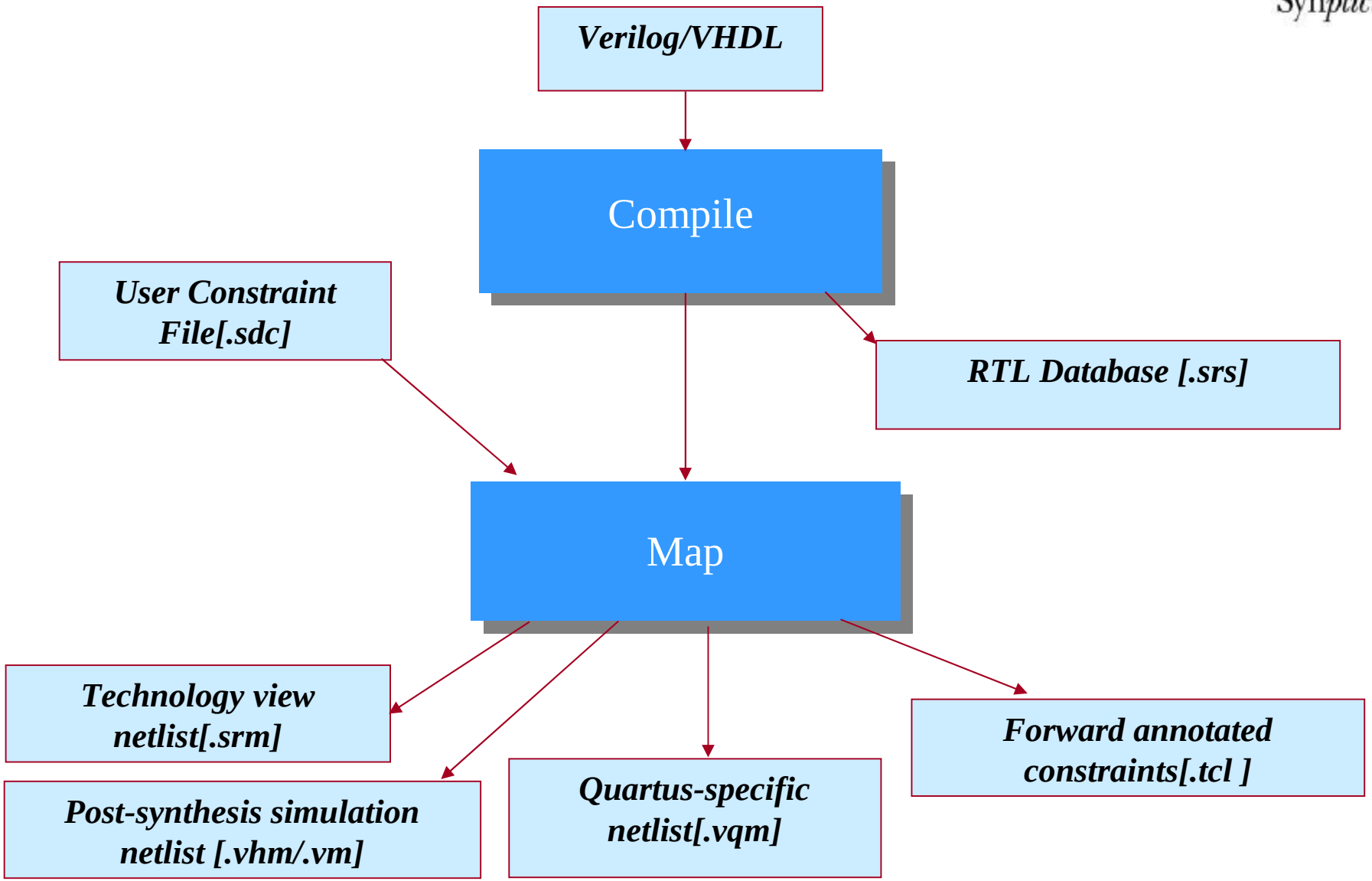


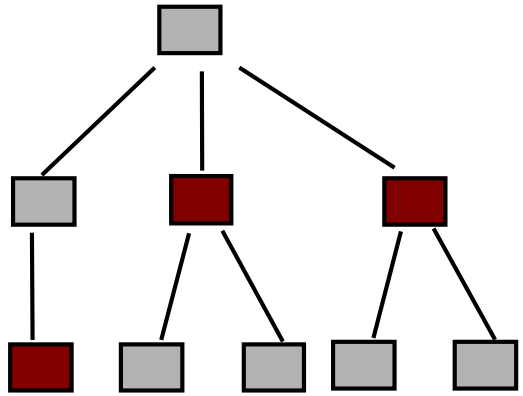
Multipoint Synthesis removes methodology trade-off's for large designs

Synthesis flow reminder



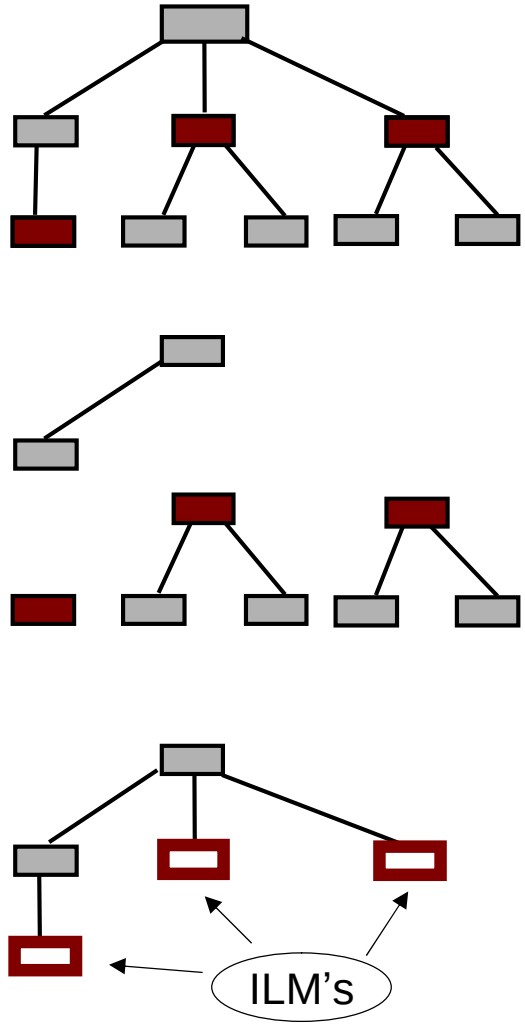
What is MultiPoint™ Synthesis ?

- Hierarchical synthesis methodology for large designs
- High capacity synthesis
- Incremental synthesis
- User defined Compile Points
  - Soft: Allows full boundary optimization
  - Hard: Allows boundary optimization while maintaining ports
  - Locked: No boundary optimization



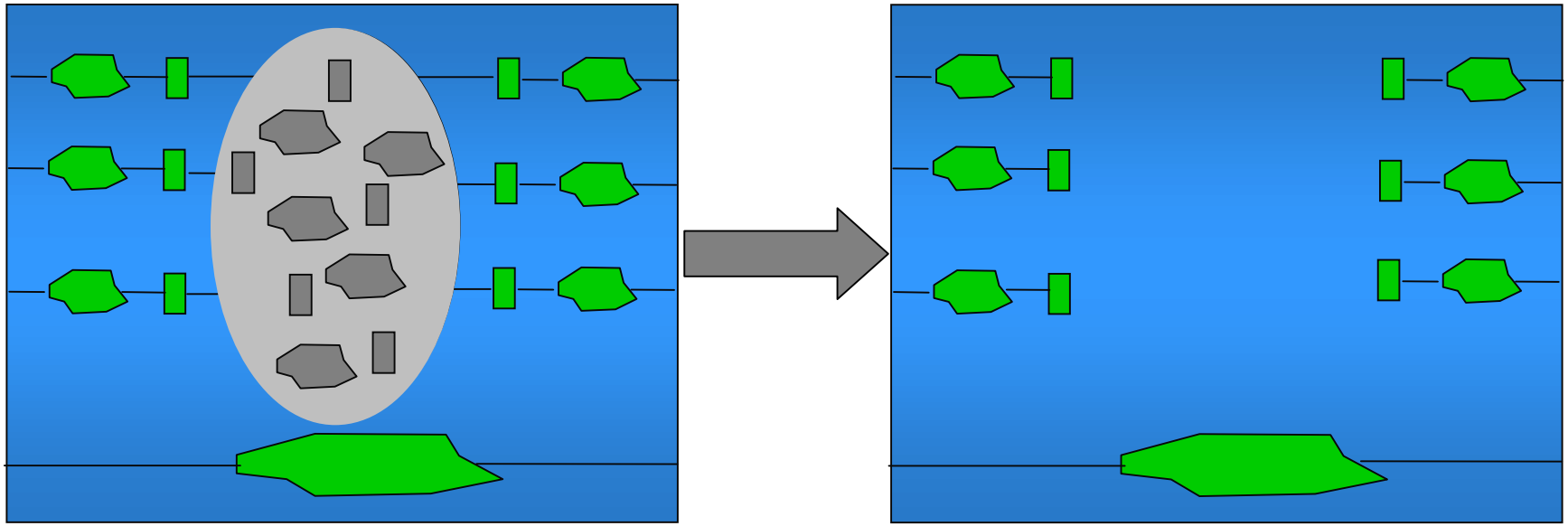
MultiPoint™ Synthesis steps

- Compile HDL, create RTL view
- Define Compile Points
  - (Automatic time-budgeting)
- Map each compile point
  - Only if required
- Create ILM's and insert into Top-Level
- Optimize Top-level and perform chip-wide timing analysis



ILM Creation In MultiPoint™

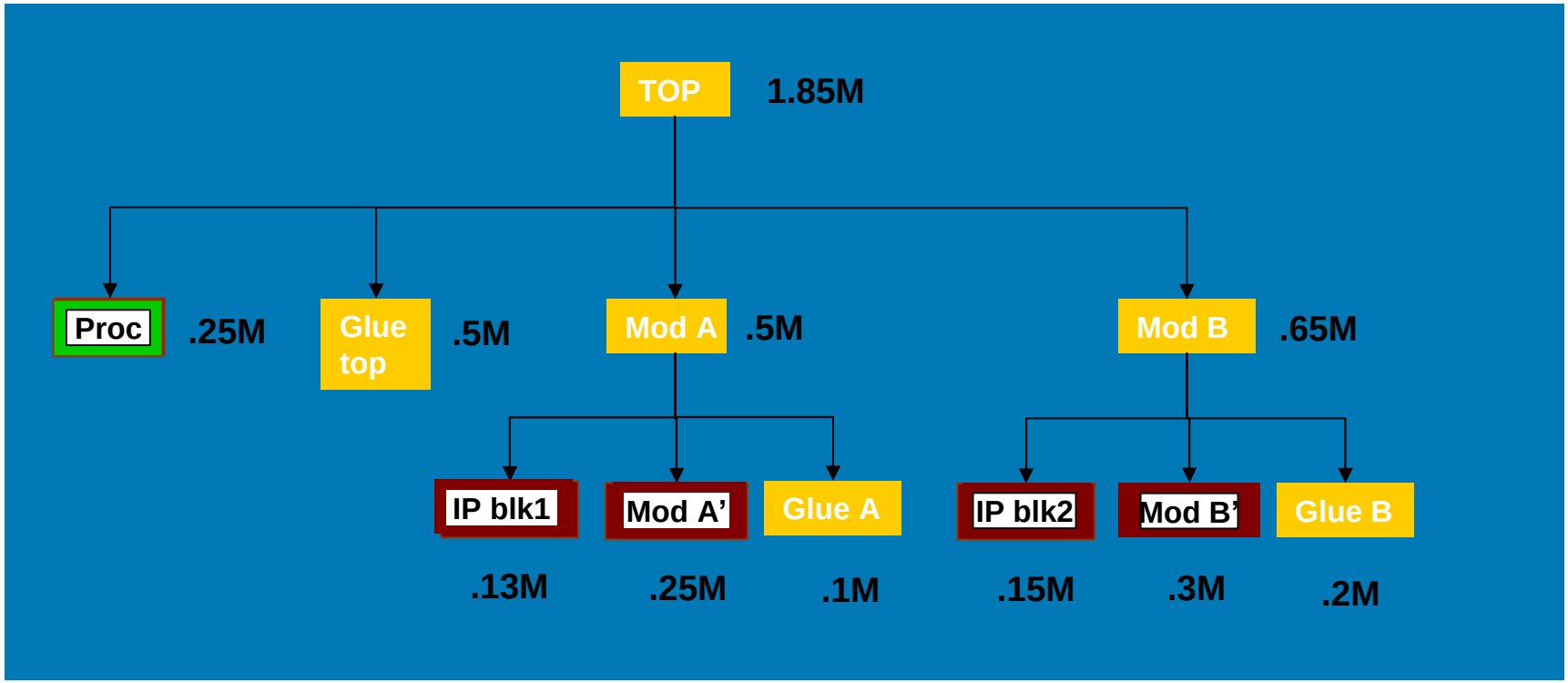
ILM is a key technology used in MultiPoint™ Synthesis



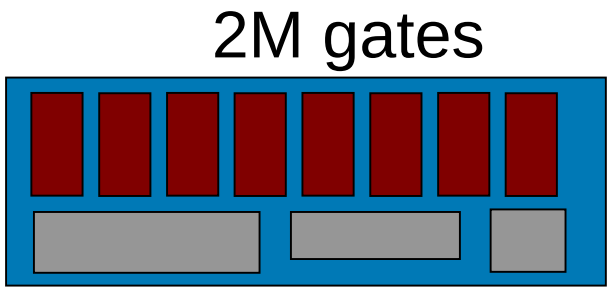
Synthesized Design

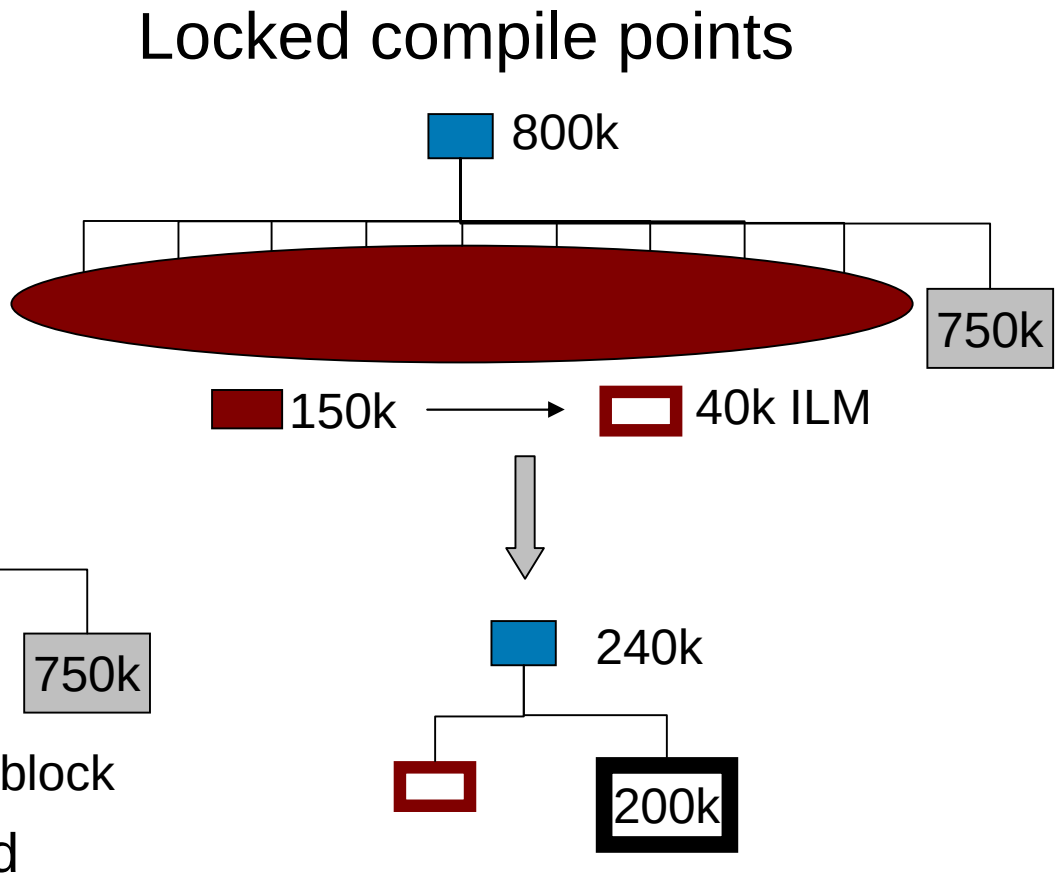
ILM average 25% of block

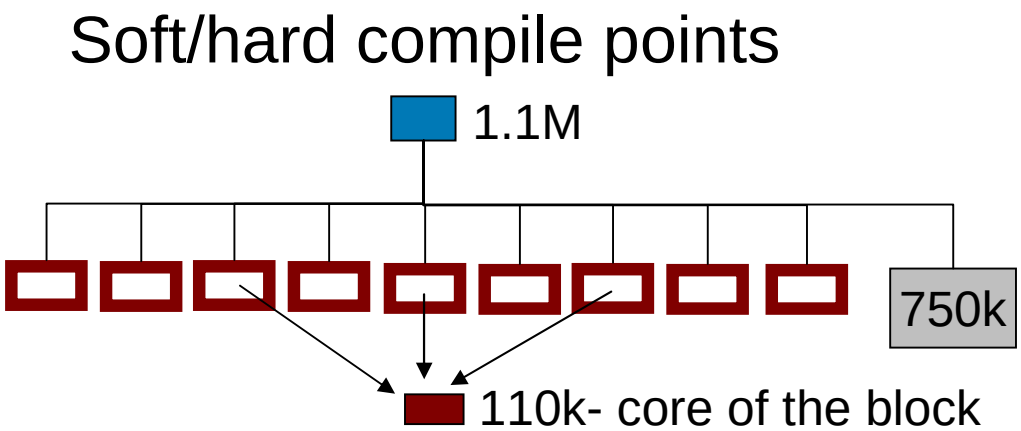
MultiPoint™ has Huge Capacity



MultiPoint™ with replicated blocks



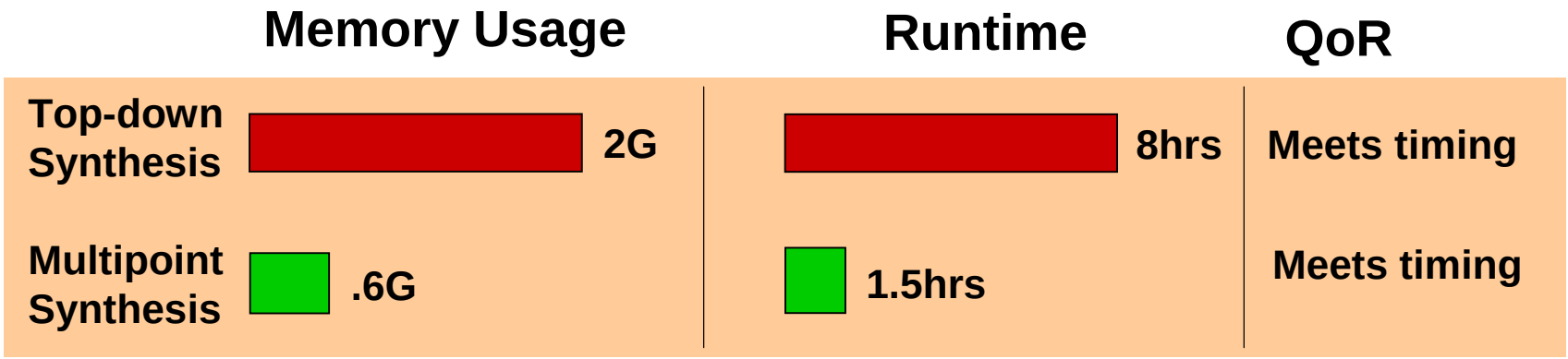




Replicated block is mapped once and then replicated followed by boundary optimizations

MultiPoint™ is Fast

- 2M gate design, 125 MHz
- 150k block replicated 9 times specified as a compile point



Incremental Synthesis

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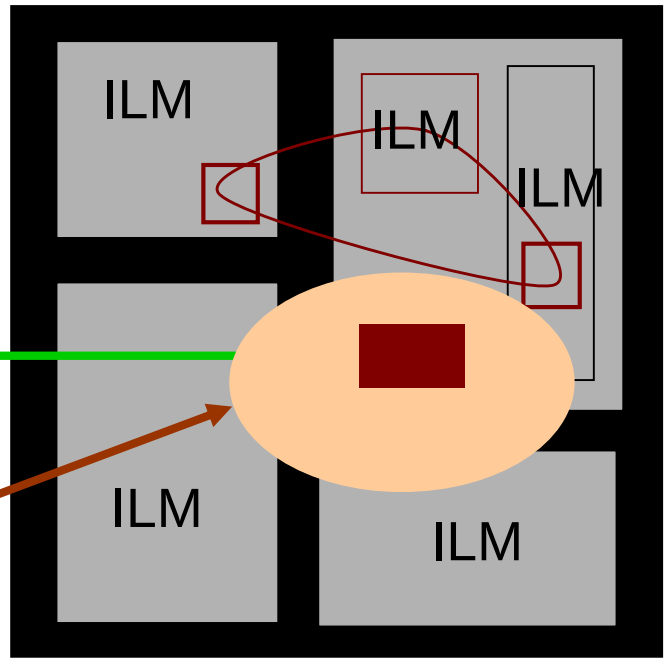
- At the end of the design cycle
  - most of the design has been verified
  - most of the design has met timing
- Minimize changes using Incremental flow



Change only this block

Connectivity of the block

Use ILM's for all other blocks and mark them as locked compile points

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Difference-based Synthesis

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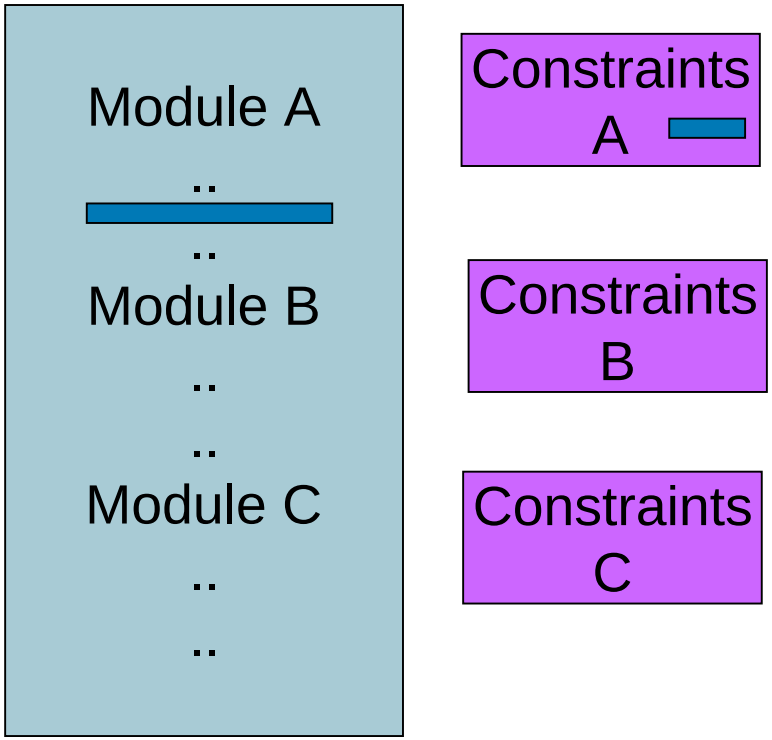
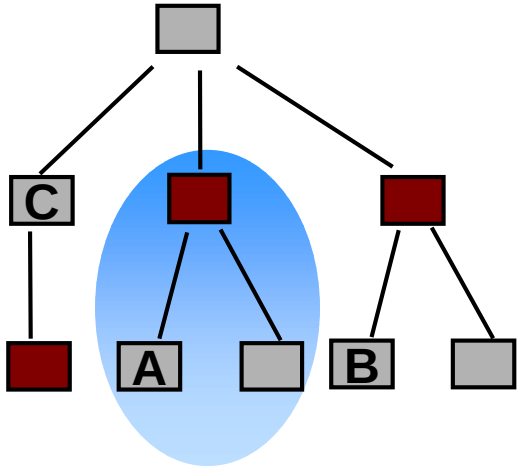
Verilog/VHDL file



Constraints A

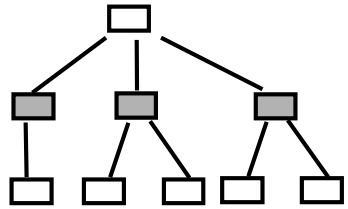
Constraints B

Constraints C

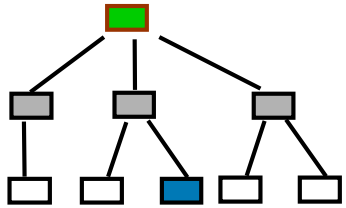


Incremental Synthesis based on Comparison of RTL, Constraints & Properties
NOT JUST DATE STAMP

MultiPoint™ is Adaptable



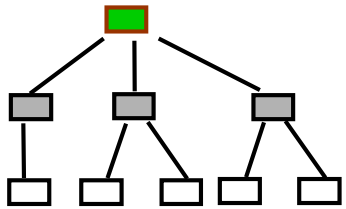
Top-down synthesis
of modules up to 1M gates



ECO synthesis to
fix localized problems

RTL → Implementation in HDL → Integration → Debug → To P&R

Top level integration of
modules using Multipoint
synthesis



MultiPoint™ is Unique

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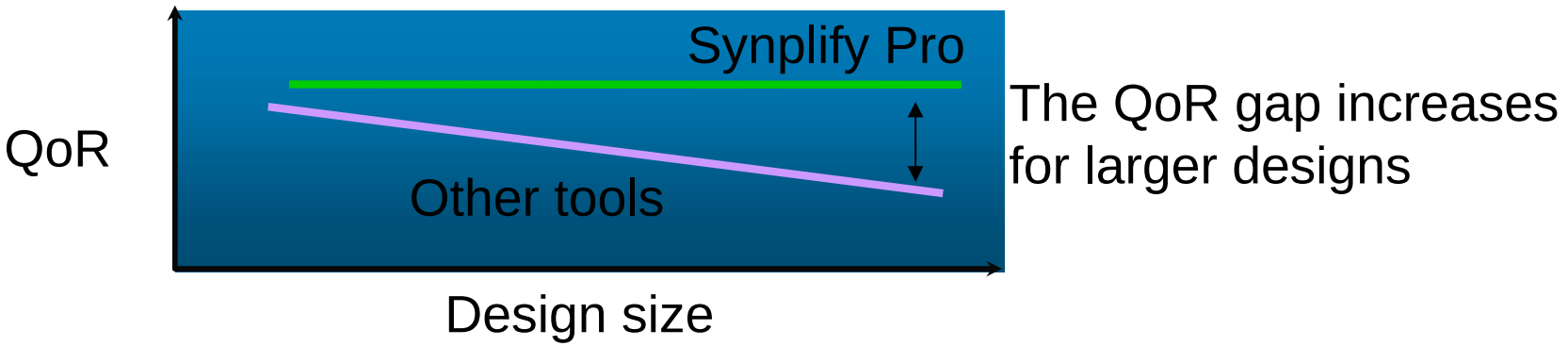
Only the Synplify Pro® solution has these capabilities:

- Ability to synthesize million gates top-down
- Ability to auto-create and use ILM's during synthesis
- Difference-based incremental synthesis



Enables fast synthesis of very large designs without compromising QoR

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MultiPoint™ Synthesis features

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Feature	Benefit
Use of Interface Layer Models (ILM's)	• Needs less memory = Increased capacity • Faster synthesis without loss of QoR
Difference-based Incremental Synthesis	• Only altered modules are re-mapped
Auto Time-budgeting*	• No need for manual constraints creation • No wasted Area because of over-constraint
Hard / Soft Compile Points *	• Allows cross-boundary optimization

* Not in first release

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Multipoint in Action

Demonstration of Synplify Pro V7.2

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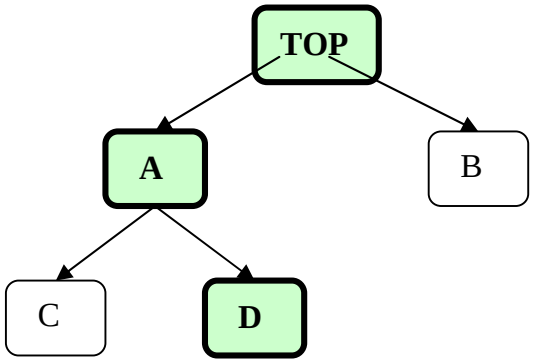
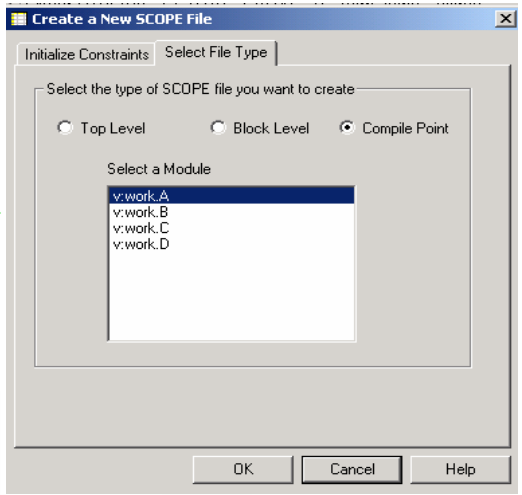
Demo Summary



Enabled	Module	Type
☑	v:work.A	locked
☑	v:work.D	locked

Define compile points and compile point constraints



First Run

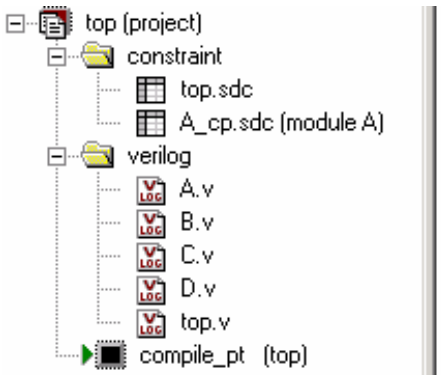
```
 Summary of Compile Points

Name      Status      Reason
-------------------------------
D         Mapped      No database
A         Mapped      No database
top       Mapped      No database
===============================
```

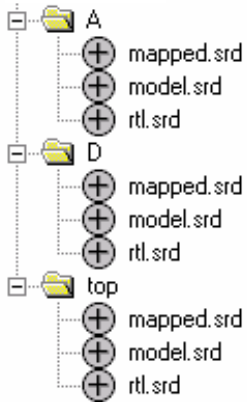
Second Run

```
 Summary of Compile Points

Name      Status         Reason
-----------------------------------
D         Remapped       Design changed
A         Unchanged      -
top       Unchanged      -
===================================
```



Project View



MultiPoint™ Synthesis Summary

- High productivity for large designs
- Same QoR and ease-of-use as top-down synthesis
- First and Only Incremental Synthesis
- All existing flows (bottom-up & incremental) are supported and improved
- Applicable to all Synplicity® Tools

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Thanks for listening

support@synplicity.com

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