SOPC WORLD 2002

FPGA Design – From Concept to Silicon

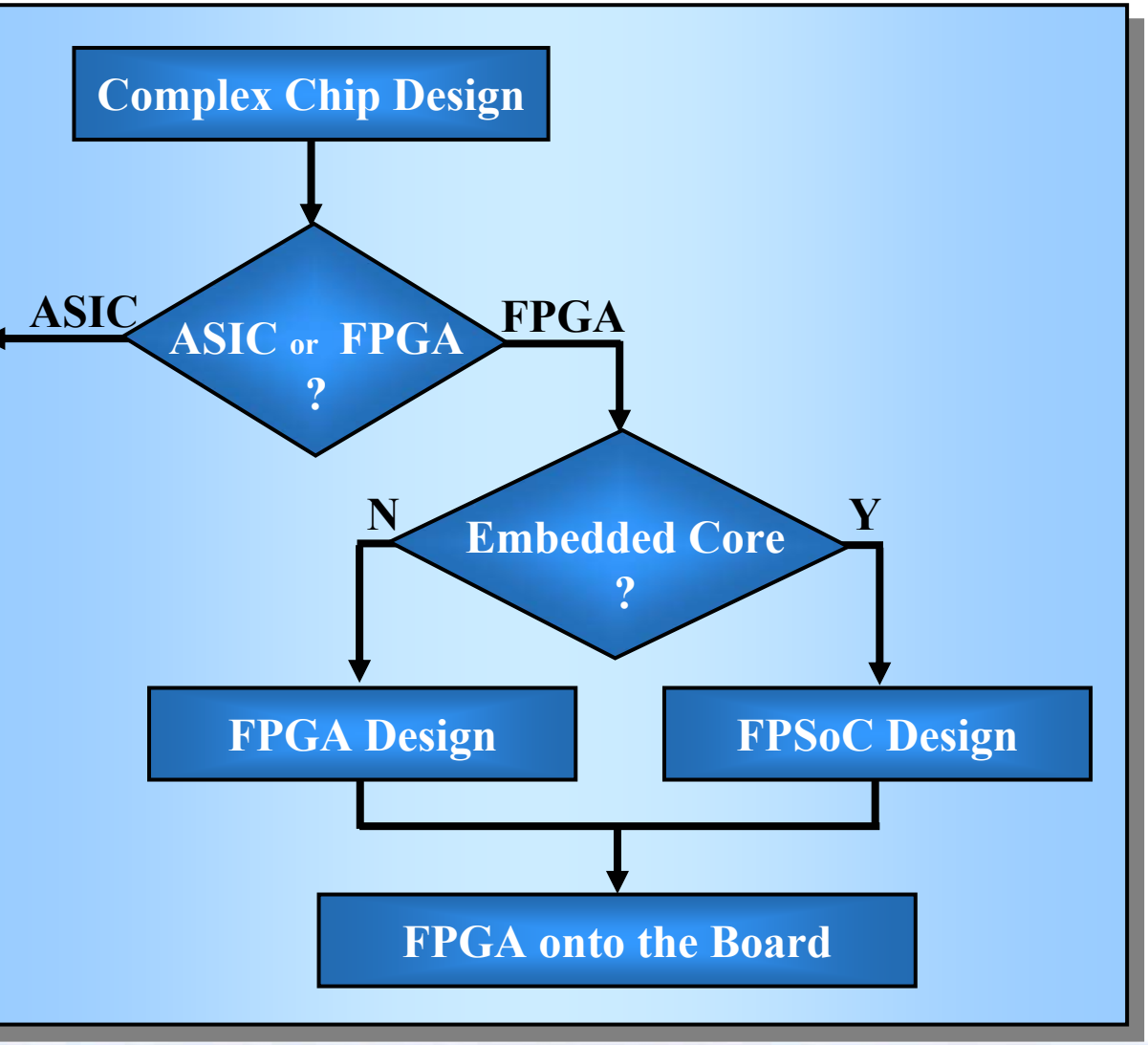
Park Sung Chul

AE

MentorGraphics Korea

Mentor Graphics®

The Challenge of Complex Chip Design



- Considerations
  - ASIC or FPGA
  - On-chip or off-chip µProcessor
  - Design and verify chip on board

What Are Your Chip Technology Choices?

- Gate Array
- Standard Cell
- PLD / FPGA

"The long-term prospects for growth in the FPGA market are good since the trend is towards placing more programmable and reconfigurable logic to allow designers to cope with ever-shortening design cycles and product life cycles."

Semico Research Corp
2001 ASIC Market Share Report
March 2002

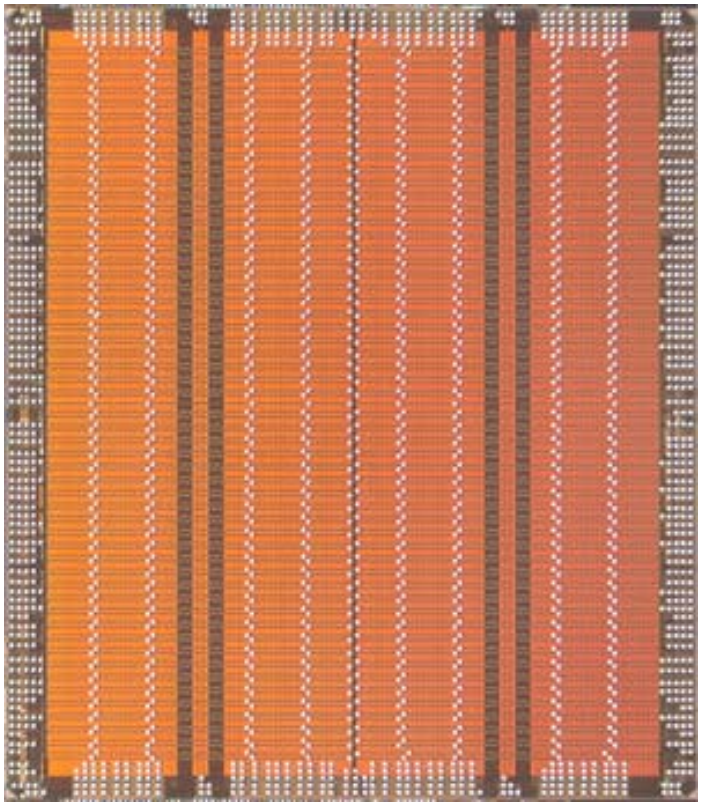
ASIC Design Realities

- Out of reach for majority of the market
  - 12 to 18 months design cycle
  - ≈ $1,000,000 mask set cost
  - Maximum performance
  - Minimum volume cost
  - Experience
    - Co-Simulation
    - Co-Verification
    - Prototype
  - High Risk
- Semico estimates 5K ASIC design starts in 2002

Source: Semico Research Dec. 2001

New FPGA Design Realities

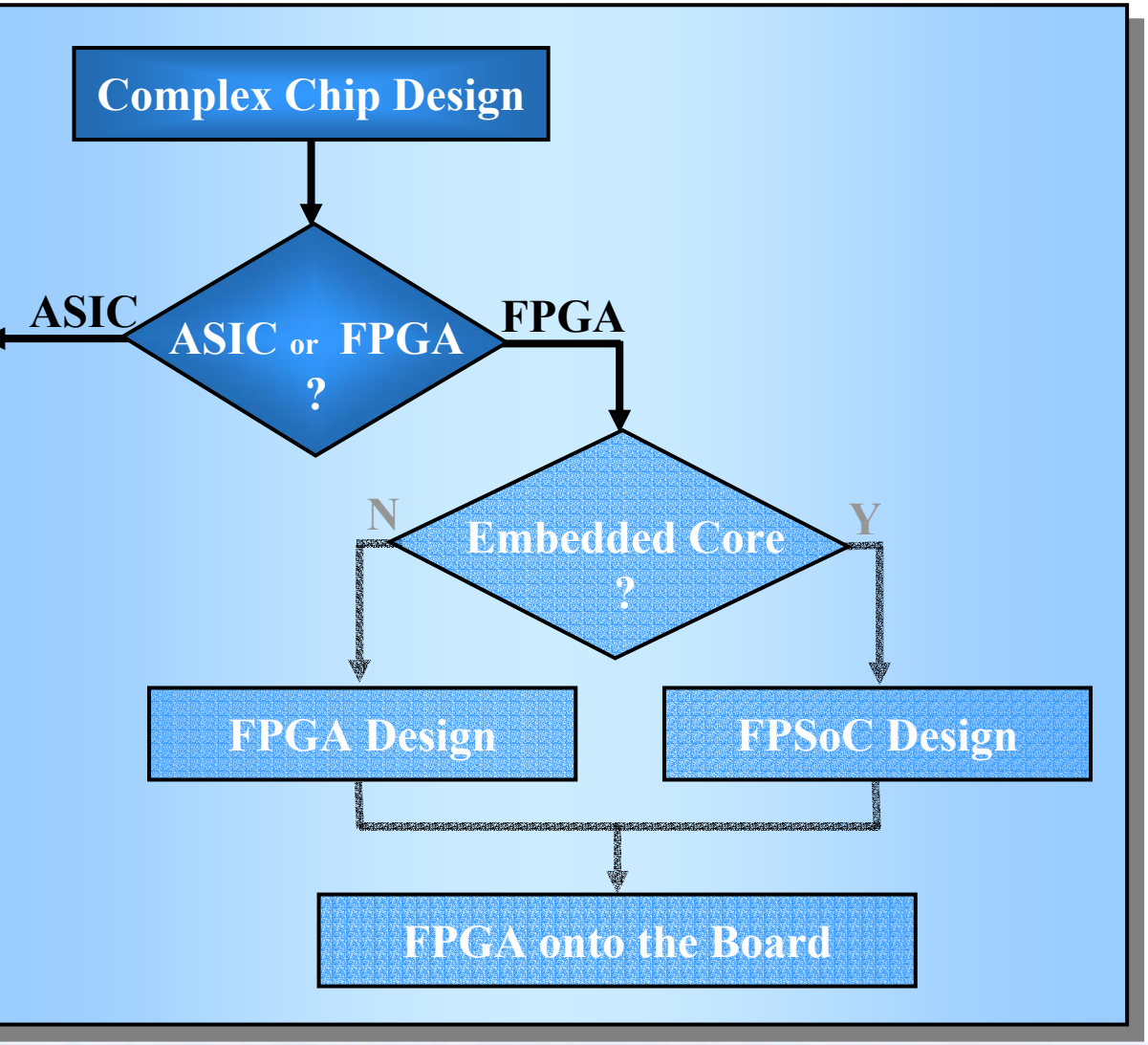
- In reach for majority of the market
  - Shorter time to market
  - No mask set cost
  - Impressive performance
    - 350 MHz internal frequency → 400 MHz
    - 3.1 GHz external frequency
  - Very good capacity
    - Multiple embedded CPUs
    - 1500 pins → 2500 pins
    - 6 M gates → 50 M gates
    - 130 nm → 90 nm



- Semico estimates 32K design starts in 2002

Source: Semico Research Dec. 2001

The Lure of FPGAs



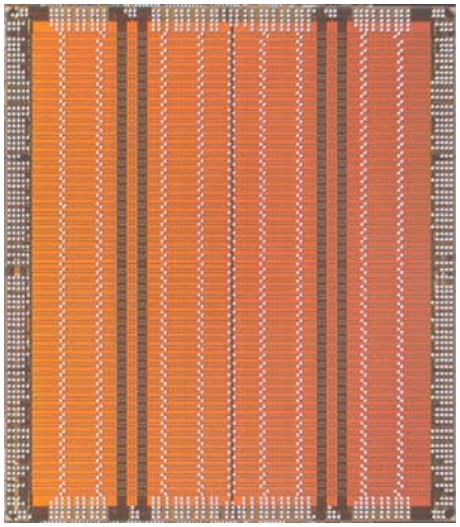
- Faster time to market
- Comparable ASIC performance
- "Forgiving" technology
- Flexible solution
- Volume friendly

FPGAs As The Mainstream Semi-Custom Component

1996:

- 100k-gate
- 5 MHz

→ *$200 per processor MHz*

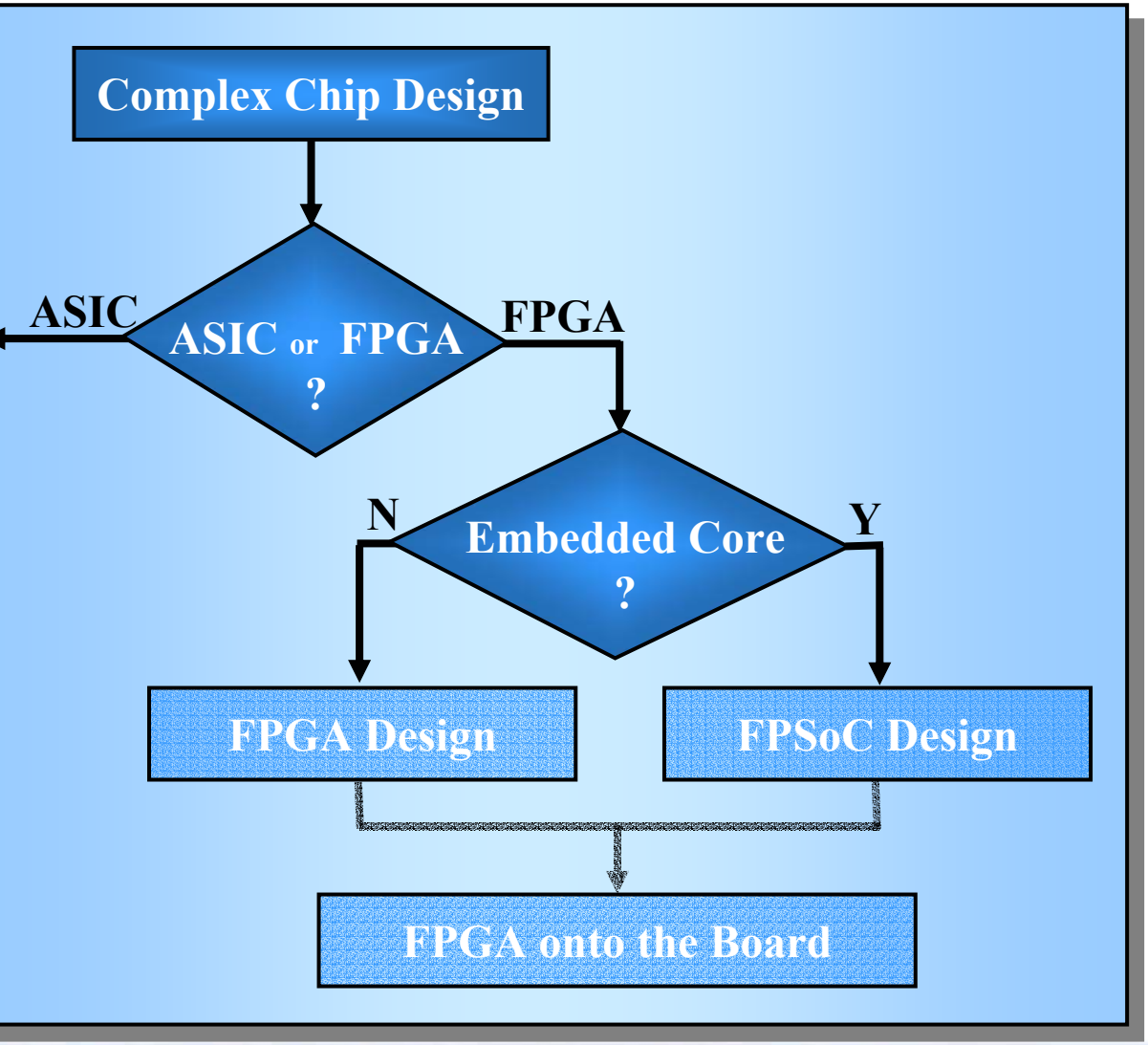


2002: Evolution To Field Programmable SoC

- 6M-gate
- 32-bit embedded microprocessor
- 250MHz

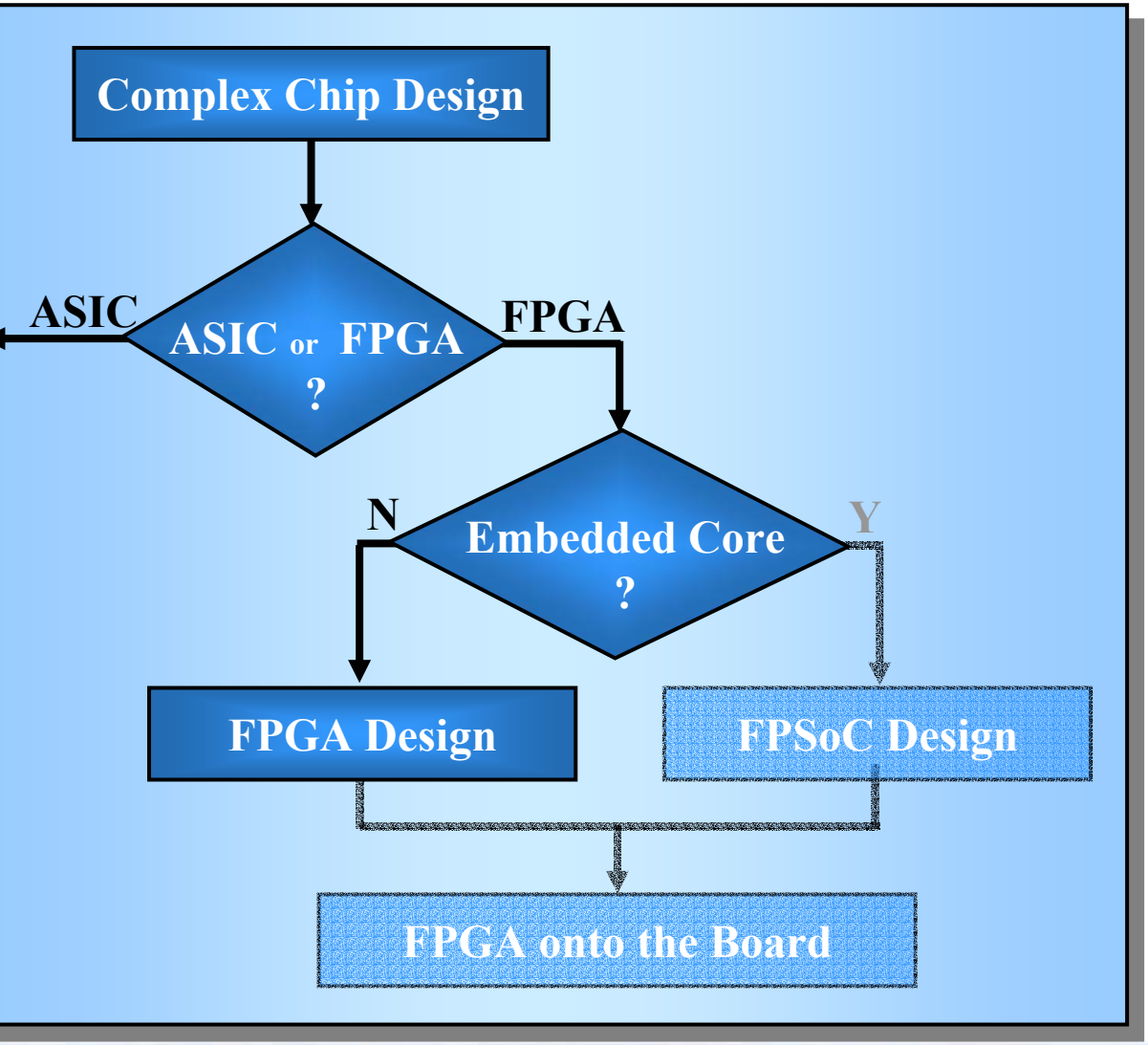
→ *$16 per processor MHz*

FPGA: On- or Off-chip Microprocessor



- **Path 1: Off-chip**
- **Path 2: On-chip**

FPGA with Off-chip Microprocessor

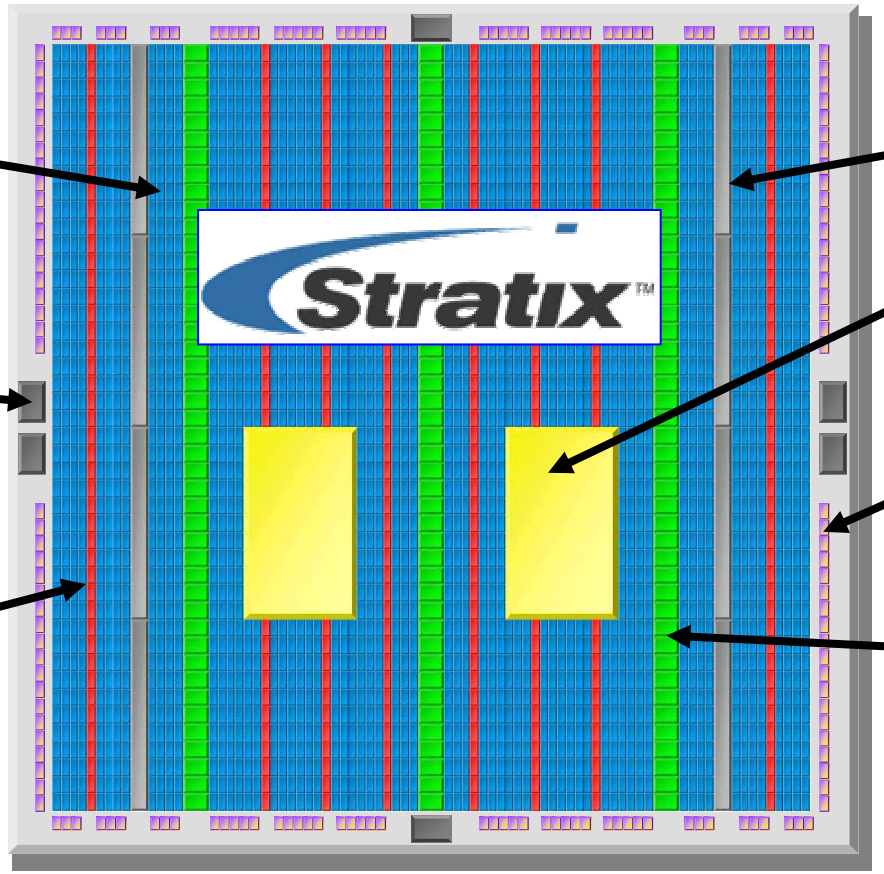


- **Path 1: Off-chip**

Today's FPGA

- Contain
  - Memories
  - DSP elements
  - Clock management
  - High-speed IOs

Altera® Stratix™ Architecture



Logic Array Blocks (LABs)

Phase-Locked Loops (PLLs)

M512 RAM Blocks

DSP Blocks

MegaRAM™ Blocks

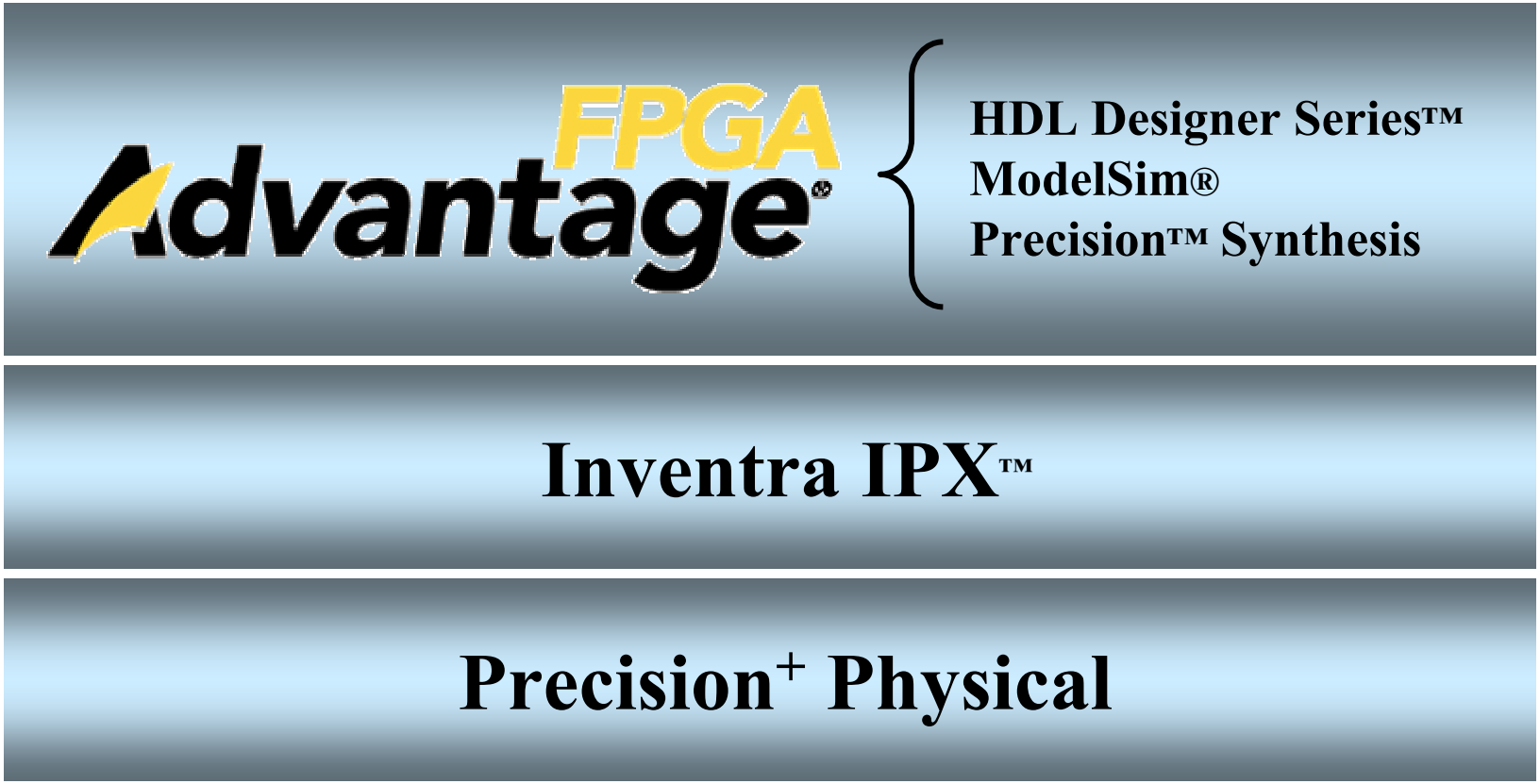
I/O Elements (IOEs)

M4K RAM Blocks

How To Design These FPGAs?

- FPGA design methodology must
  - Deliver a predictable design environment
  - Focus on larger blocks, ie ROMs, RAM, CAM
  - Ease inclusion of IP
  - Link closely to FPGA vendor technology
  - Find critical paths
  - Work tightly with design constraints
    - Result →smaller device or lower speed grade

Mentor's FPGA Design Solutions

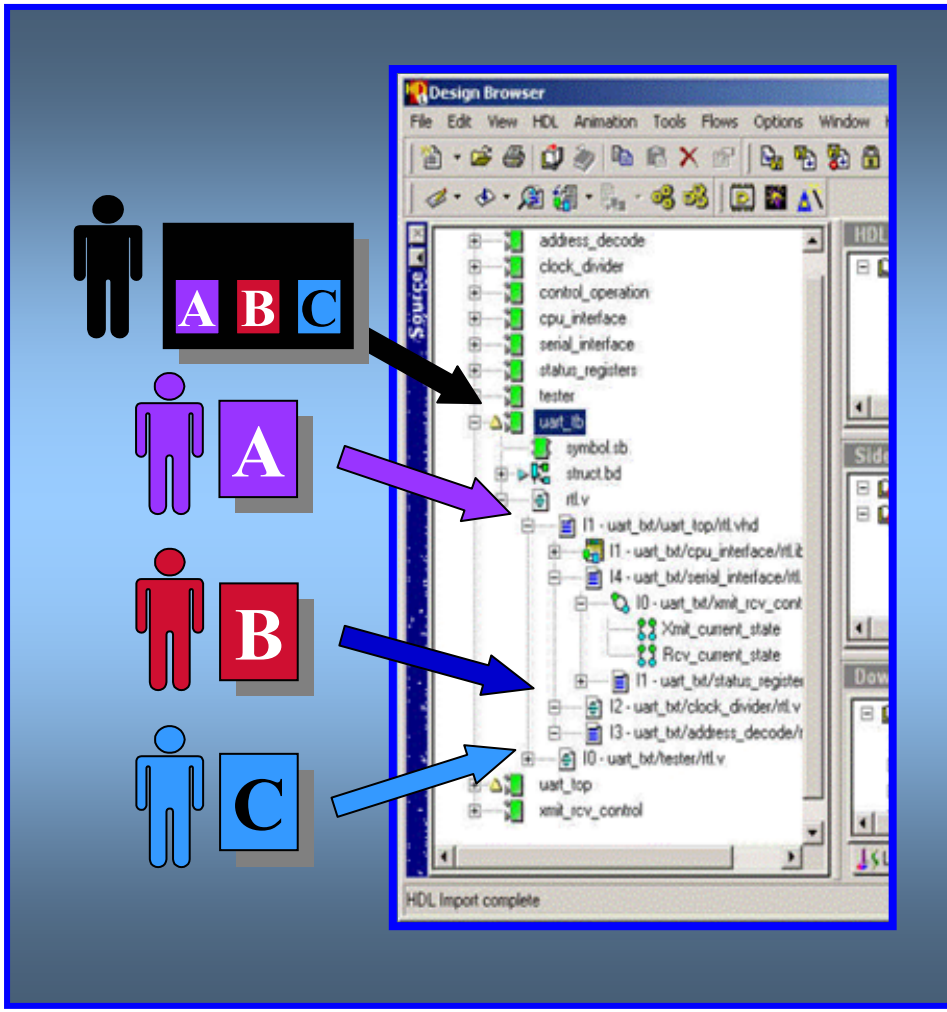


FPGA Advantage

- **FPGA Advantage enhances your FPGA design environment and increases productivity through**
  - **Design creation & reuse**
  - **Design management**
  - **Design documentation**
  - **Design debug**
  - **Design integration & iteration**

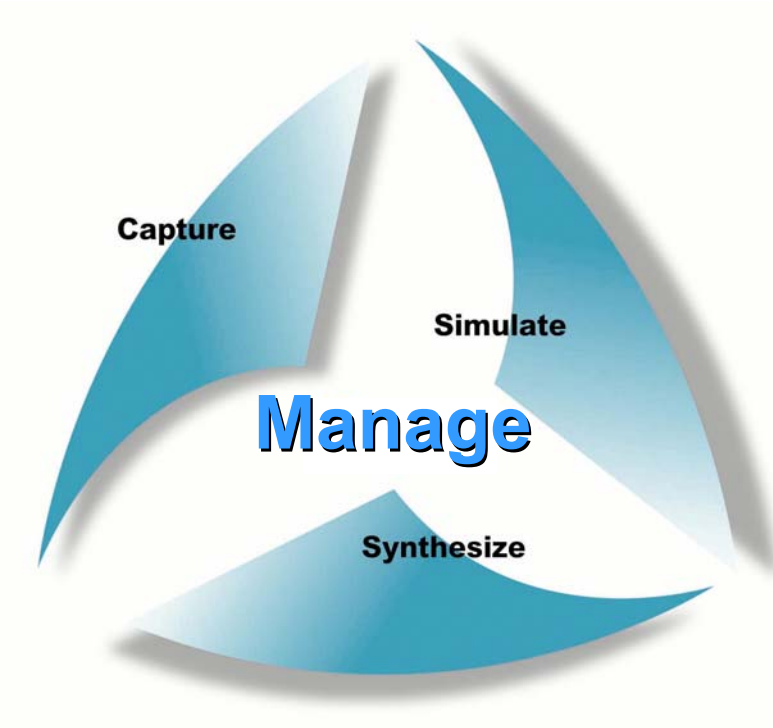
Team Design Environment

- FPGA design teams
  - 1, 5, 10+ engineers
  - Blocks designed separately but in context of entire design
  - Version control



Design Management

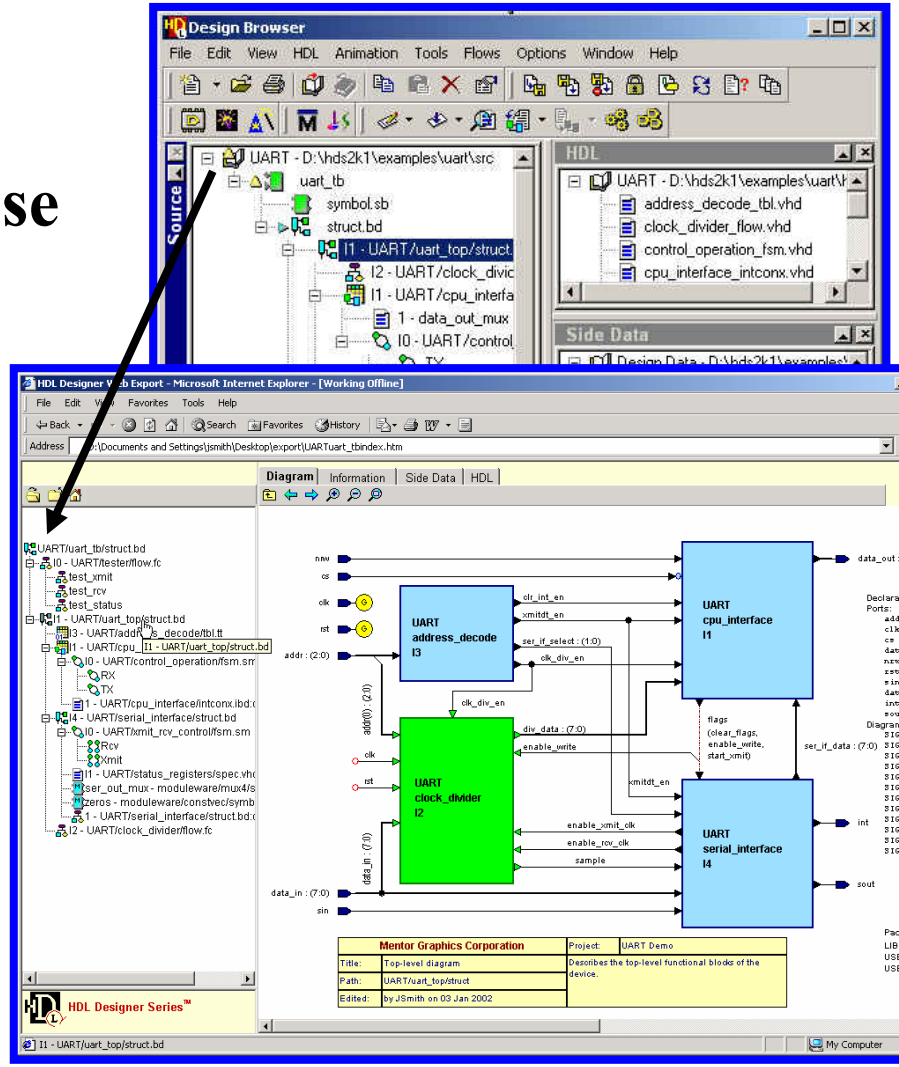
- FPGA Advantage manages
  - Libraries
  - Data files
  - Scripts & control files
  - FPGA vendor place & route
  - Timing files & test vectors
  - Documentation files
  - Version control



- Prepares design for future reuse

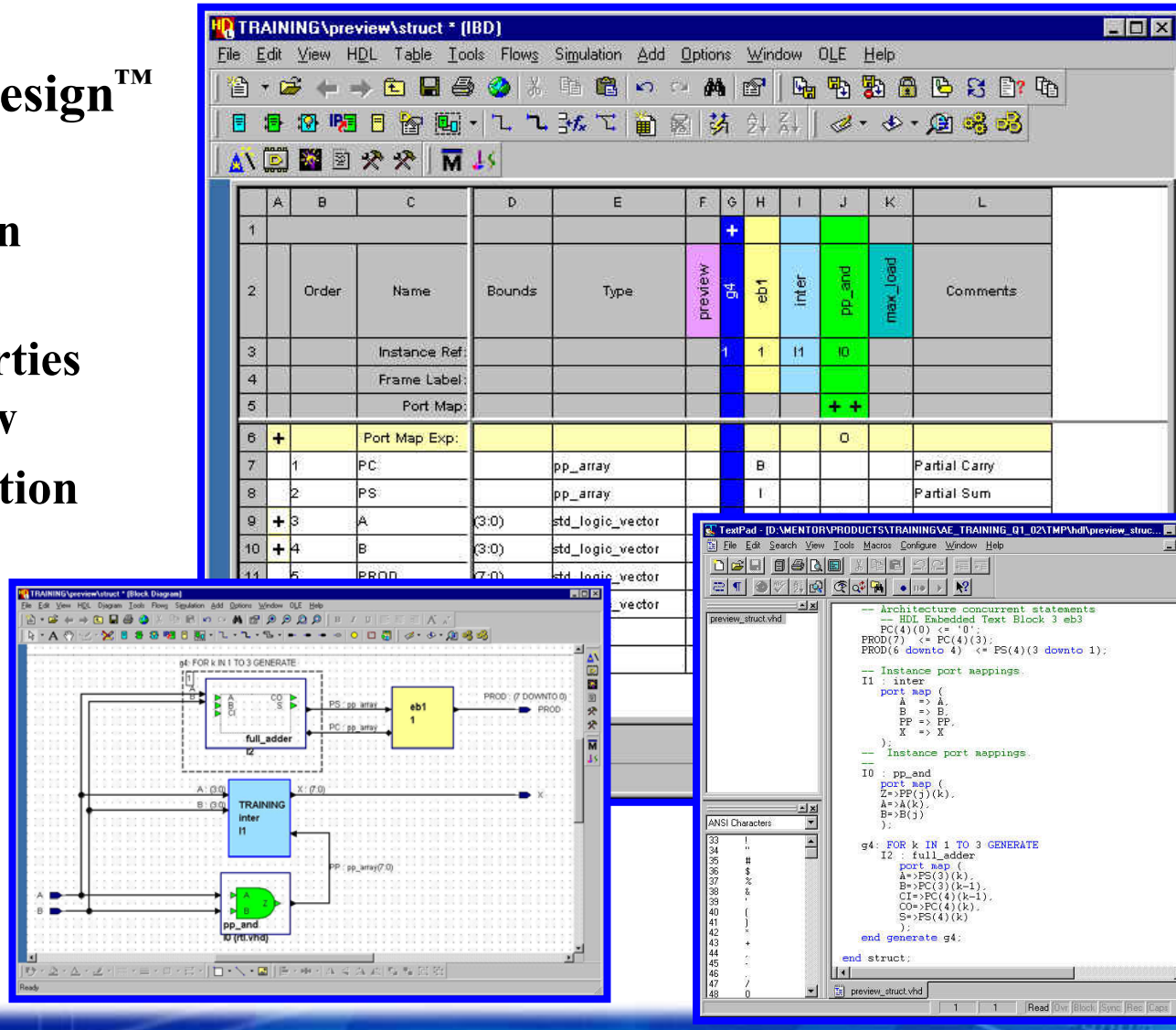
Design Documentation

- Required for design reuse
- Early start to design documentation
  - HTML
    - Share or publish the design
  - OLE
    - Keep design & documentation in sync



Design Creation

- **Interface-Based Design™ (IBD)**
  - **Structural design definition**
  - **Synthesis properties specified for flow**
  - **Aids documentation**
- **Block diagram**
- **Text entry**
- **State machine**
- **Flow chart**
- **Truth table**



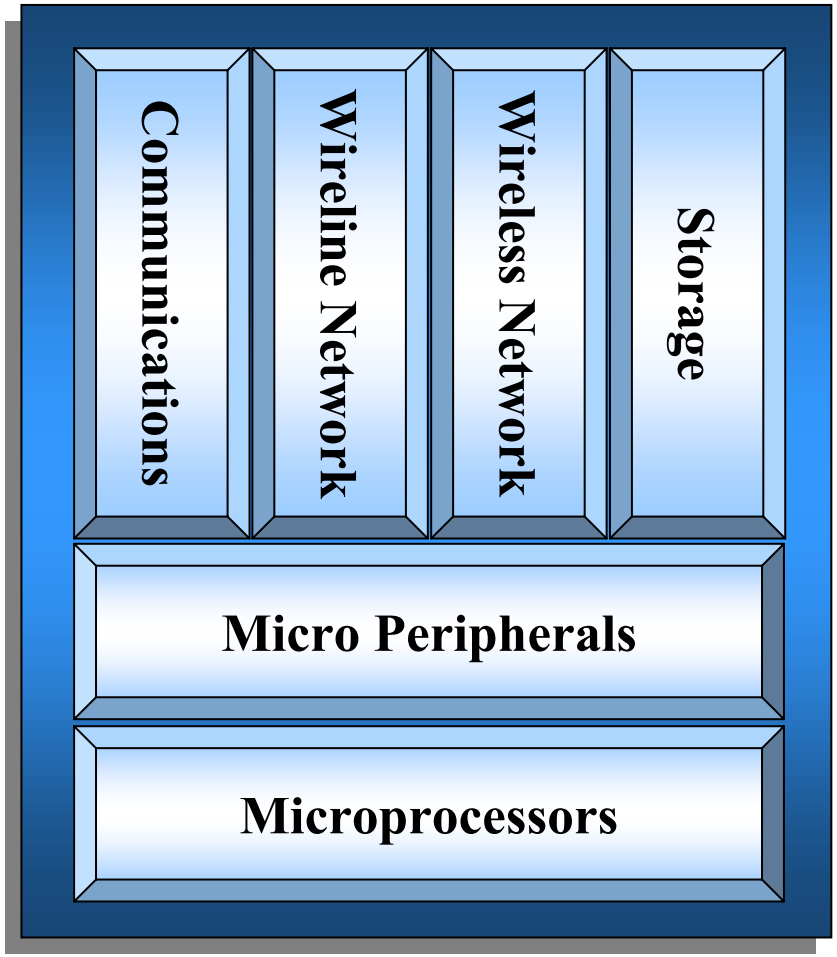
IP & Design Reuse

- **Cannot design without reuse**
  - **10 years ago: 1 engineer → 2K gates/project**
  - **Today: 1 engineer → 10K gates/project**
  - **By 2009: 1 engineer → 200K gates/project**

- **FPGA Advantage (HDL Designer Series)**
  - **ModuleWare™**
  - **Altera MegaWizard™**
- **Inventra™**
  - **Accelerated access, evaluation, & integration of proven IP cores**

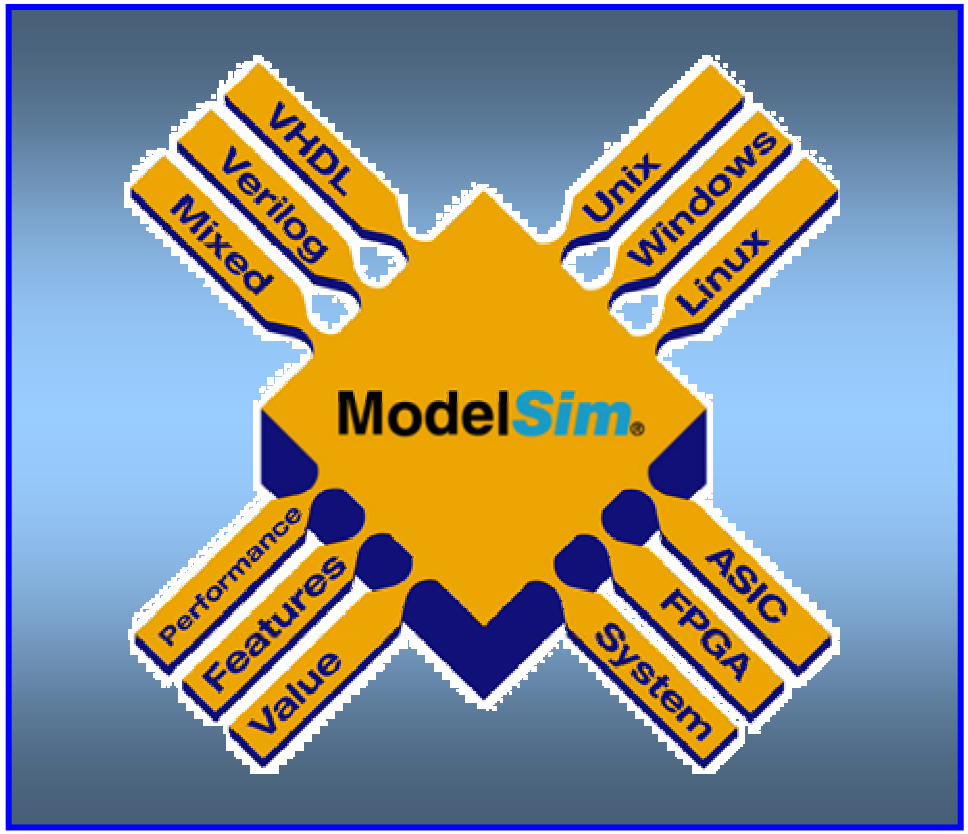
Inventra Products

- 80 synthesizable IP cores
- Robust deliverables for use & reuse
- Focus on communications standards
  - USB
  - Bluetooth
  - Ethernet
  - Wireless LAN
- Standard bus interfaces



ModelSim

- Market leading HDL simulator
- Focus
  - Performance
  - Debug
  - Productivity



FPGA Alliance

- **ModelSimAE (Altera Edition)**
  - **Altera Version is approx. 40% ModelSimPE (Contract says 25% of EE)**
  - **No Size limit**
  - **PE Functions Only**
  - **VHDL or Verilog not both**
  - **Only Altera Libraries (Pre-Compiled)**

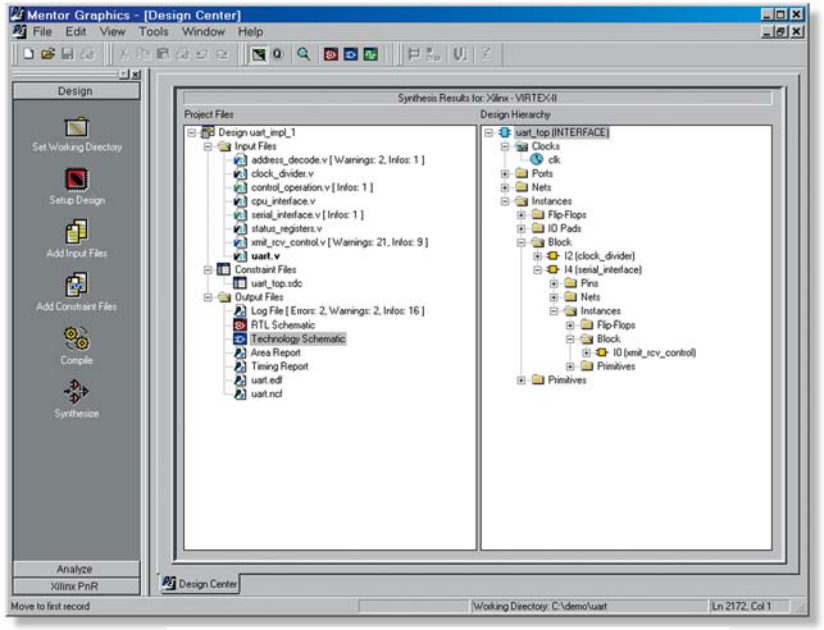
Advanced Synthesis for Advanced FPGAs

1. Intuitive Operation
2. Excellent Results
3. Accurate Analysis

Precision Design Center

- One interface drives all synthesis steps
  - Synthesis setup
  - Constraint entry
  - Results viewing
- Intuitive for first time user
- Includes advanced functionality required for large designs

The Synthesis Design Center



1. Intuitive Operation
2. Excellent Results
3. Accurate Analysis

LogicLock Design Flow

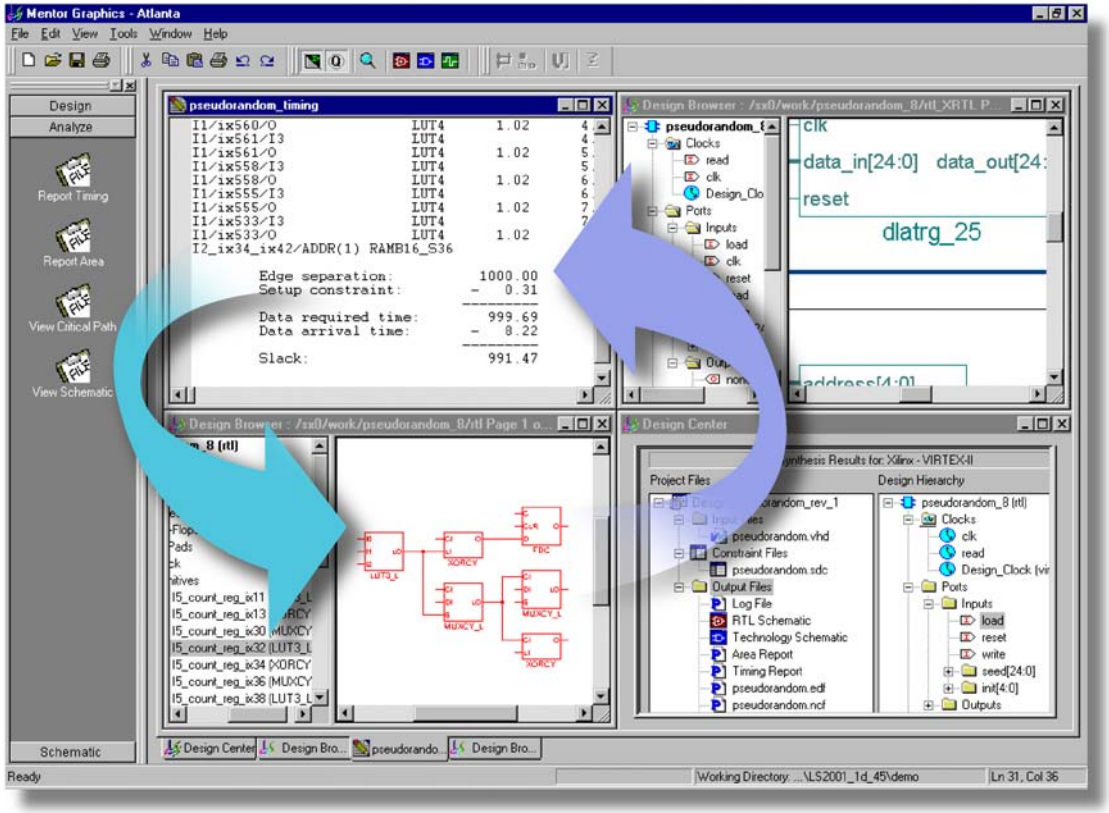
- **Precision Synthesis**
  1. Apply LogicLock
  2. Synthesize
  3. Output Multiple EDIF & Quartus Tcl Files

- **Quartus P&R**
  1. Analyze & Elaborate Design
  2. Import LogicLock Blocks
  3. Compile
  4. Back-Annotate LogicLock Constraints
  5. Incrementally Change and Re-import Blocks as needed
  6. Re-Compile

PreciseTime Analysis

- Incremental
- Advanced
- Interactive

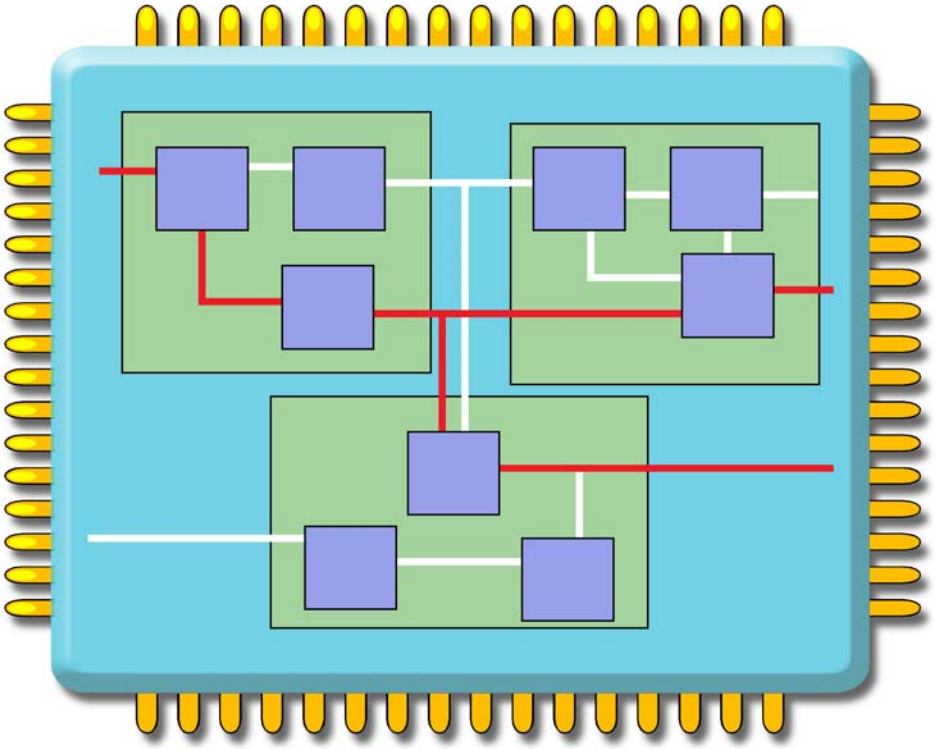
- Focuses on timing issues within the circuit



Precision™ synthesis

ASE Optimizations

Architecture Signature Extraction

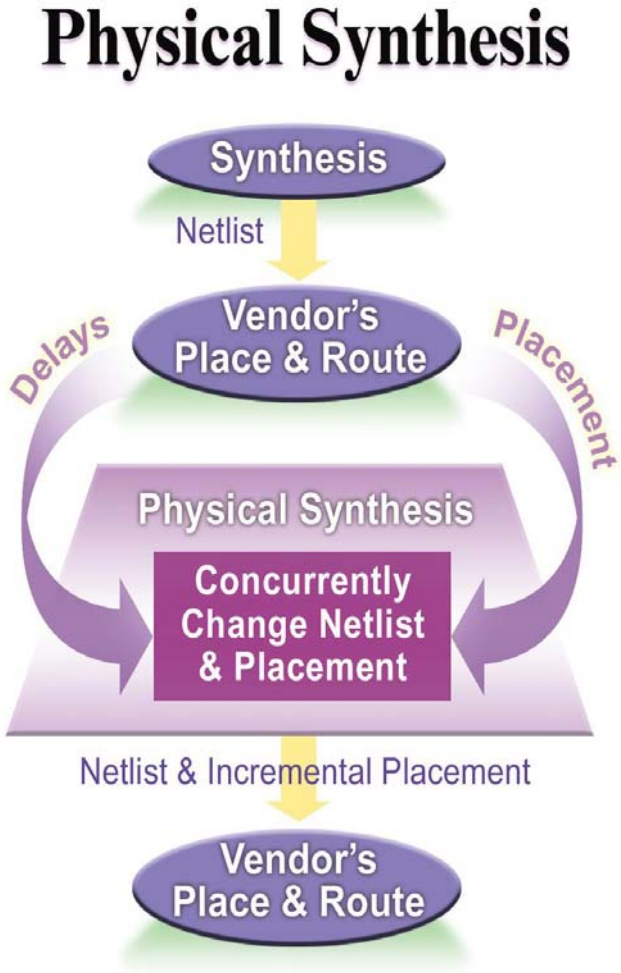


- Finite state machine restructuring
- Cross hierarchy restructuring
- Critical path optimization
- Path retiming

Precision™ synthesis

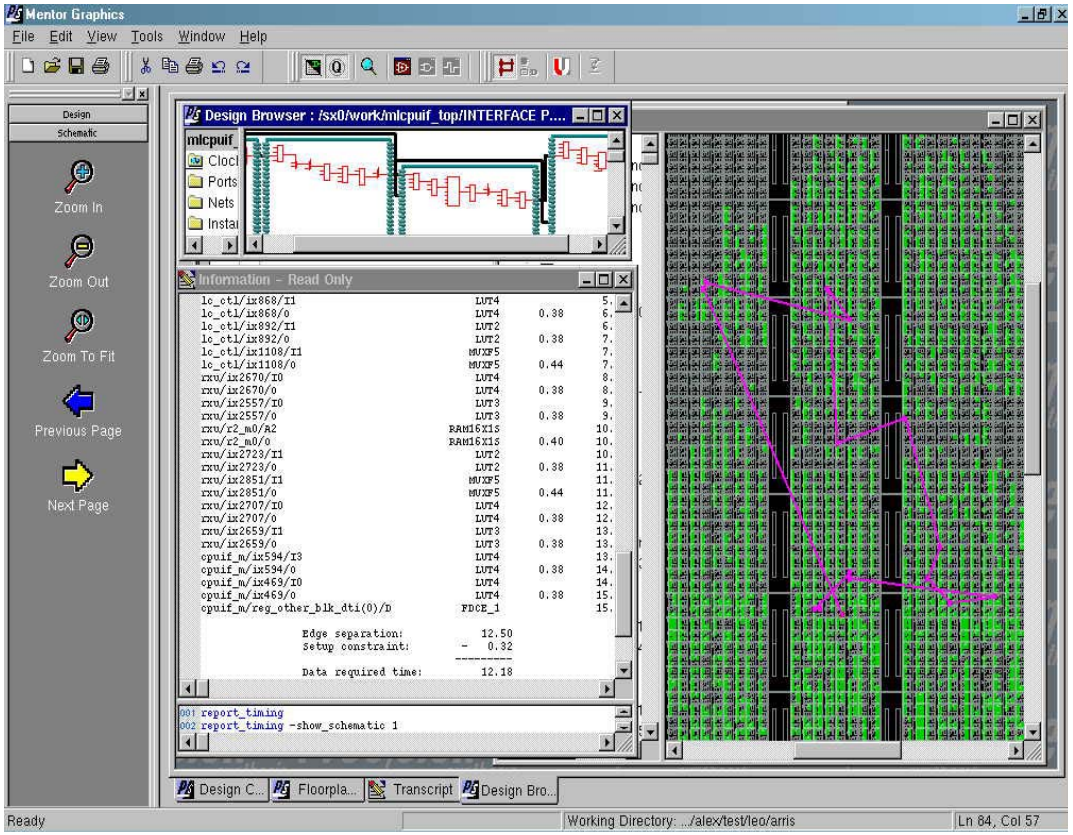
Physical+ Synthesis

- Synthesis based on knowledge of placement and the delays
  - Delay calculation based on the placement
  - Understanding of placement rules
  - Knowledge of available resources
- Incremental changes speeds design convergence

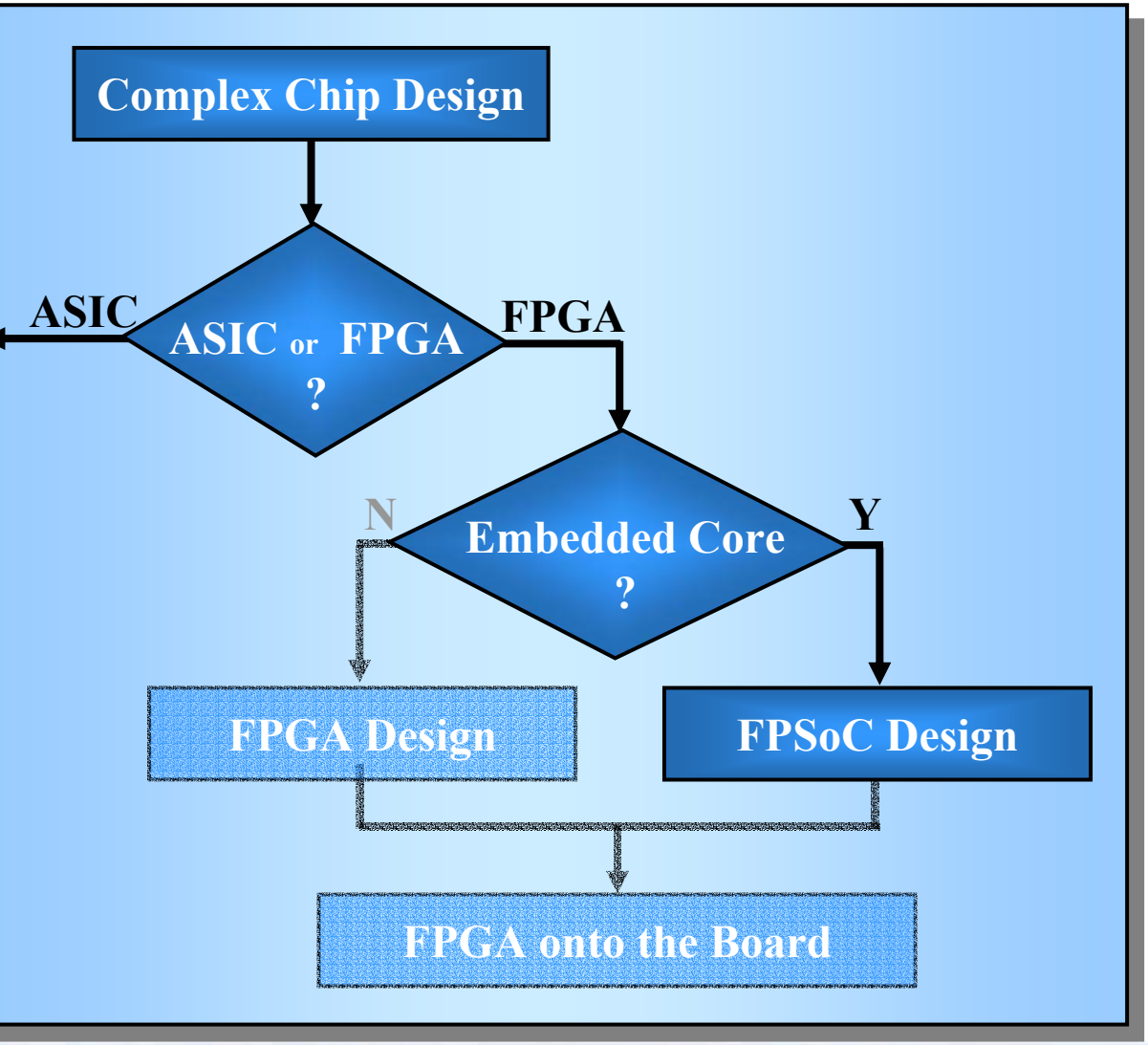


Precision™ synthesis Physical+ Environment

- **Physical & schematic views with interactive timing environment**
  - **Floorplanning and interactive fix-up**
  - **Cross probing from different windows**
  - **Incremental updates of timing to quickly verify any edits**



FPGA with On-chip Microprocessor



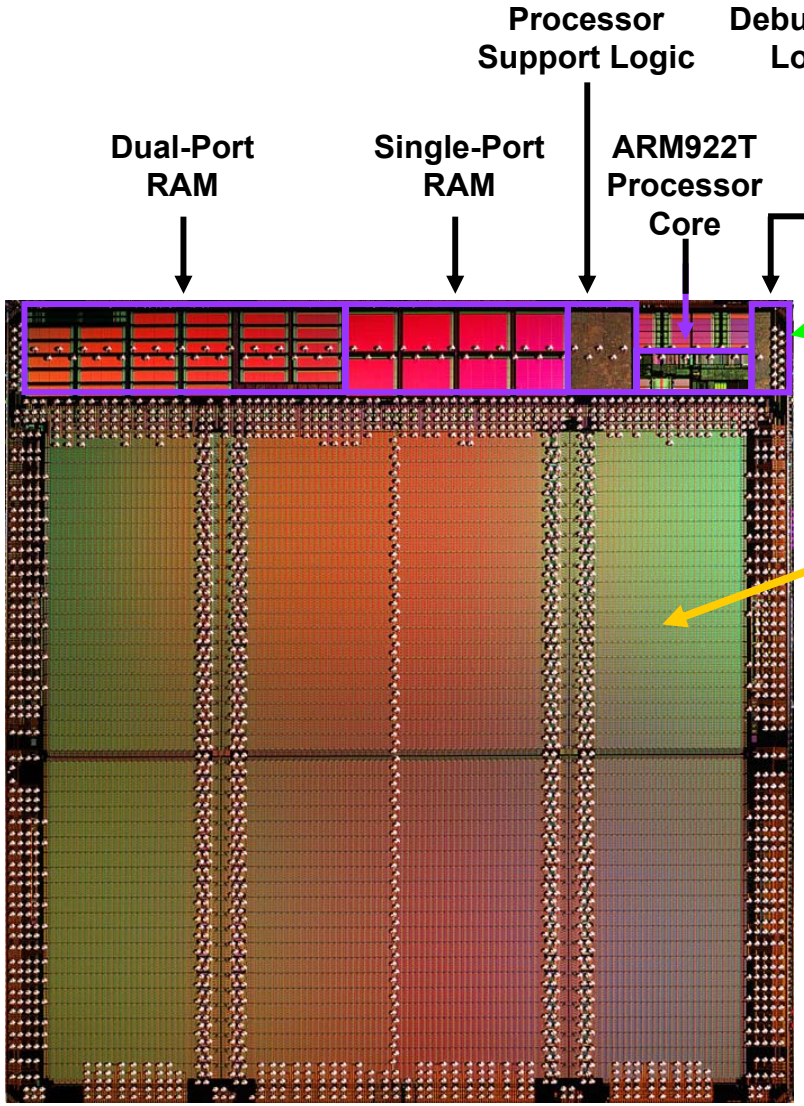
- **FPSoC: Field Programmable System-on-a-Chip**
  - Single device for
    - Field programmable logic
    - One or more processor cores, memory, hard & soft macros
    - Incorporating system functionality

Why FPSoC?

- FPGA technology has bounded the SoC challenge
- Embed the processor core for high speed
- FPGAs provide HW/SW repartitioning flexibility
- Single device can contain
  - Processor, memory, peripherals, glue logic

In 3-5 years, 10% of the FPGA market will be FPSoC design, compared to today's 1%.

Altera ARM-Based Excalibur Architecture



The "Stripe"

- Hard logic

Programmable Logic Fabric

- 100K to 1M gates

Mentor's FPSoC Design Solutions

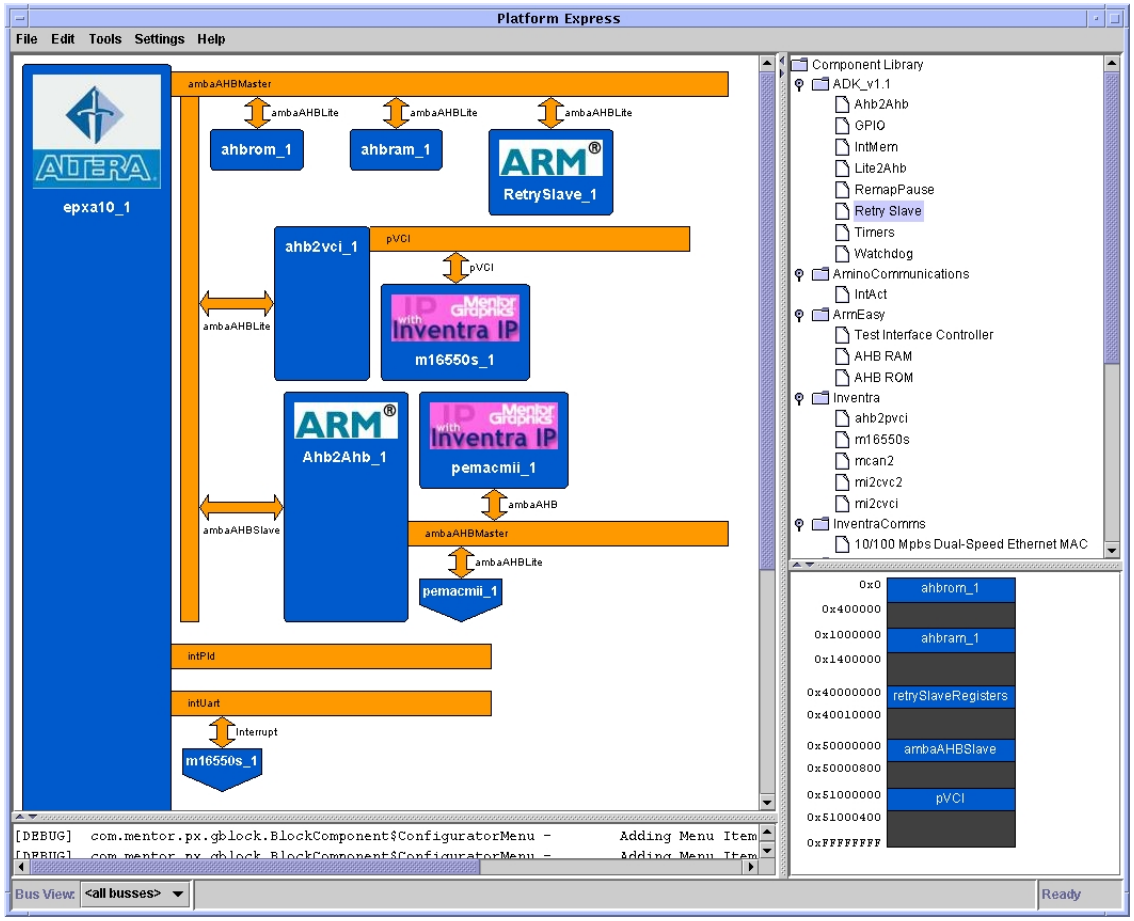
Platform Express™

Seamless® CVE

FPGA Advantage®

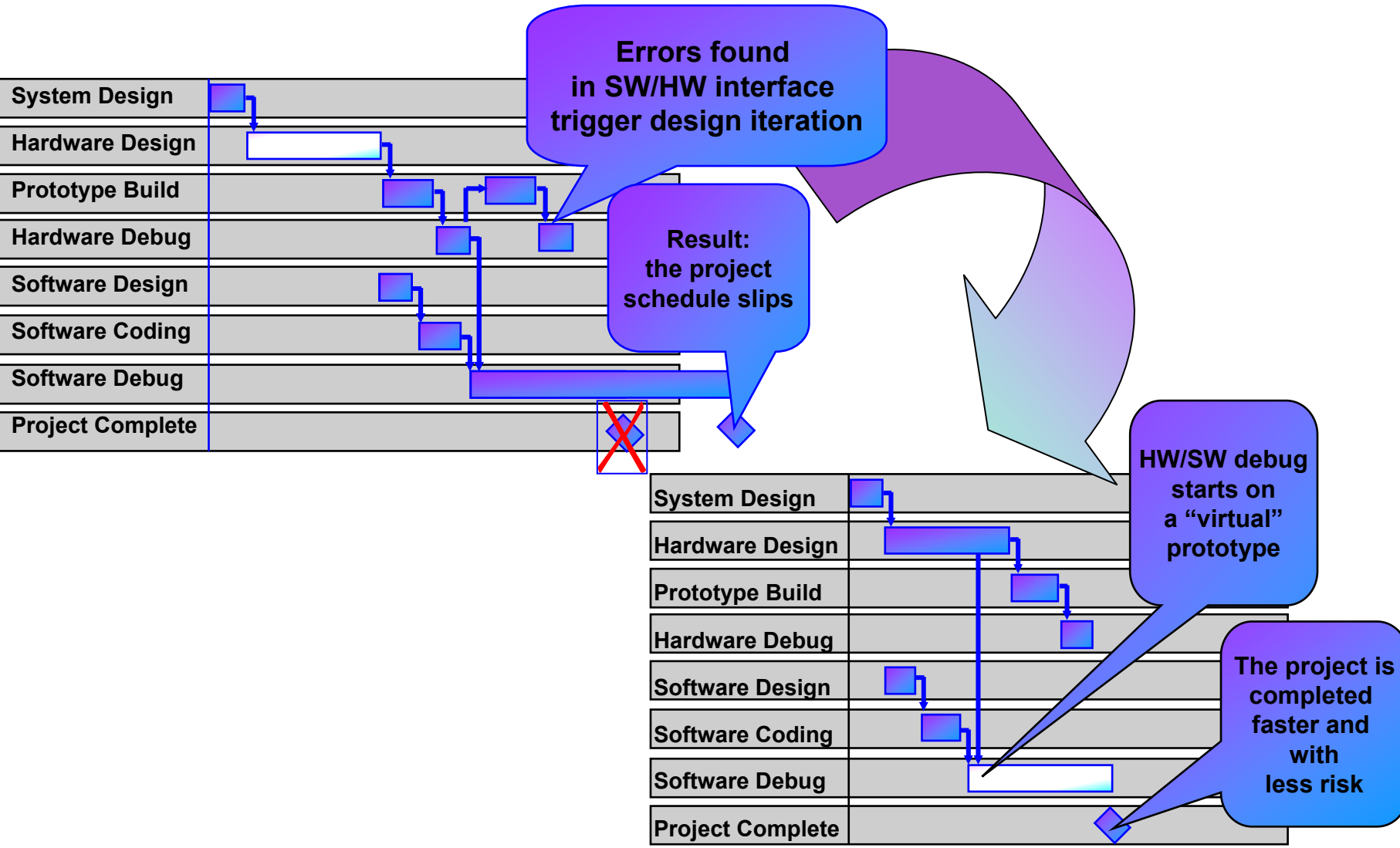
Platform Express

Rapid design of complex SoC sub-systems



- **Drag'n'drop platform core & IP**
- **Bus knowledgable**
  - **Automatic bus decoding bridging**
  - **Automatic interrupt bridging**
- **Top level netlist generation**

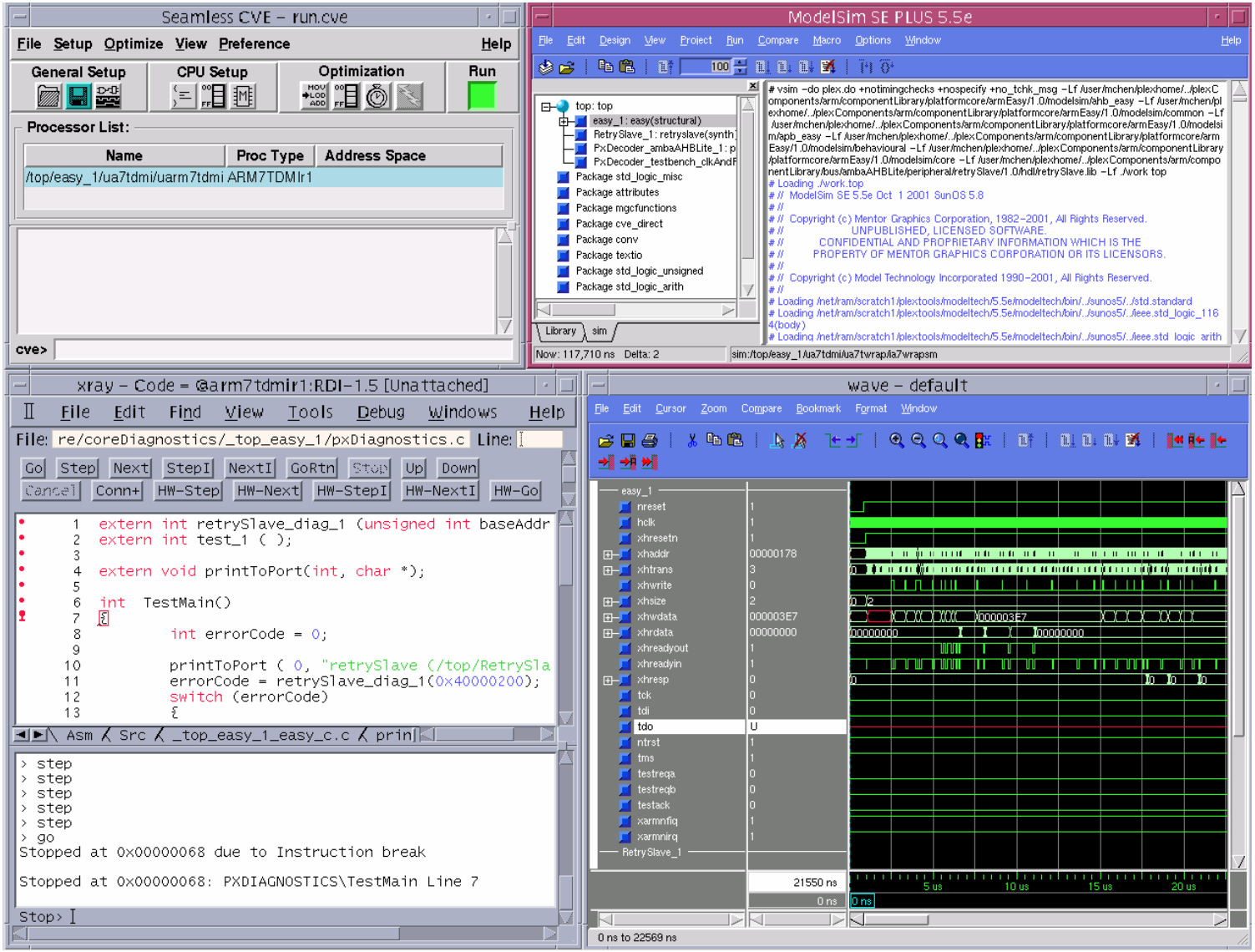
Seamless CVE For Co-Verification



Why Not Program FPSoC and Test In-System?

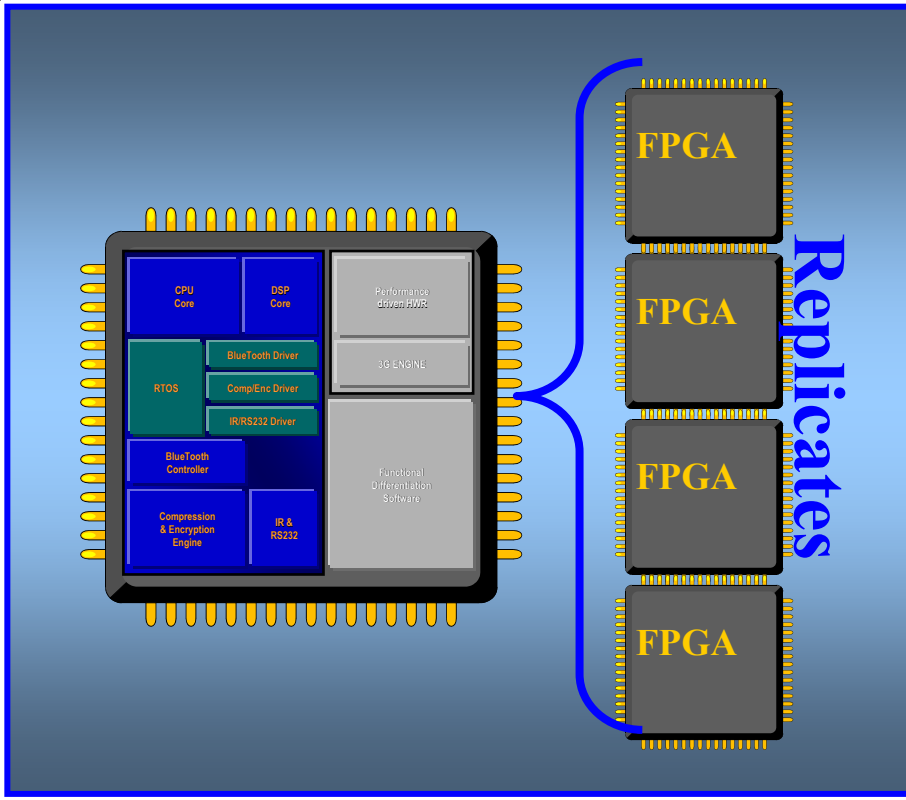
- Co-verification provides
  - Virtual prototype
  - Early availability
    - Begin SW debug earlier
    - Board may not be ready
  - FPSoC in the system context
  - Debug controllability & observability
    - Can reverse time
  - Performance

Seamless Environment

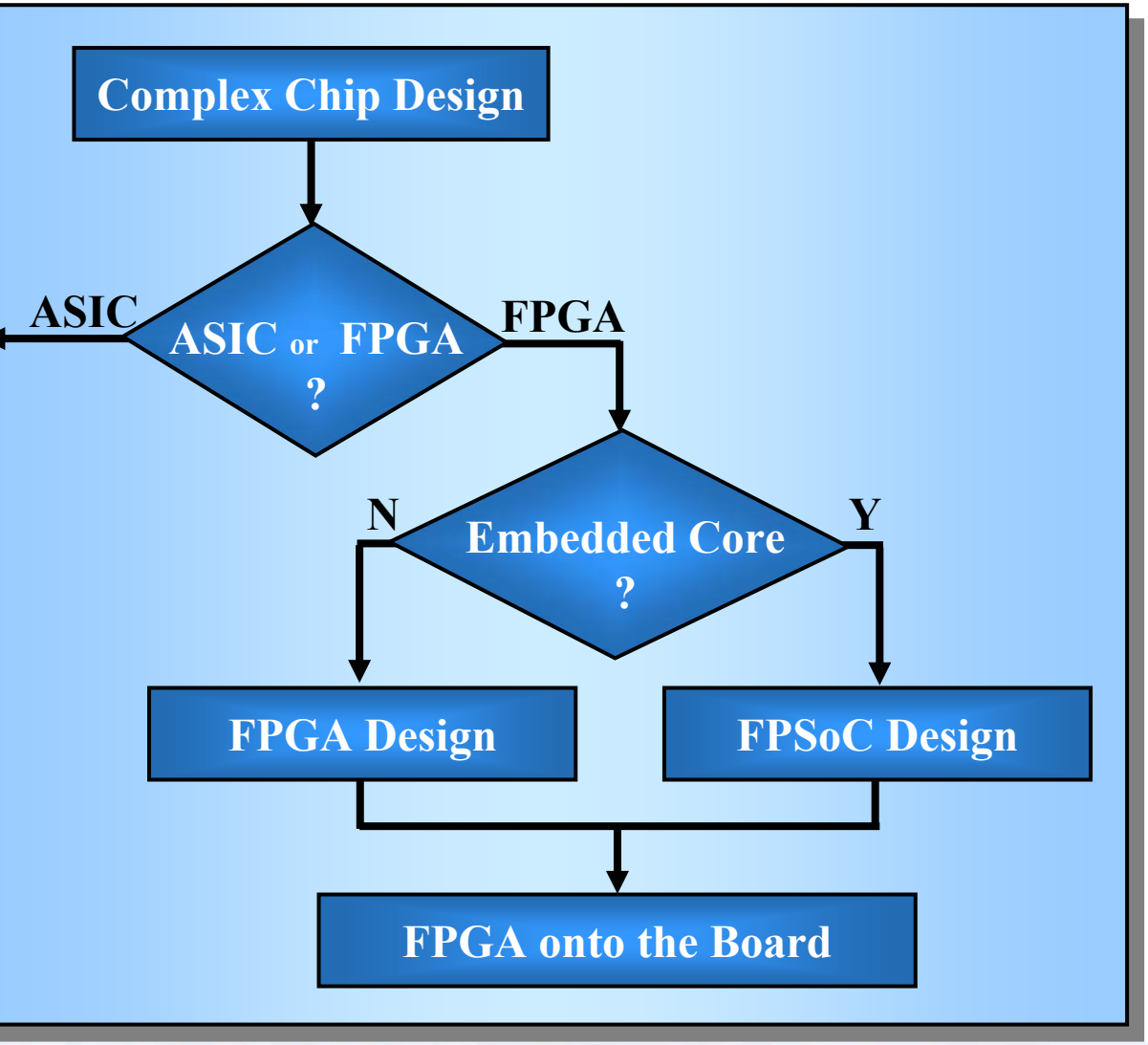


Replicates

- **Parallel development of complex design**
  - **Copies of design in development →HW and SW designers**
  - **Same functionality, different observability**
  - **Updates as design refines**



Every Chip Goes Onto A Board



- Extend FPGA debug & verification to FPGA on board design & verification

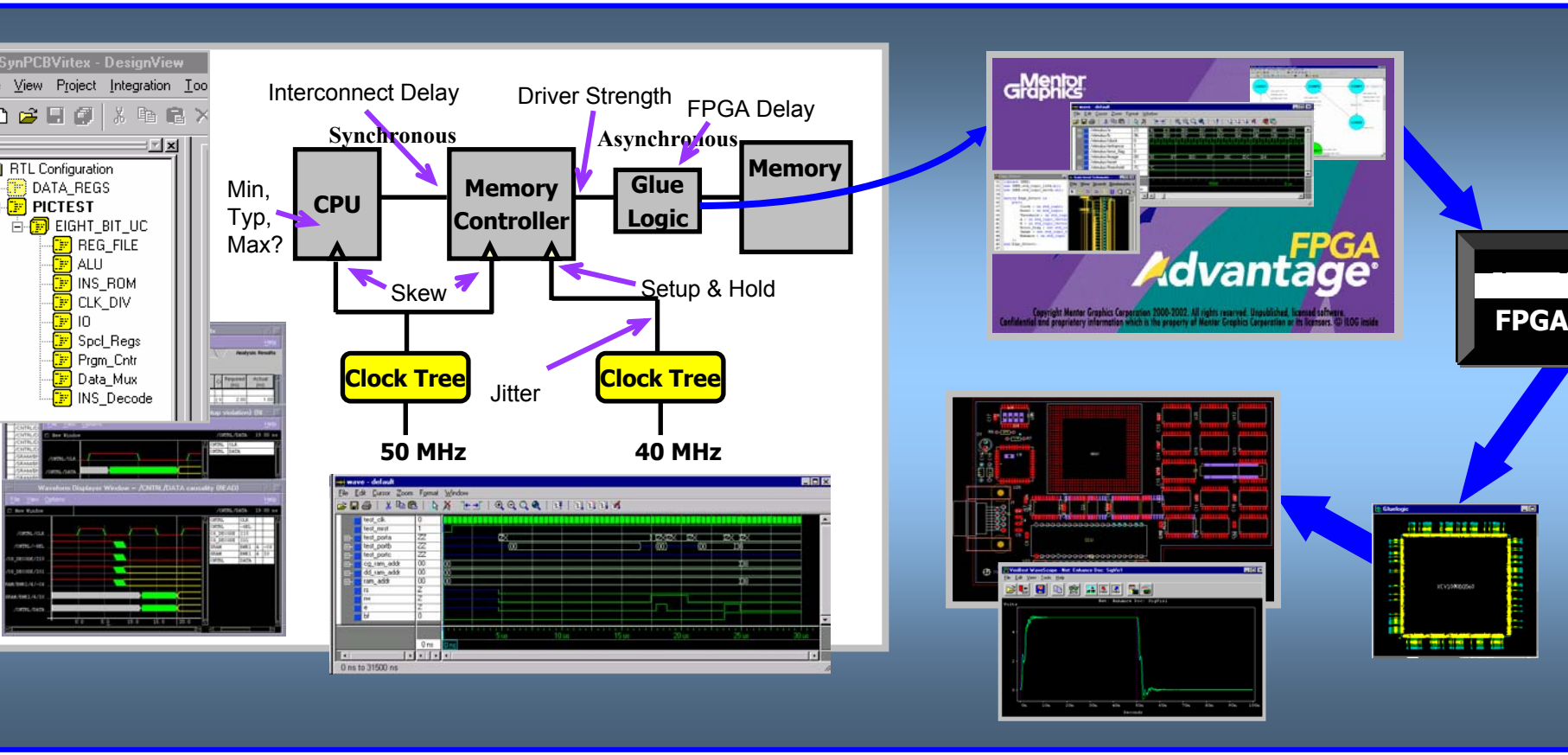
Mentor's FPGA on Board Solution

DesignView™

FPGA BoardLink™

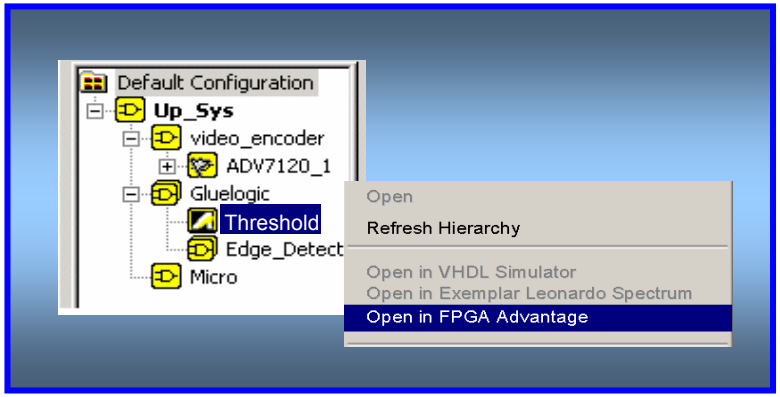
FPGA Advantage®

DesignView
Design Process Integration



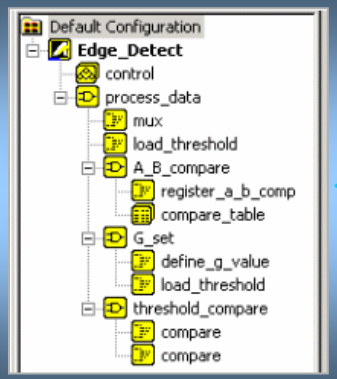
FPGA Advantage
Design Process Integration

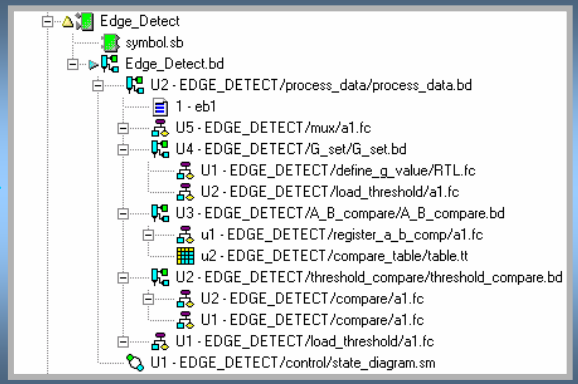
FPGA design invocation in FPGA Advantage from DesignView



FPGA design structure visible DesignView

DesignView

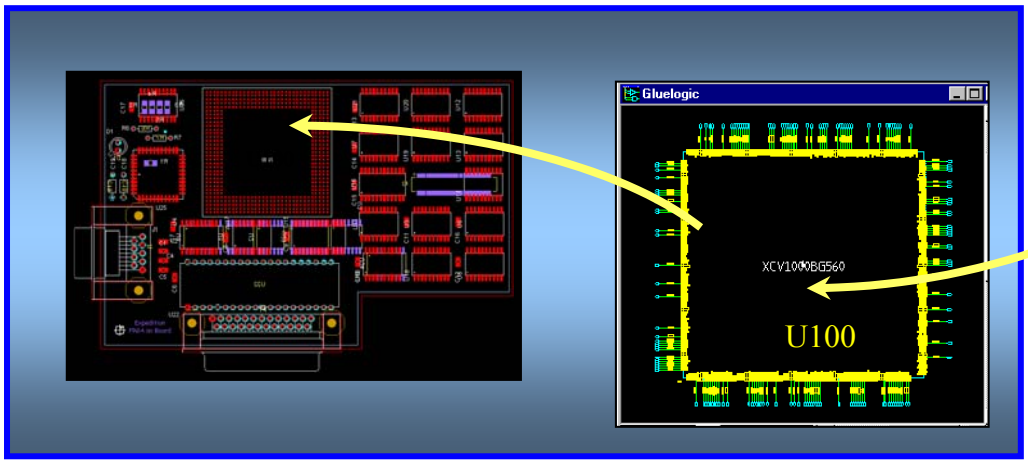


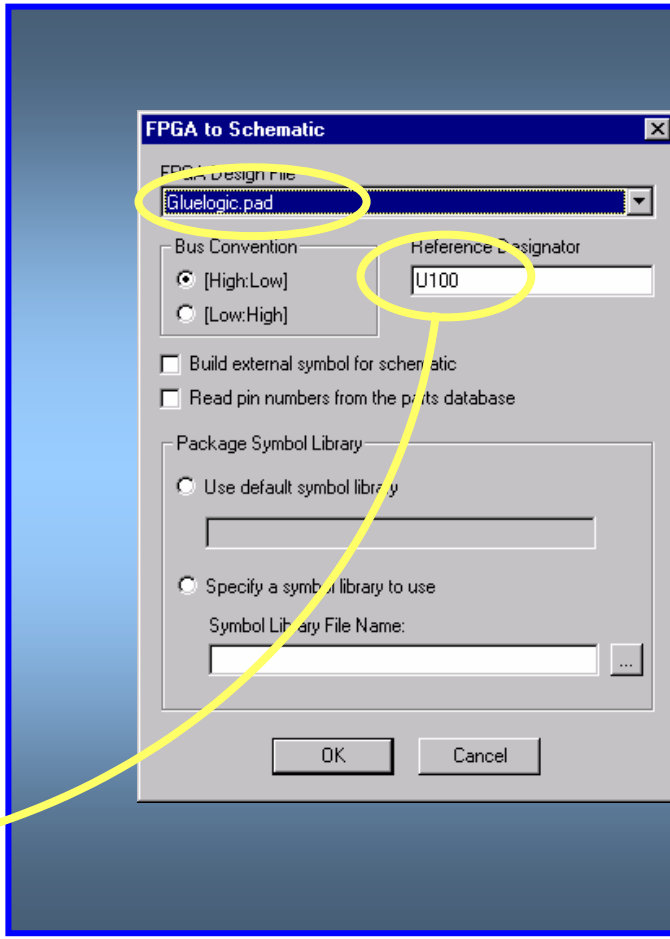


FPGA Advantage (HDL Designer)

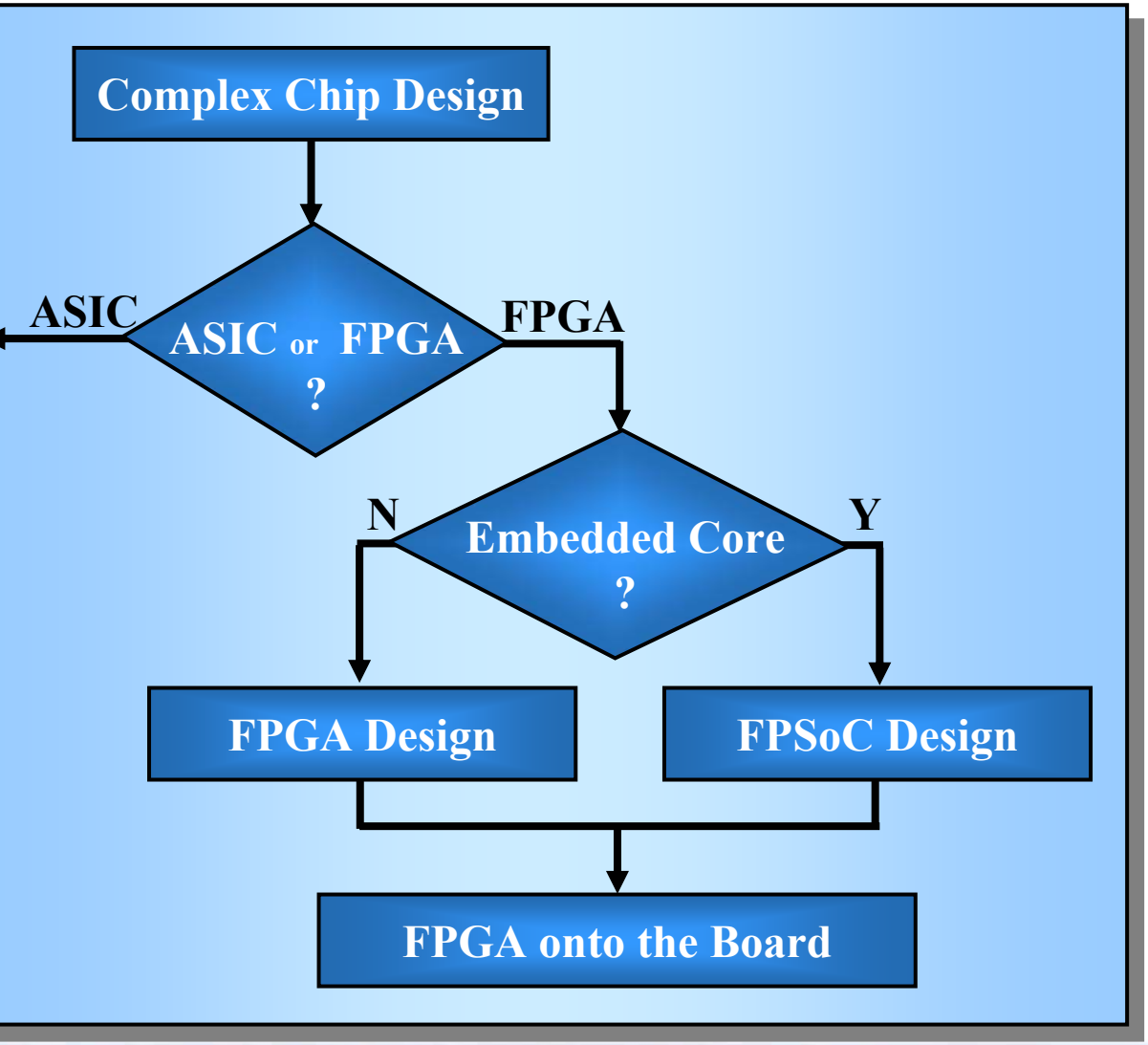
FPGA BoardLink Interconnectivity

FPGA BoardLink synchronizes FPGA and board processes





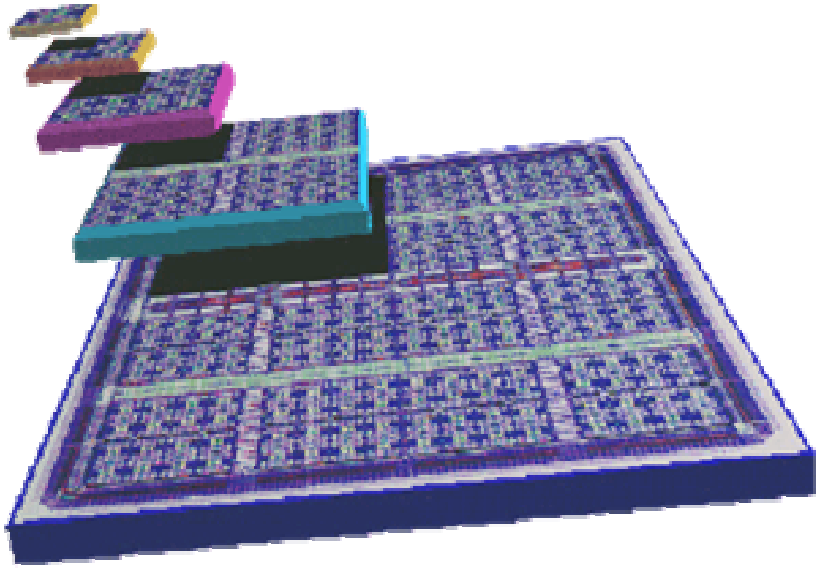
Other FPGA Design Considerations



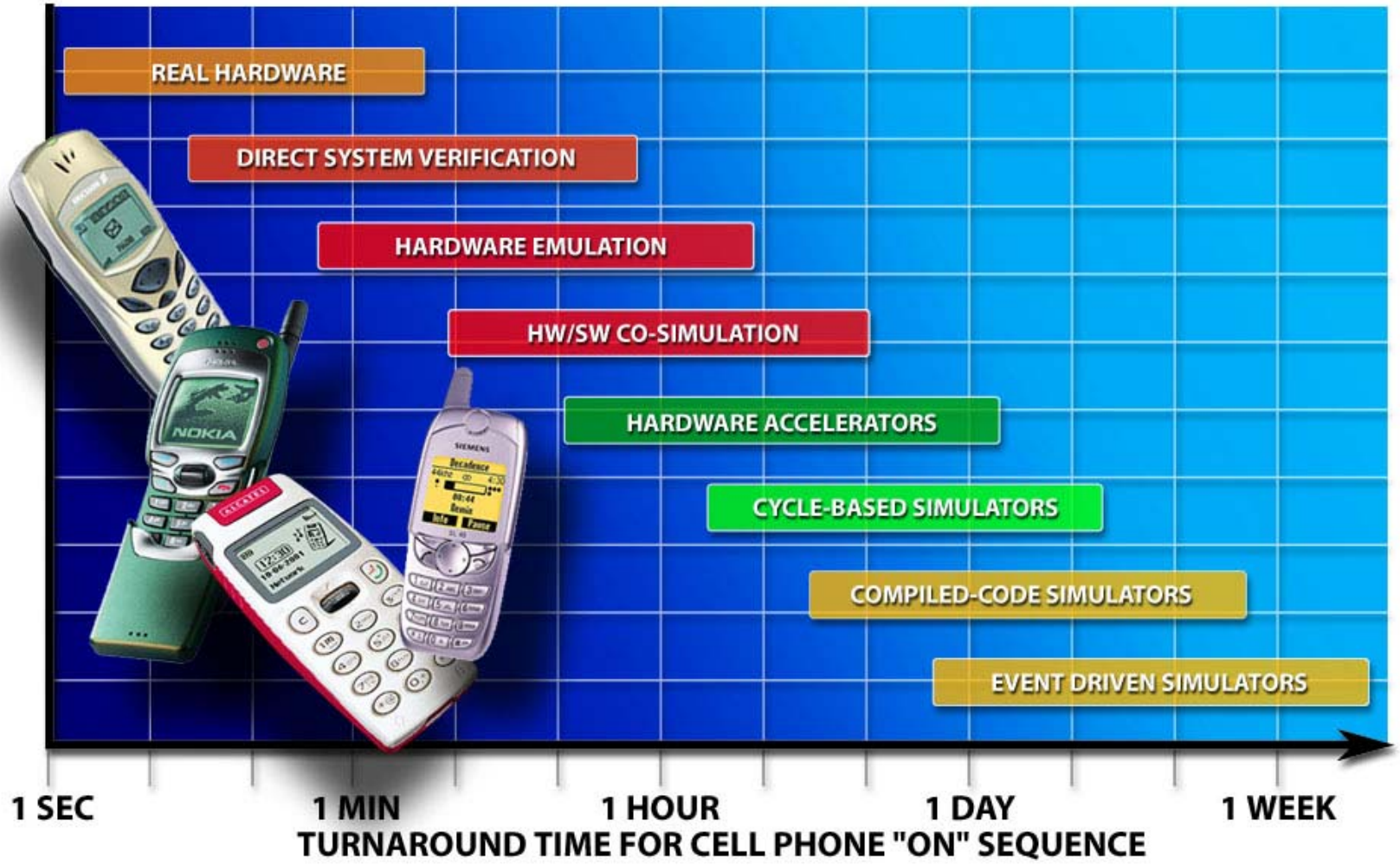
- ASIC prototyping
- Formal verification
- Customer support

FPGA's for ASIC Verification

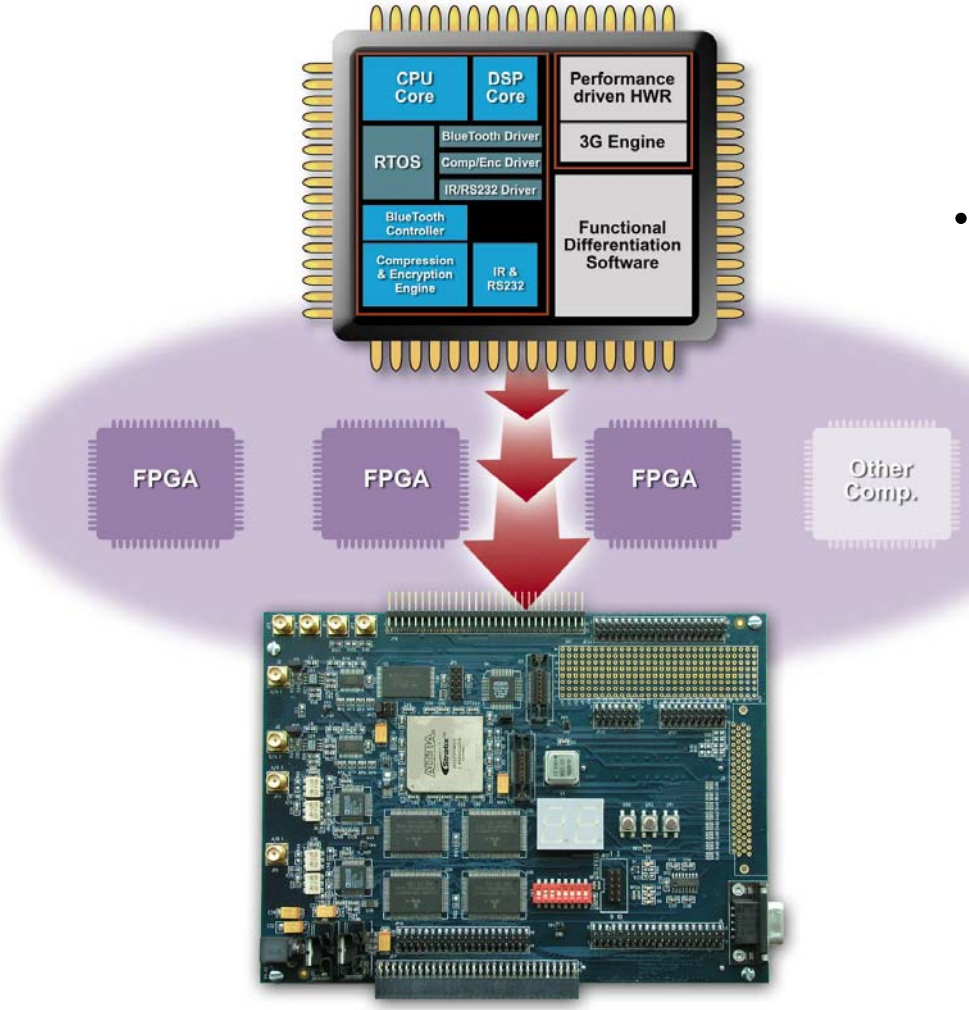
- **Faster time to market**
  - Fastest operating speeds of all verification technologies
- **Lower risk**
  - Low Cost
  - Avoid Mask Set
  - Avoid Re-spin



Direct System Verification (DSV)



SpeedGate DSV™

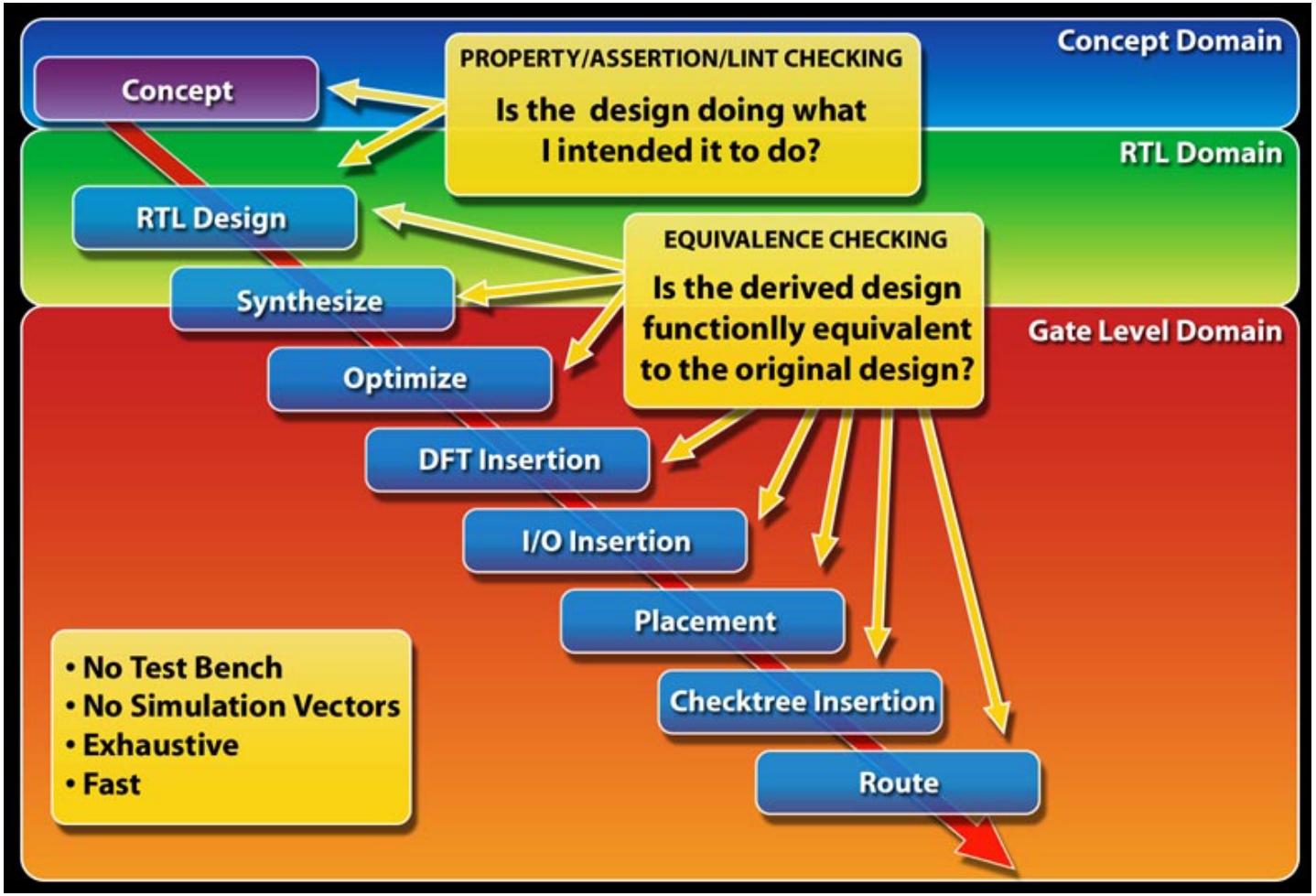


…an advanced methodology for developing and testing ASIC and SoC prototypes using off-the-shelf FPGAs in one or more custom or pre-defined Printed Circuit Boards…

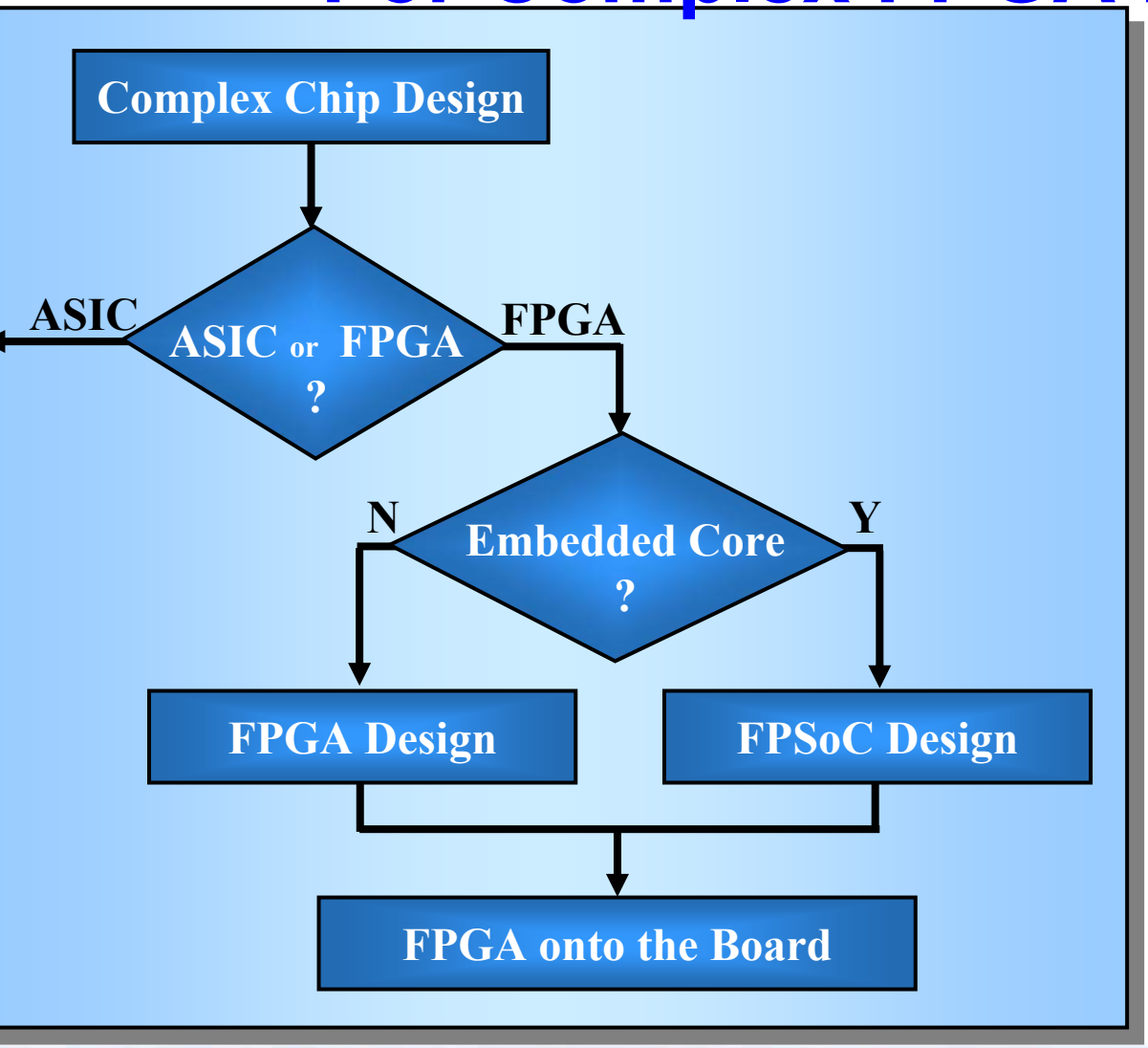
SpeedGate DSV and PCBs

- 3rd party prototyping boards
  - Fixed routed THE DINI GROUP
  - Reconfigurable Aptix
  - Others: Logic Express, Nallatech
- Custom boards
  - DesignView with FPGA BoardLink

Formal Verification with FormalPro™



Mentor Graphics Has The Tools For Complex FPGA Design



- Individual suites on
  - FPGA Advantage
  - HDL Designer Series
  - ModelSim
  - Precision Synthesis
  - Precision Physical
  - Inventra IP
  - Platform Express
  - Seamless CVE
  - DesignView
  - FPGA BoardLink
  - SpeedGate DSV
  - FormalPro

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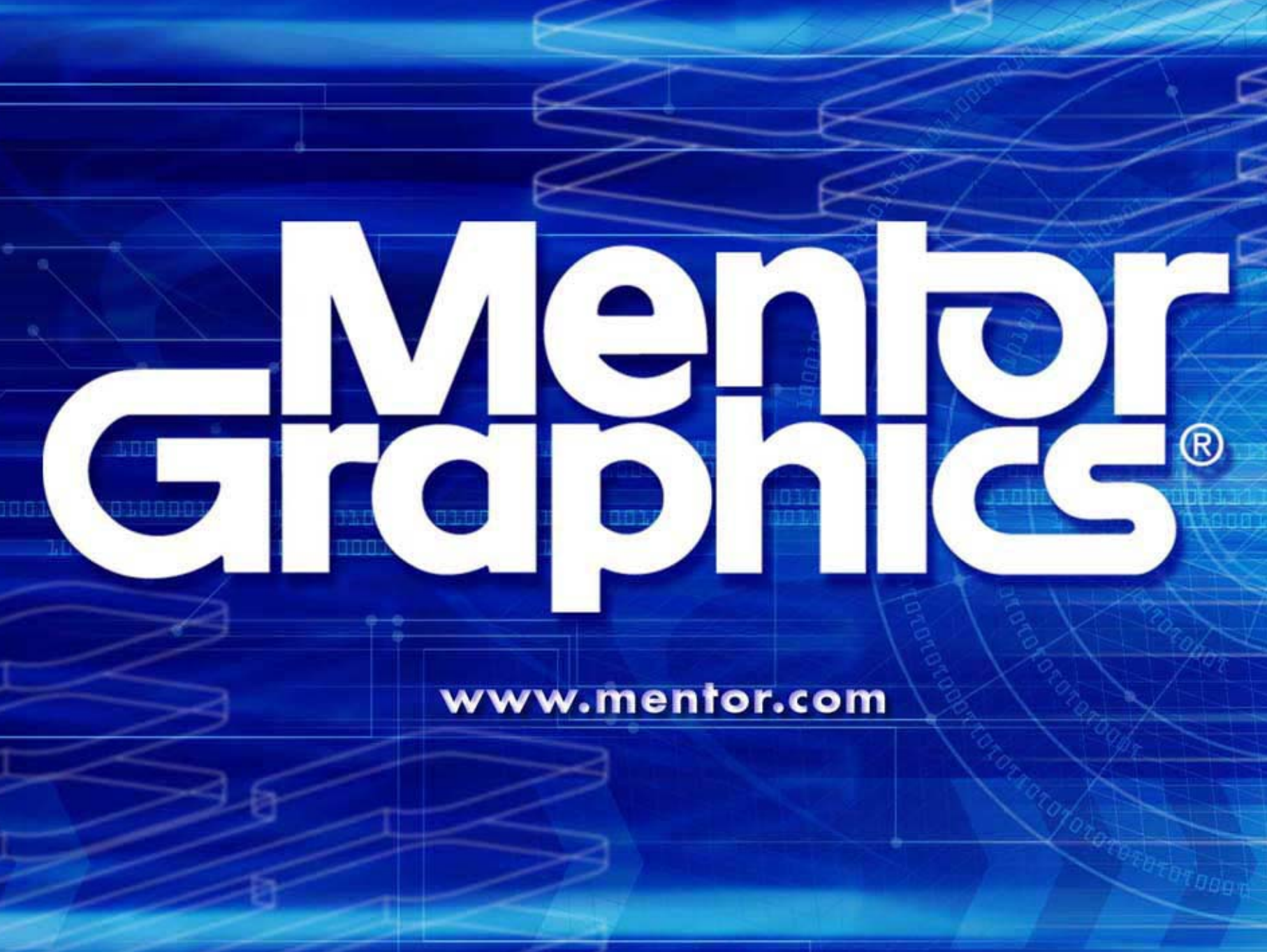
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