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FPGA Co-Processing for DSP

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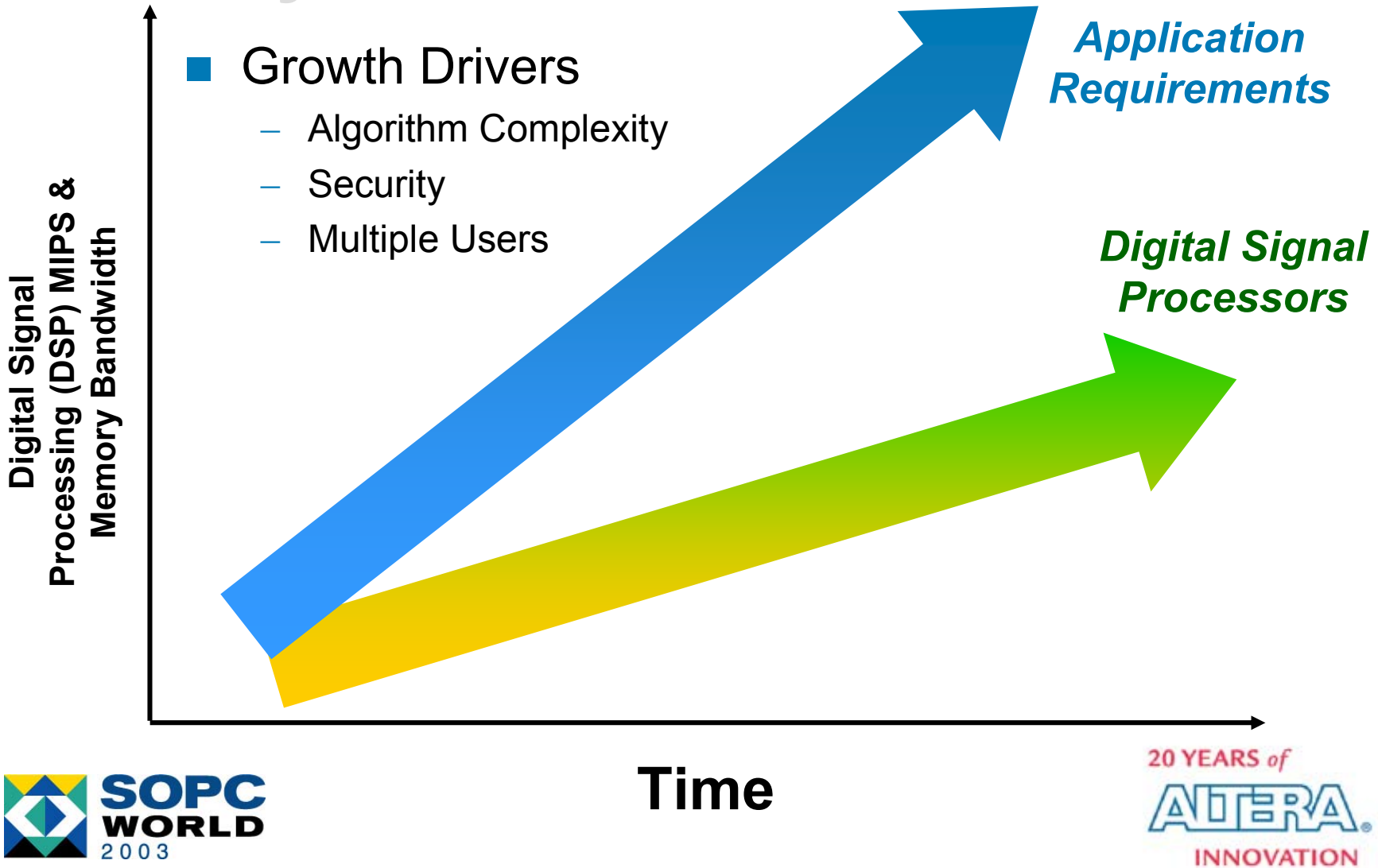
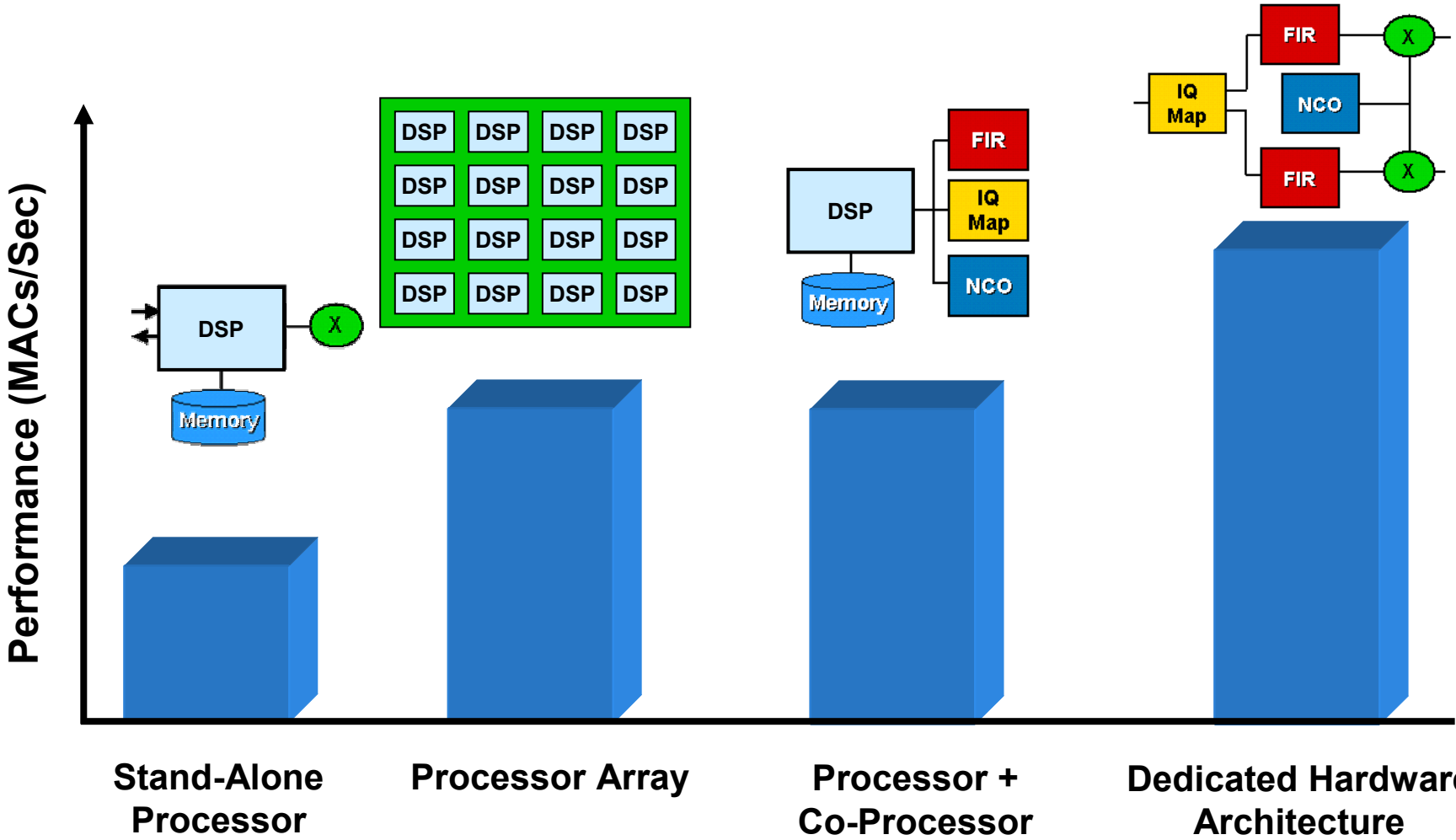
Agenda

- Applications of FPGA-Based Co-Processors for DSP
- Development Tools & Methodologies Available from Altera to Build Co-Processors
  - SOPC Builder
  - DSP Builder
- FPGA Co-Processor Development Examples
  - QAM Modulator
  - FIR Filter

Growing Demand for MIPS & Memory Bandwidth



DSP System Architecture Options



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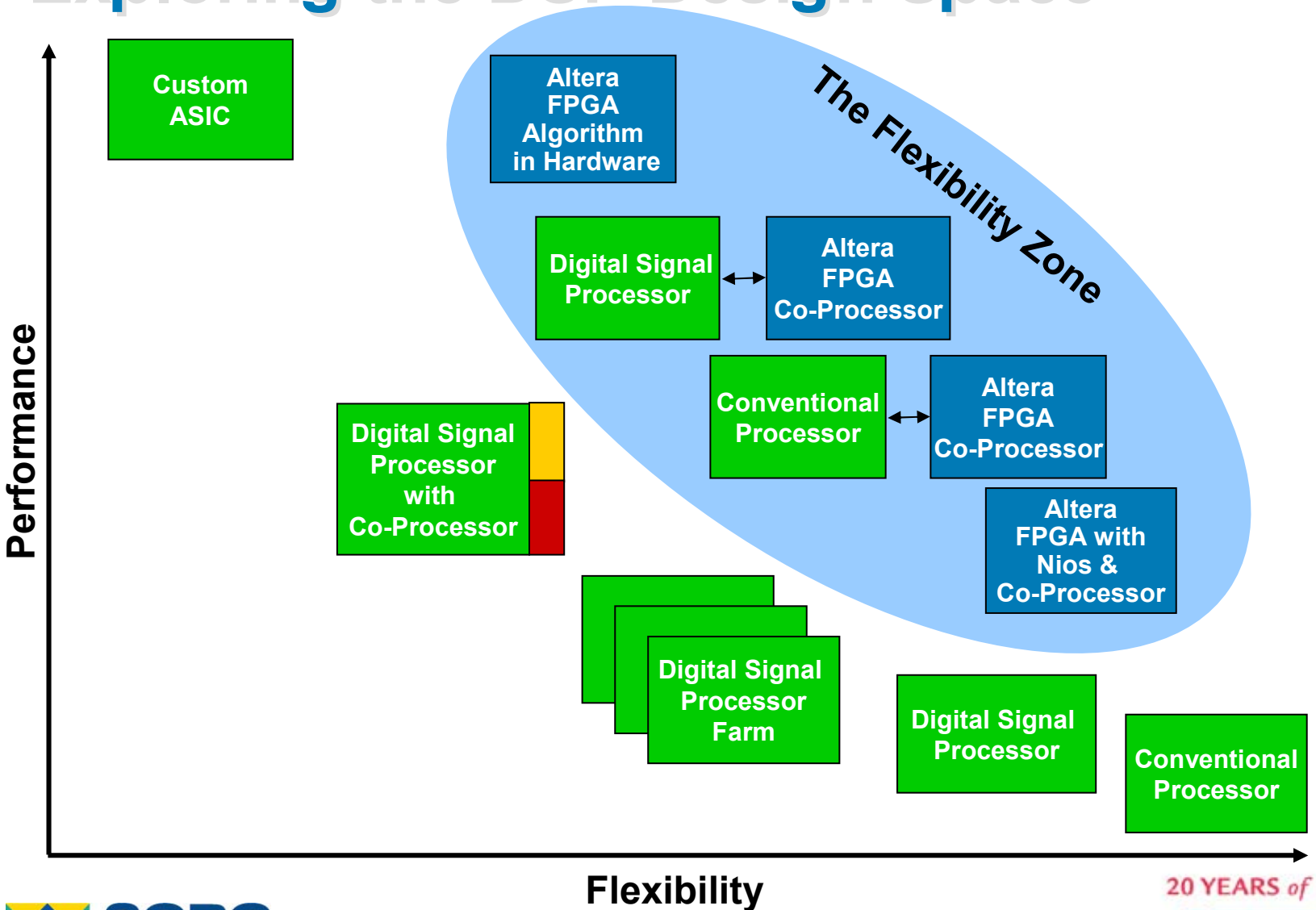
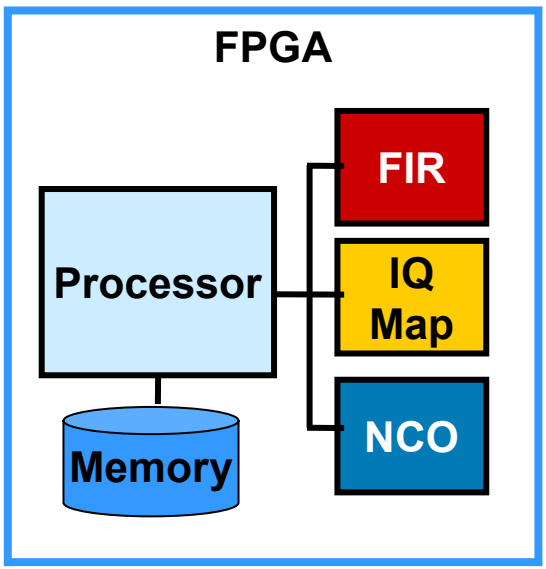
Exploring the DSP Design Space

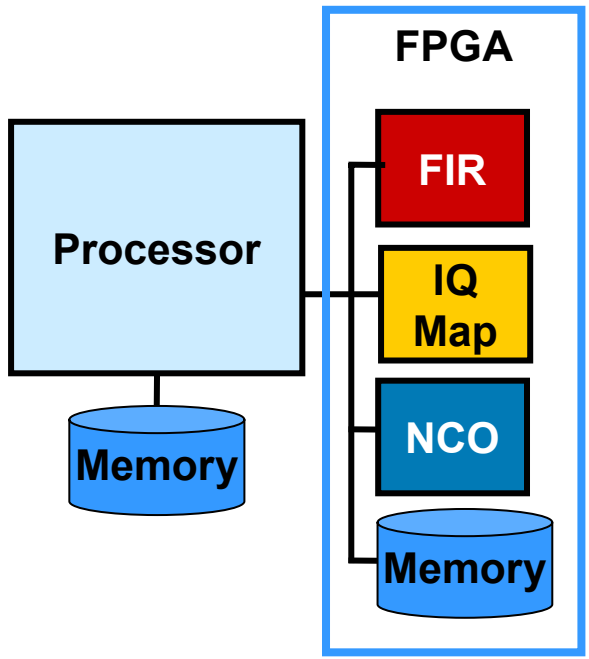


Co-Processing on FPGAs

Processor on FPGA

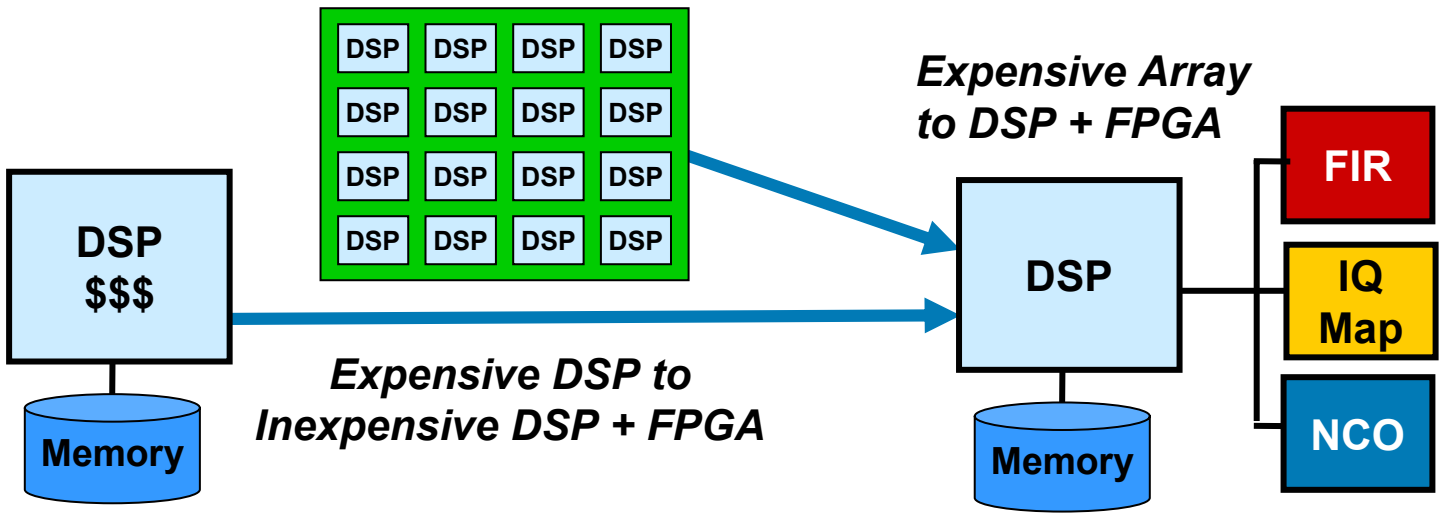


Processor External to FPGA



When Do FPGA Co-Processors Reduce System Cost?

- Off-Loading Algorithms to Co-Processor Reduces Number or Cost of Digital Signal Processors



- Applications
  - Algorithms with Large Amount of Digital Signal Processing & Small Amount of Control Processing

FPGA Co-Processor Applications

- Wireless
  - 2.5-G EDGE Equalization
  - 3-G Baseband Processing
    - HSDPA
    - 1xEVDV
  - 3-G RF Linearization
- Consumer
  - Broadcast - Studio & Cable Plant
  - Digital Entertainment – MPEG2 & MPEG4
- Medical
  - Imaging
- Wireline Communications
  - Encryption
  - Framer
  - Traffic Management
  - TCP/IP
- Computer & Storage
  - Data Analysis & Routing Engine
  - Digital Imaging
- Military & Aerospace
- Security

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DSP Development Tools & Design Methodology

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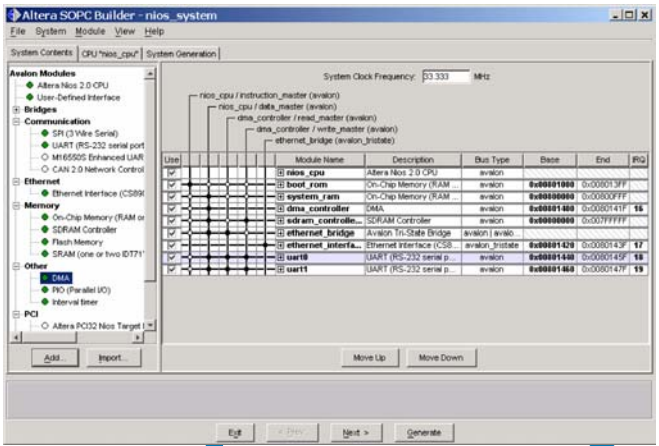
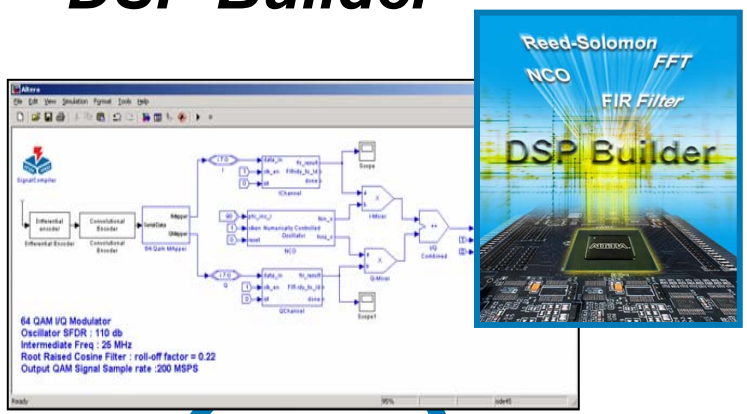
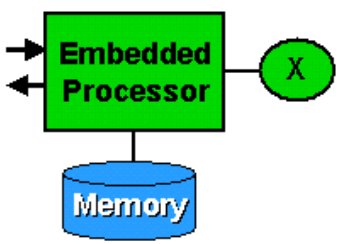
FPGA Co-Processor Design Tools

SOPC Builder

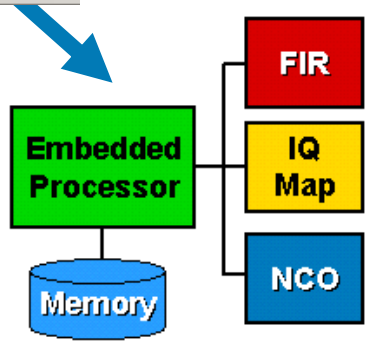


DSP Builder

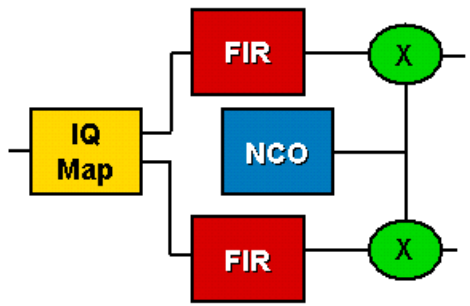




Stand-Alone Processor



Processor + Co-Processor



Dedicated Hardware Architecture

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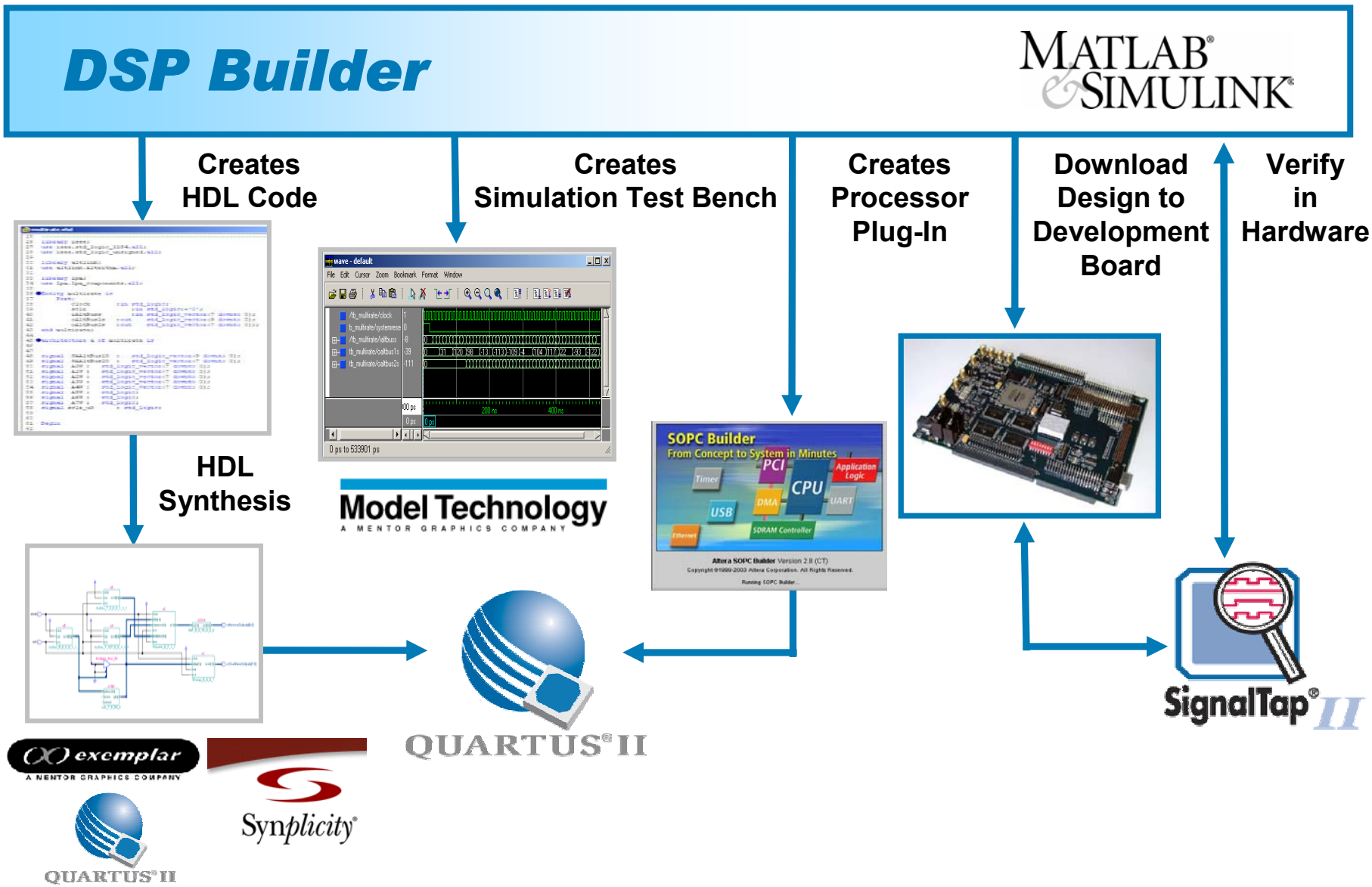
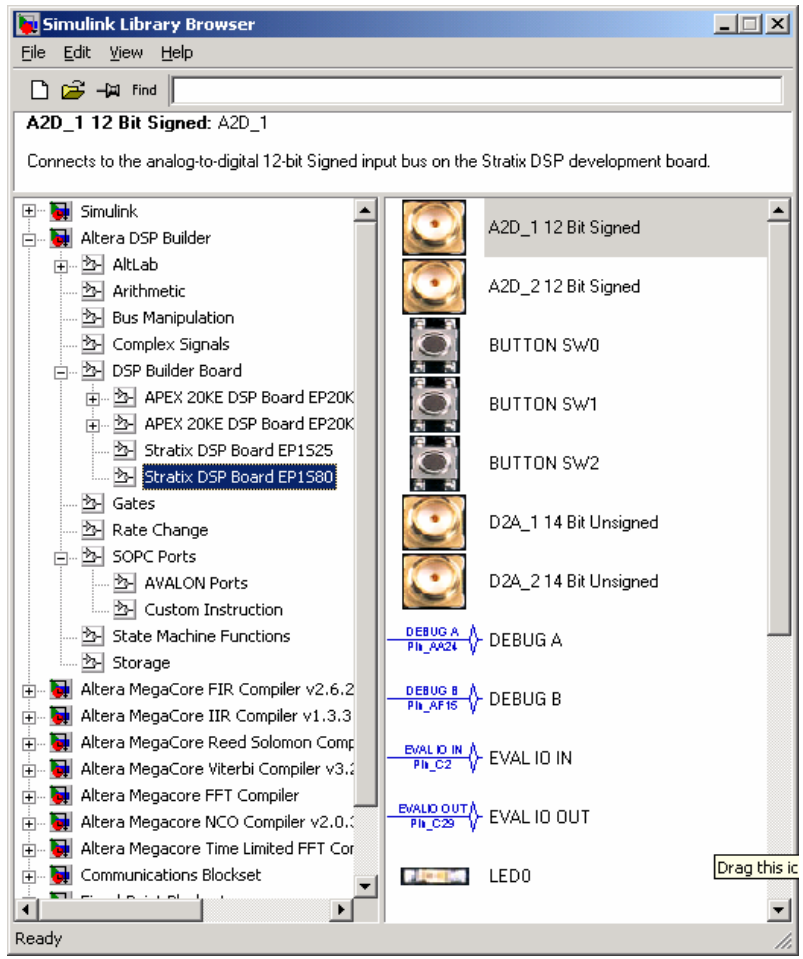
DSP Builder Overview



DSP Builder Library Components

- Arithmetic
- Bus Manipulation
- Complex Signals
- Logical Components
- SOPC Ports
- Storage
- MegaCore® IP
- Rate Change
- State Machine
- Altera Library
- DSP Board



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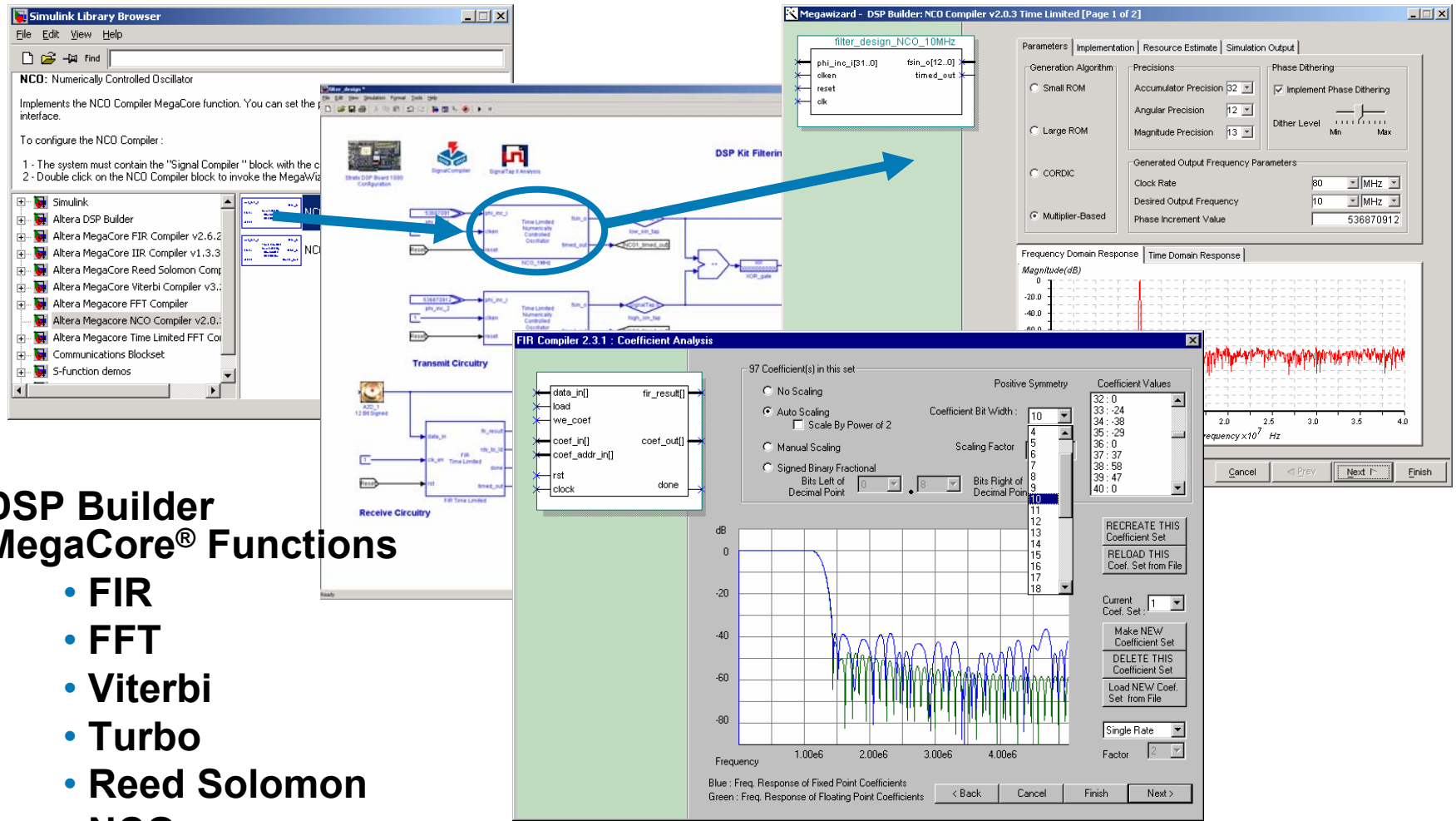
MegaCore IP in DSP Builder



DSP Builder MegaCore® Functions

- FIR
- FFT
- Viterbi
- Turbo
- Reed Solomon
- NCO

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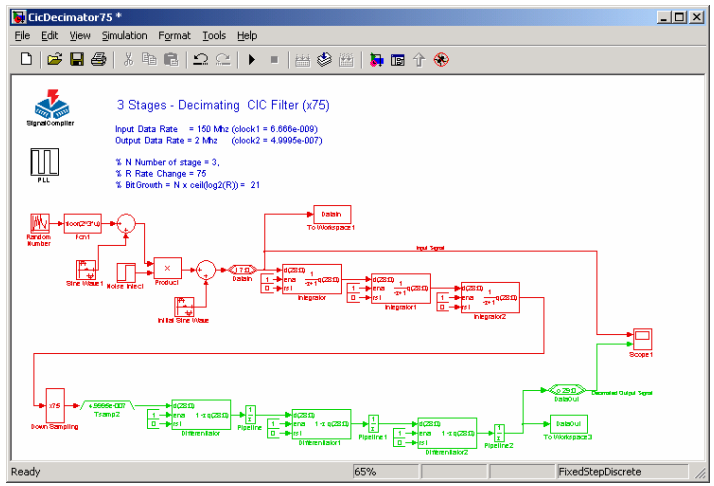
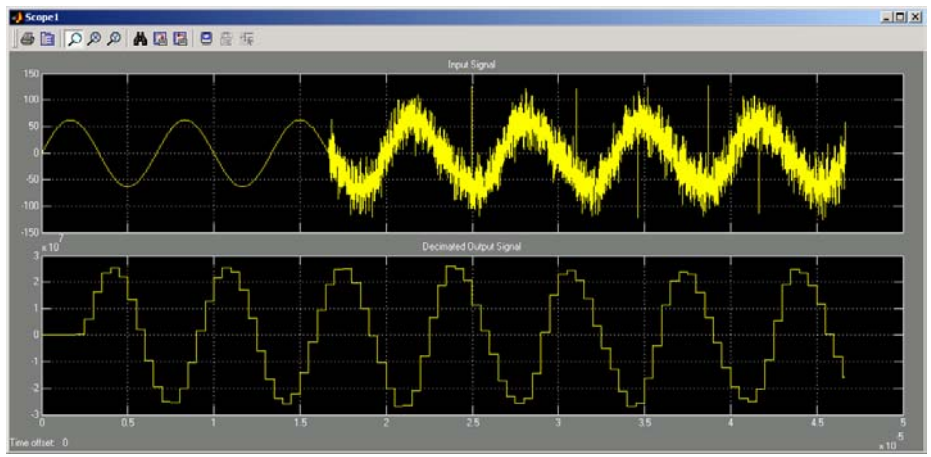
DSP Builder Support for Multiple Clock Domains

- Inherit Sampling Frequency (FS)
- Adhere to Clock Design Rules
- All Sample Times Match One of Phase-Locked Loops (PLLs) Output Clock Periods
- Simplify Analysis & Implementation of Multi-Rate System
  - Up Sampling
  - Down Sampling





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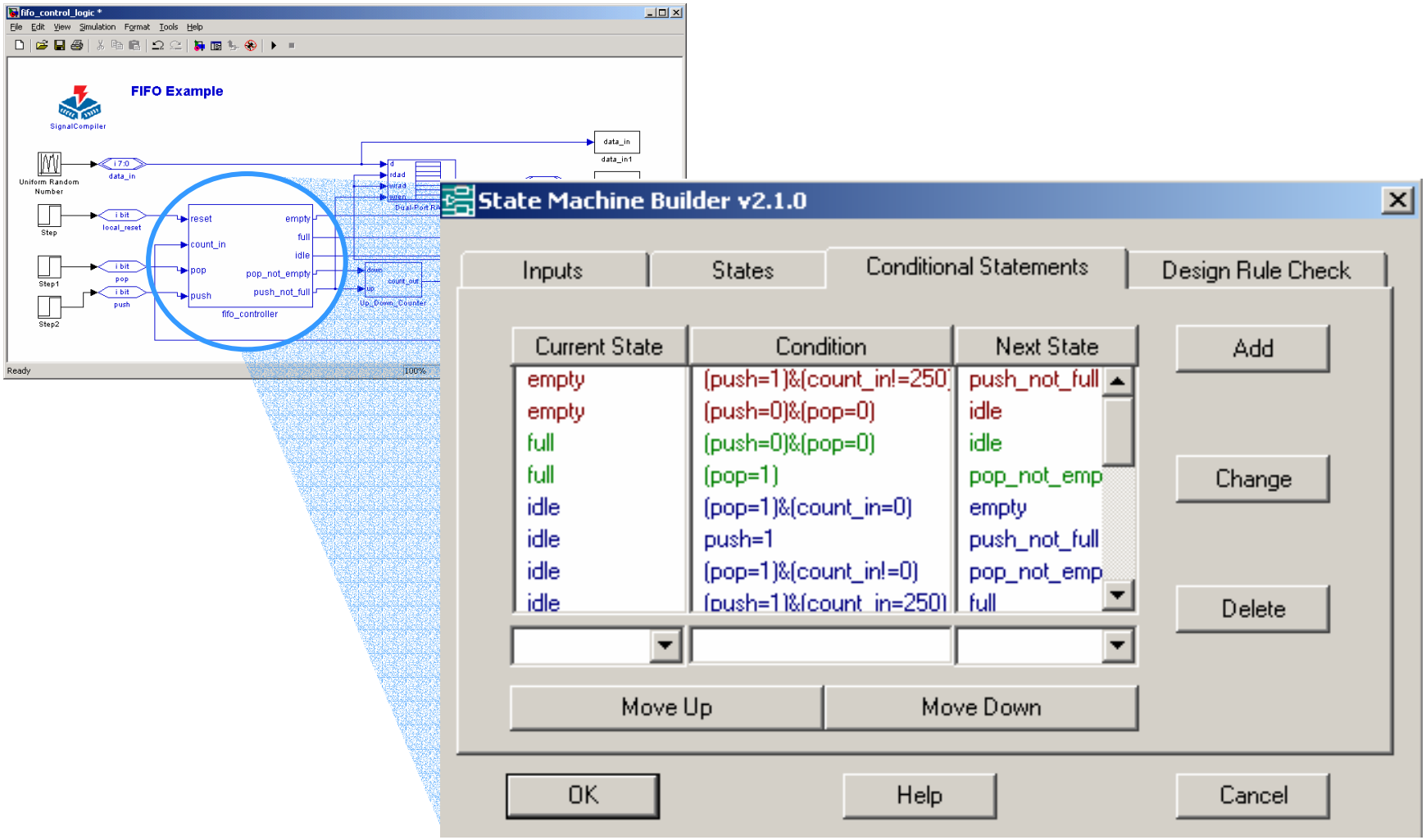
State Machine Builder



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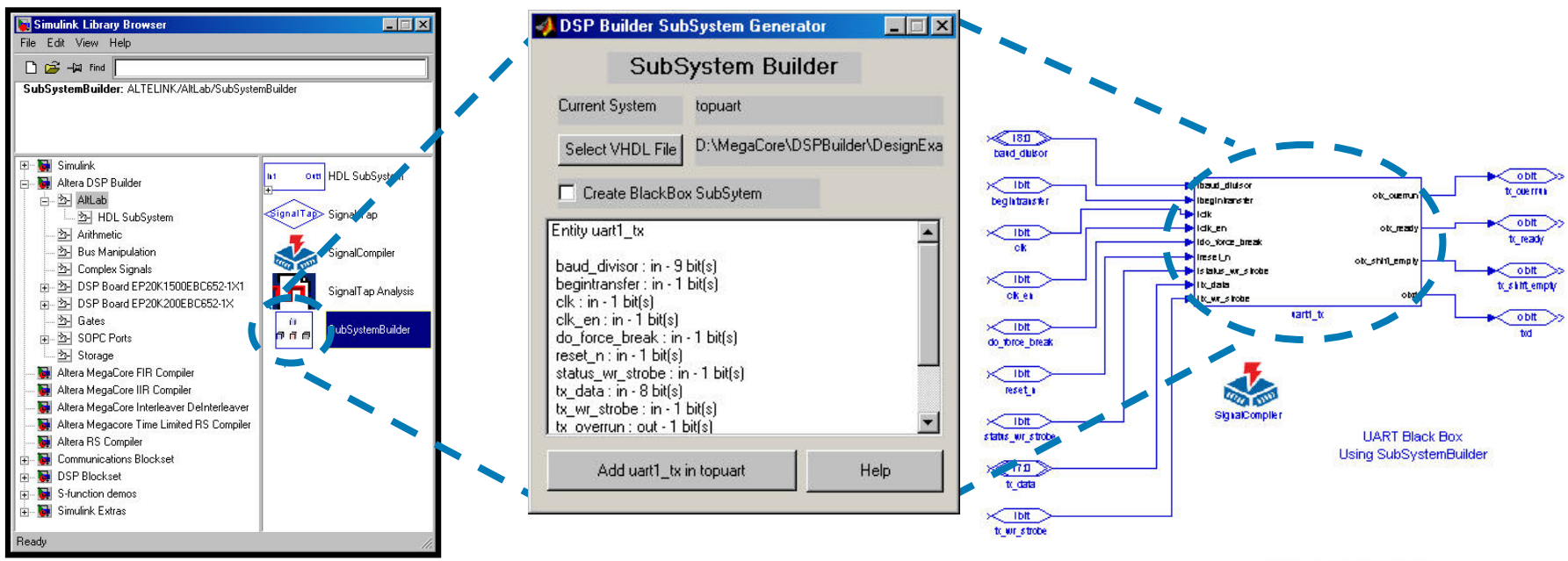
Sub-System Builder

- Import Existing VHDL Design into Simulink
- Simulink Simulation Options
  - Convert into DSP Builder Blocks or MATLAB Functions
  - Treat VHDL Design as Black Box



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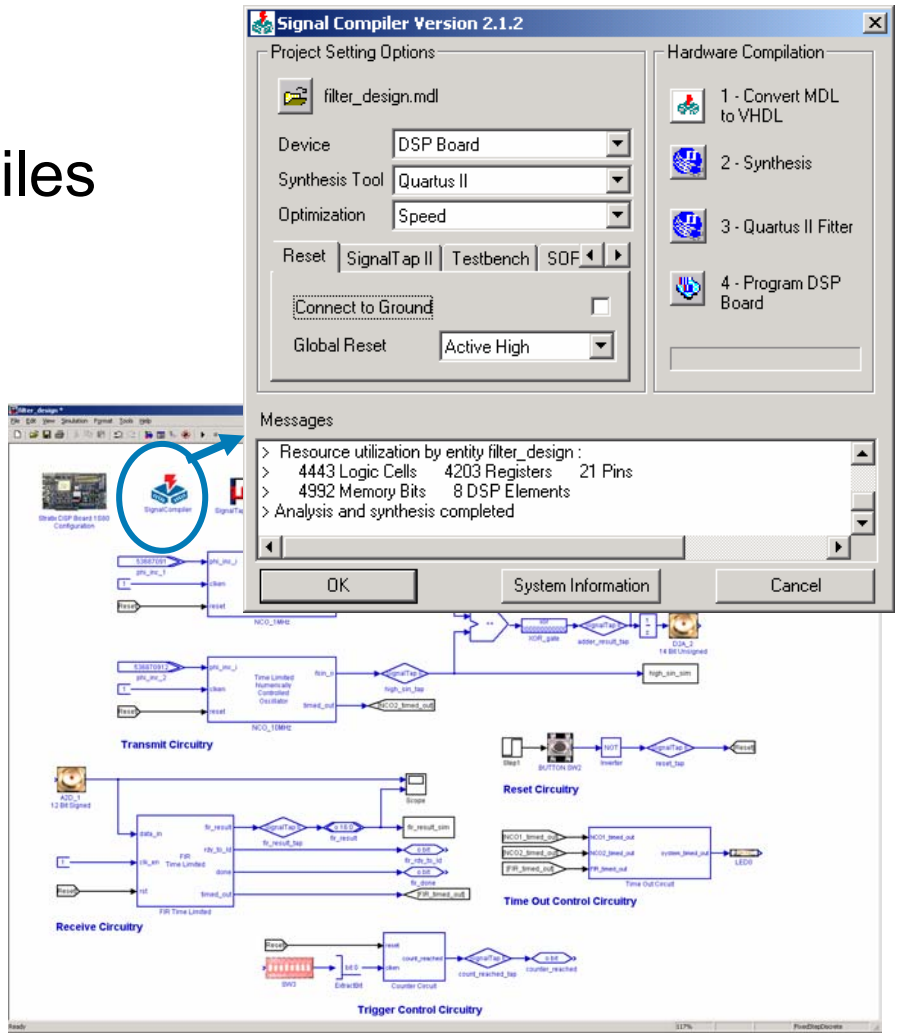
Signal Compiler

- Generates VHDL Design Files
- Generates Tool Command Language (Tcl) Scripts
- Generates Testbench
- Enables Parameterization of IP Blocks
- Launch Hardware Compilation from Simulink Cockpit



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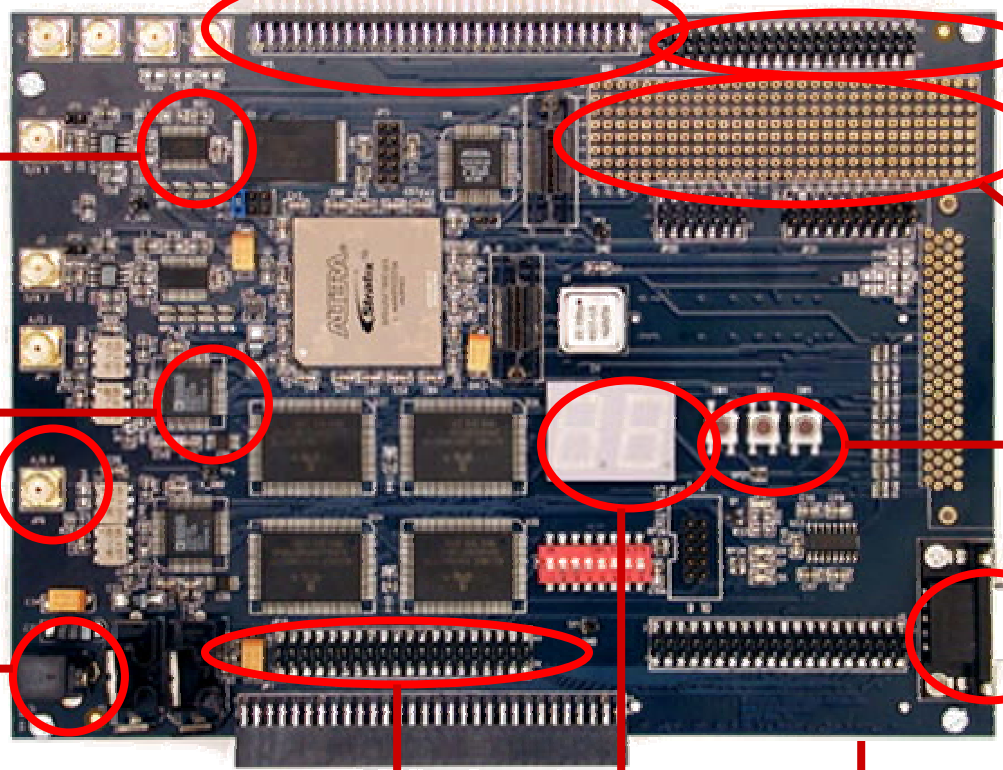
Stratix DSP Development Board



80-Pin I/O Connector

14-Bit, 165-MHz D/A

12-Bit, 125-MHz A/D

SMA Connector

5-V Power Supply

Altera® Nios® Expansion Prototype Connector

Prototyping Area

Push-Button Switches

9-Pin RS232 Connector

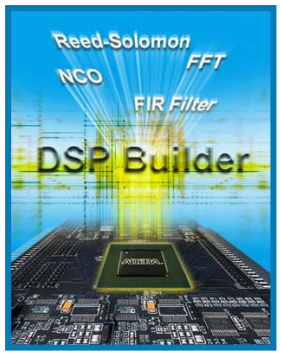
40-Pin Connector for Analog Devices Evaluation Boards

LEDs

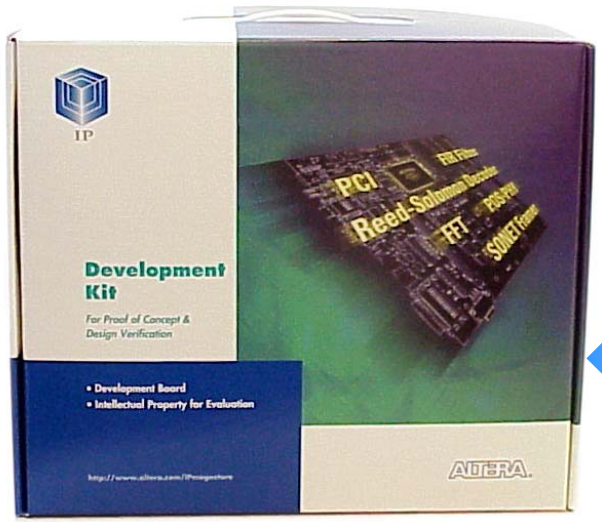
Texas Instruments Connectors Can Be Found on Underside of Board

Altera DSP Development Kits

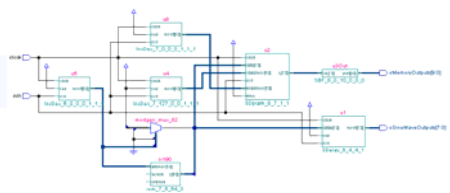
Contains Everything You Need to Develop High-Performance DSP Designs on FPGAs



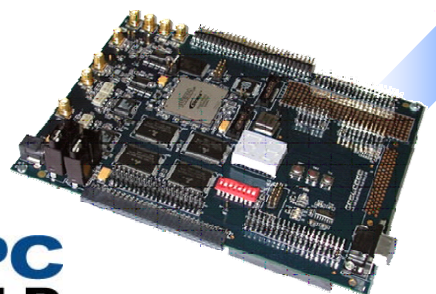
QUARTUS® II



30-Day Evaluation Version



System Reference Designs



OpenCore® plus

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QAM Modulator Co-Processor Design Example

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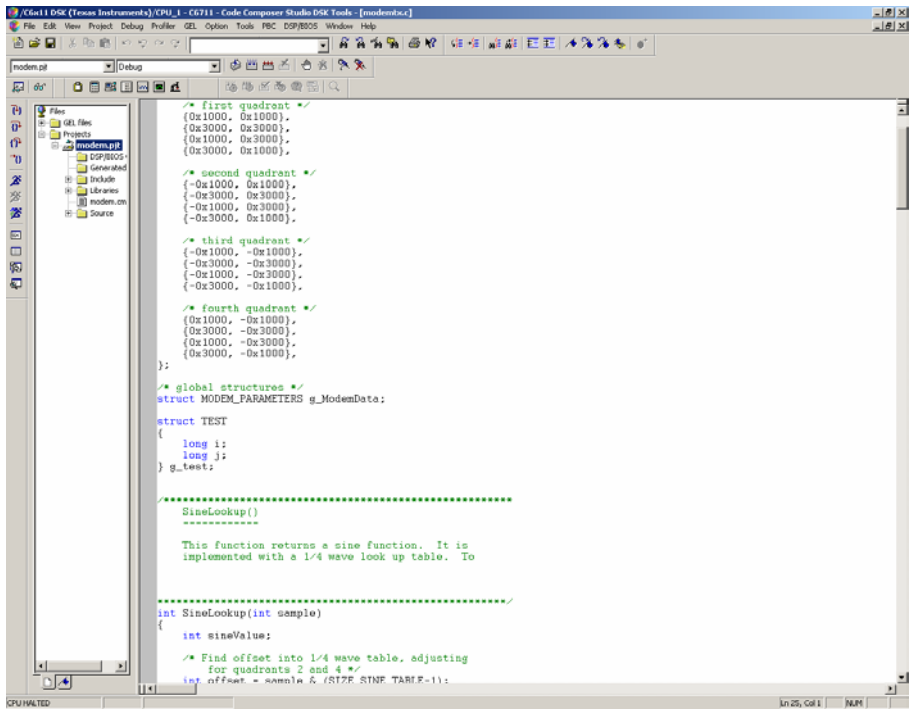
Modem Reference Design

- Installed with Code Composer Studio As a Tutorial
  - C:\ti\tutorial\dsk6711\modem
- Used to Demonstrate CCS Functionality
- 16 QAM TX Modem



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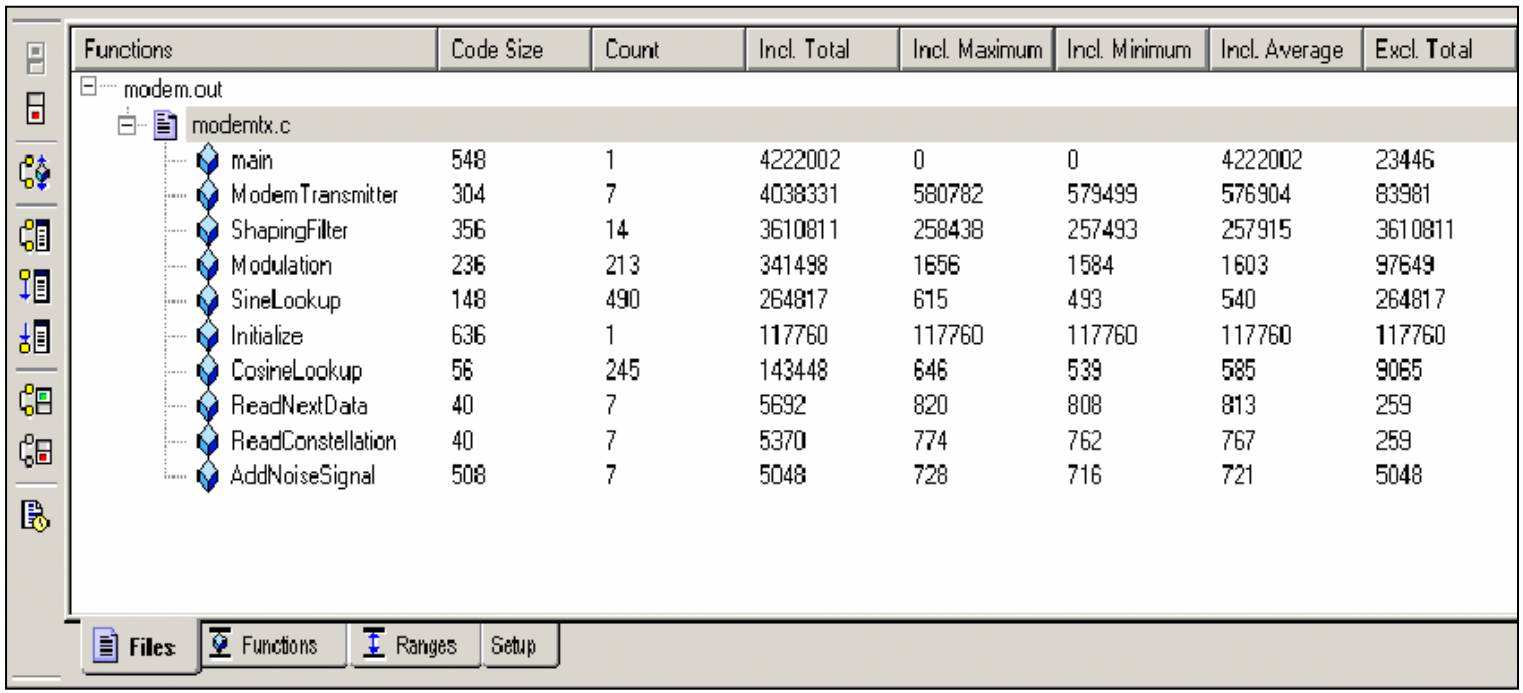
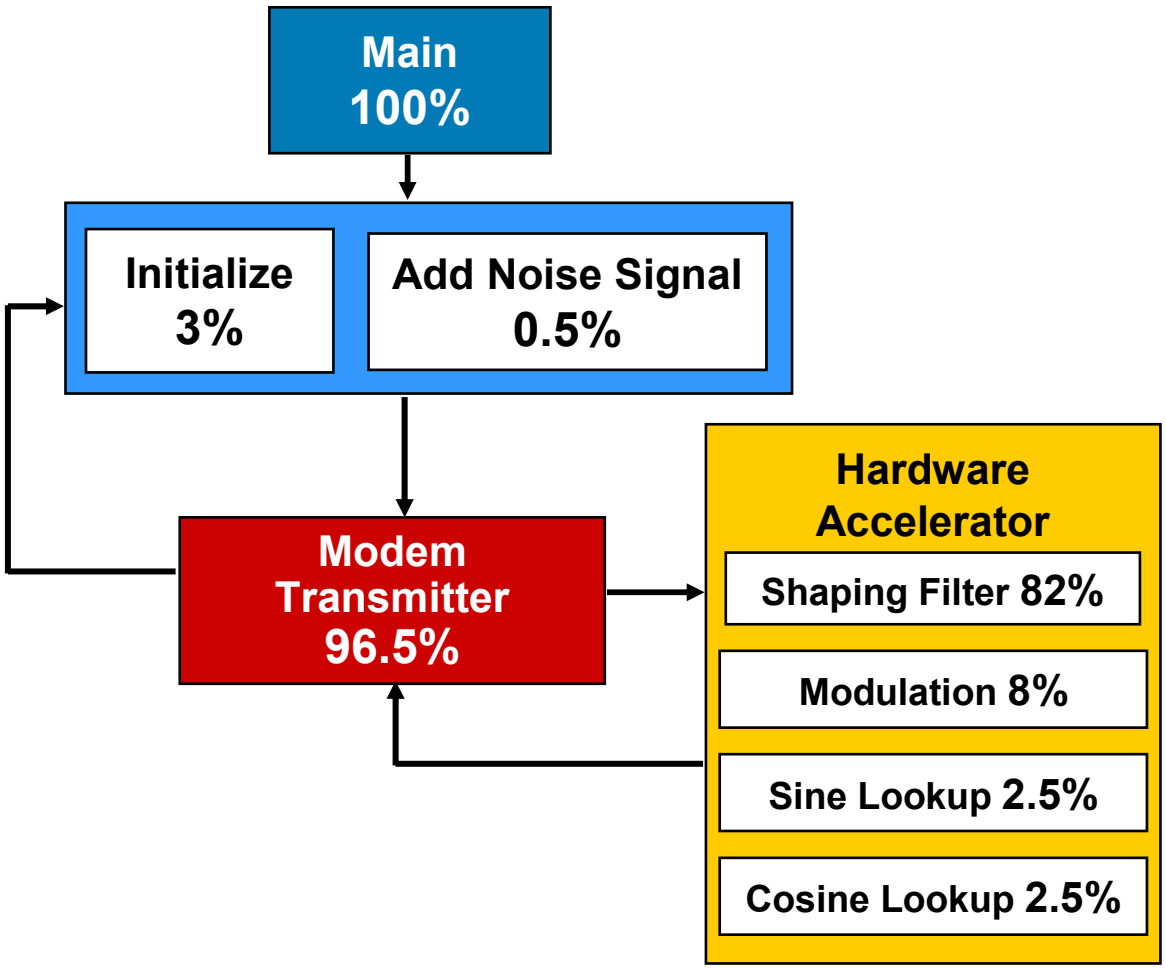
Modem Design Code Profile



Functions	Code Size	Count	Incl. Total	Incl. Maximum	Incl. Minimum	Incl. Average	Excl. Total
modem.out							
modemtx.c							
main	548	1	4222002	0	0	4222002	23446
ModemTransmitter	304	7	4038331	580782	579499	576904	83981
ShapingFilter	356	14	3610811	258438	257493	257915	3610811
Modulation	236	213	341498	1656	1584	1603	97649
SineLookup	148	490	264817	615	493	540	264817
Initialize	636	1	117760	117760	117760	117760	117760
CosineLookup	56	245	143448	646	539	585	9065
ReadNextData	40	7	5692	820	808	813	259
ReadConstellation	40	7	5370	774	762	767	259
AddNoiseSignal	508	7	5048	728	716	721	5048

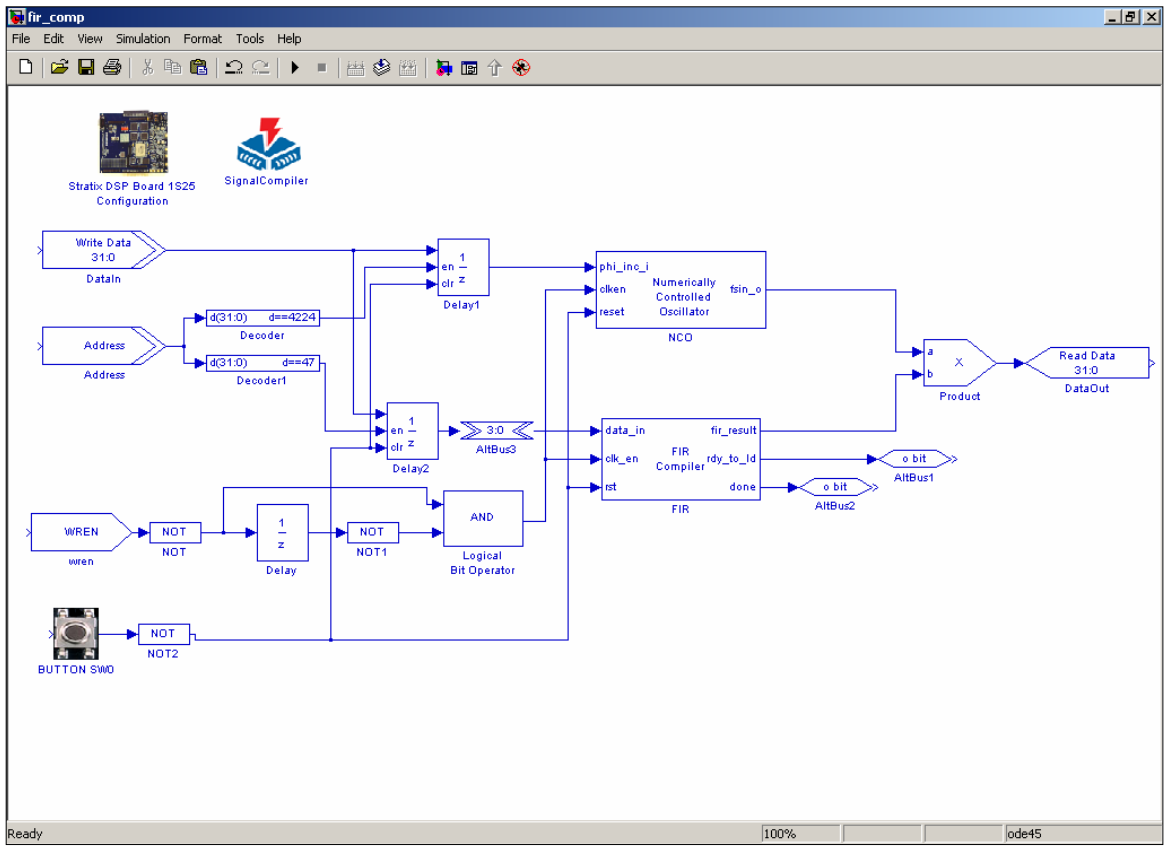
Files | Functions | Ranges | Setup

Modem Design Hardware/ Software Petition



Modulator Co-Processor

DSP Builder Used to Build Hardware DSP Data Path



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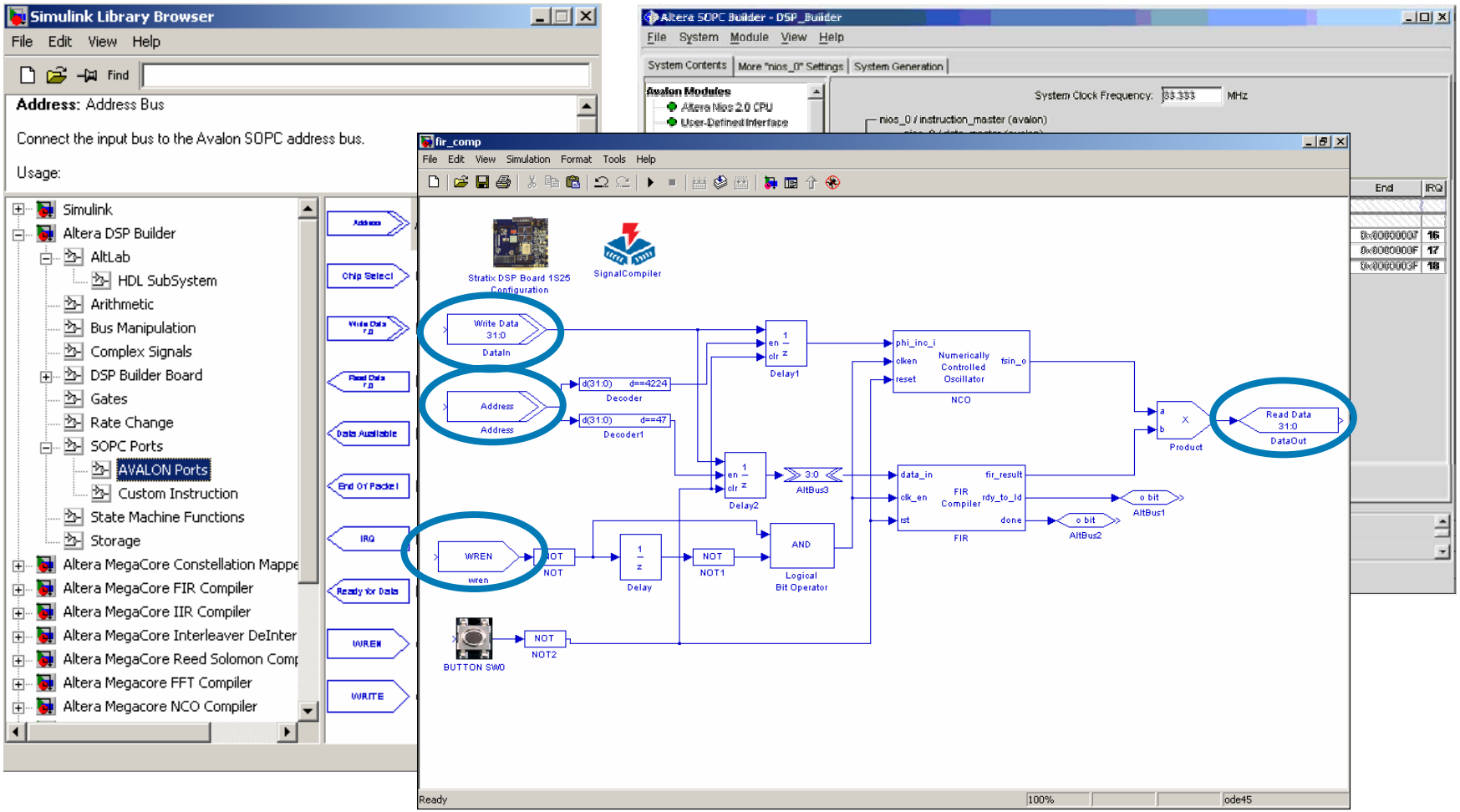
Avalon™ Interface in SOPC Builder



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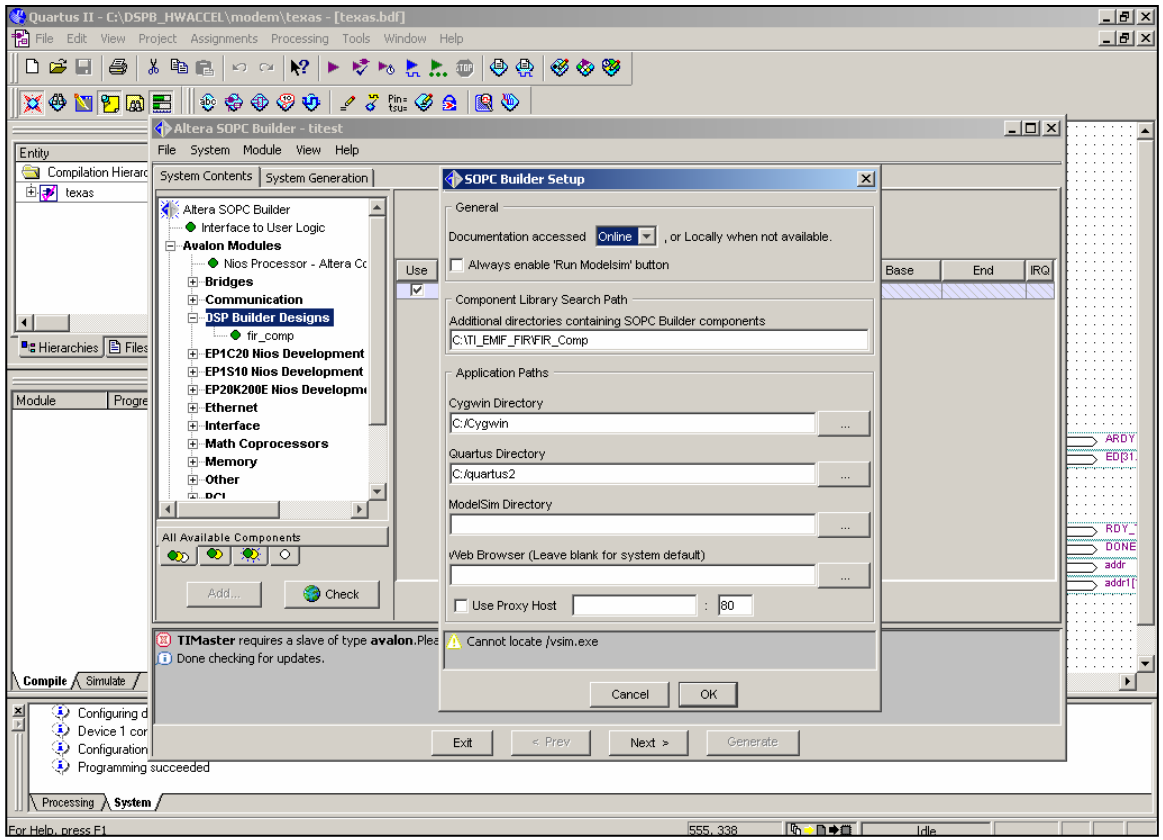
DSP Builder— SOPC Builder Import

Import DSP Builder Generated Co-Processor into SOPC Builder



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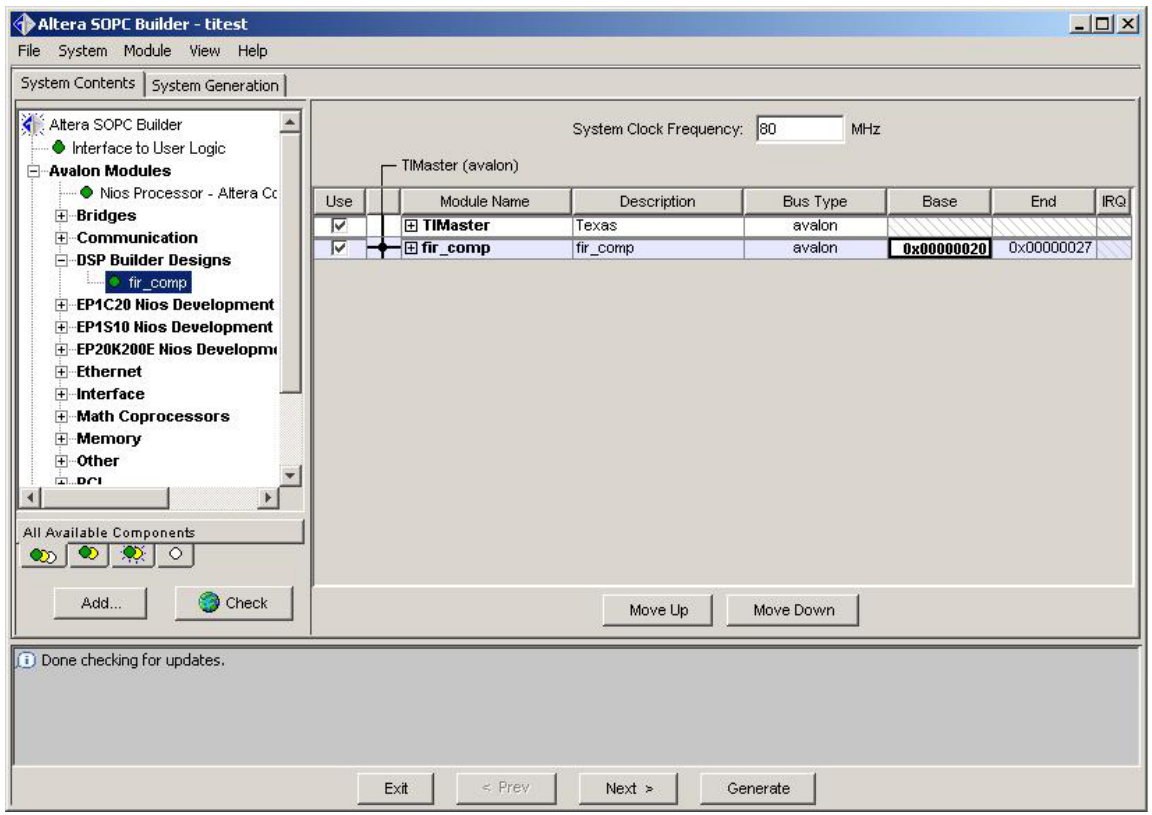
SOPC Builder Integration

Modem Co-Processor (fir_comp)
Integrated with TI EMIF I/F (TIMaster)



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FIR Filter Co-Processor Design Example

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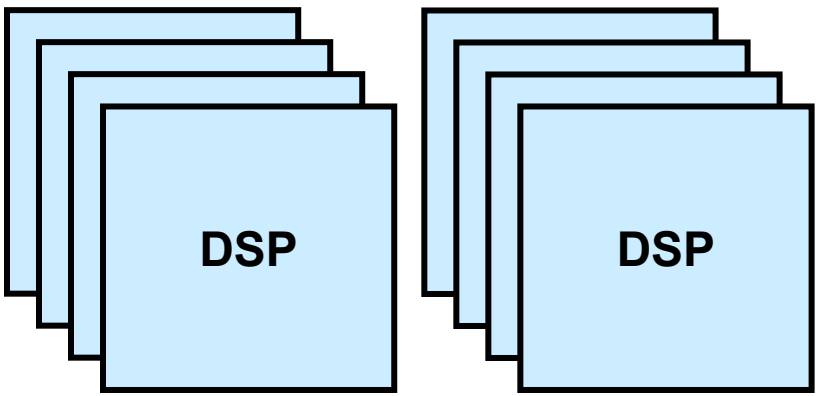
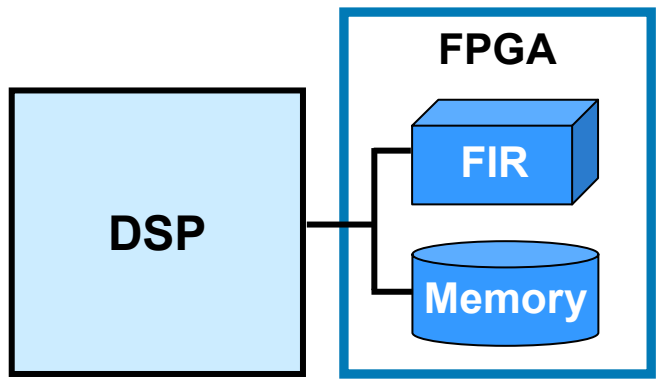
Driving Down System Costs

Multi-Processing DSP



Digital Signal Processor + FPGA Co-Processor



FIR Co-Processor Design Example

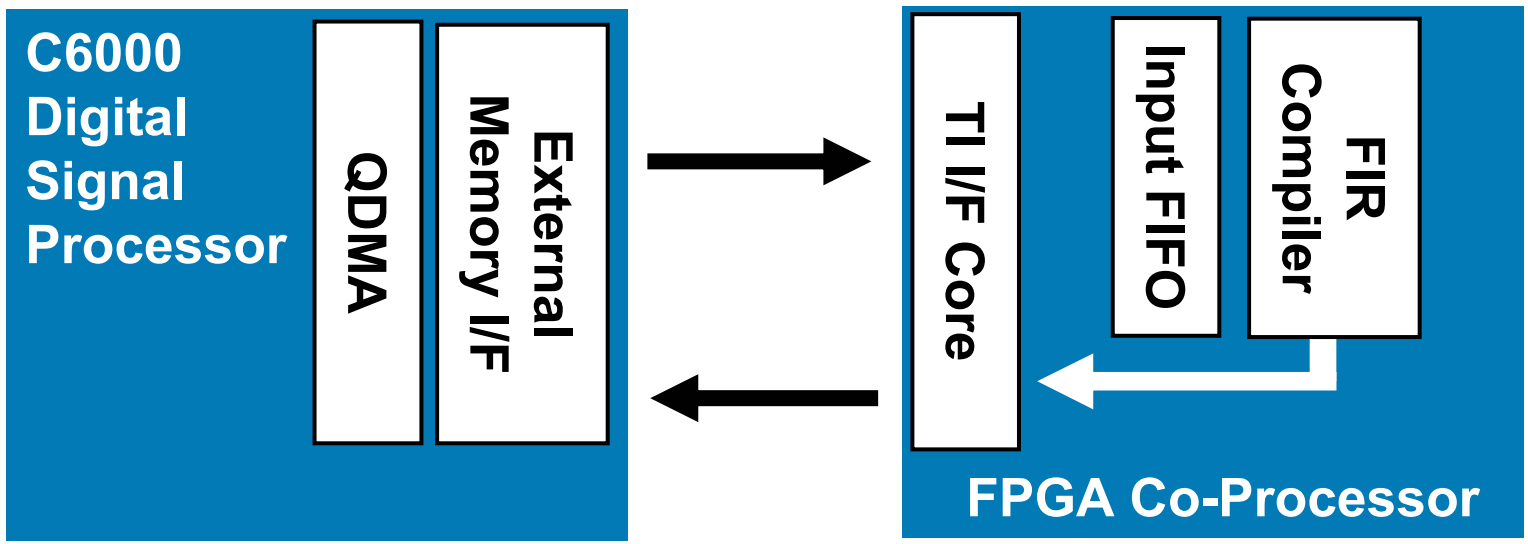
- FIR Parameters
  - 128-Tap
  - 16-Bit Data, 14-Bit Coefficients
- Four FIR Implementations for Comparison
  - TI C6711-Optimized TI DSPLib Function
  - TI C6416-Optimized TI DSPLib Function
  - Altera Eight-Cycle FIR Co-Processor
  - Altera One-Cycle FIR Co-Processor

TI Filtering Library (DSP Lib)

- C-Callable Optimized Assembly Routines
- TI C67x DSPLib: Fir Filter (Radix 8)
  - Formula: Nh * Nr /2 + 13
    - Nh = Number of Coefficients
    - Nr = Number of Samples
  - ~1 Sample/ 64 Cycles (128 Tap Filter)
- TI C64x DSPLib: FIR Filter (Radix 8)
  - Formula: Nh * Nr/4 + 17
  - ~ 1 Sample/ 32 Cycles (128 Tap Filter)

Filter Co-Processor Design Example

- Current Implementation
  - 100 MHz, 32-Bit, Asynchronous EMIF on DSK
  - TI Writes 300 Samples to Co-Processor (Input Data)
  - Filter & Send Output to TI

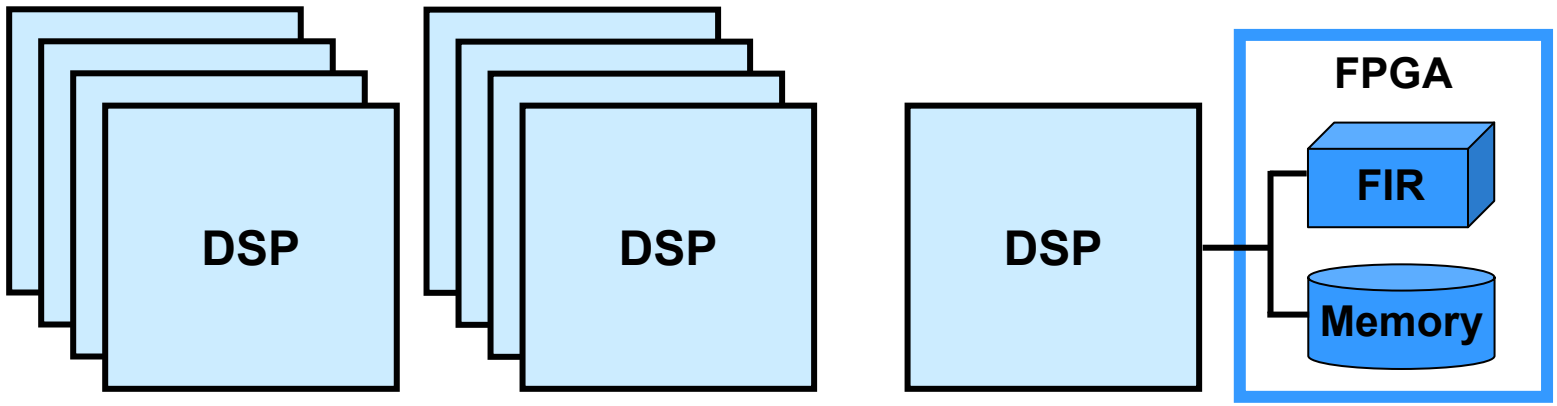


FIR Filter Example* – 16X Cost/Performance Improvement

Device	Solution	FIR Performance (MHz)	Device Cost****	Cost per FIR MHz
TI C6713-200	64-Cycles** at 200 MHz	3.125	$24.59	$7.87
TI C6416-600	32-Cycles** at 600 MHz	18.75	$160	$8.53
Altera EP1C3-8	7-Cycles*** at 200 MHz	28	$14	$0.50
Altera EP1C12-8	1-Cycle*** at 170 MHz	170	$84	$0.49

* FIR 128 Tap, 16-Bit Data, 14-Bit Coefficients
** DSPLib Optimized Assembly Libraries from Texas Instruments
*** Optimized MegaCore FIR Compiler from Altera
**** Pricing in Quantity of 100 at Arrow 6/25/03

14X Reduction in System Costs



Architecture	FIR Performance (MHz)	Total FIR Performance (MHz)	Device Costs	Total Cost
9 * TI C6416-600	9 * 18.75	167	9 * $160	$1,440
Altera EP1C12-8 + 1 TI c6713-200	170 + 3	173	$84 + $25	$110

Summary

- FPGA Co-Processors for DSP Offer Many Advantages
  - 10X Performance Boost
    - More Channels
    - More Complex Algorithms
    - Increased System Throughput
  - 10X Cost Reduction
    - Fewer Components
  - Complementary to DSP-Based Systems
    - Offloads Existing DSP
    - Integrates Into Existing DSP IDE
    - Evolution Not Revolution

Altera Code: DSP Solutions

- FPGAs
  - Stratix, Stratix GX, Cyclone
- Development Tools
  - DSP Builder, SOPC Builder
- Intellectual Property
  - FIR, FFT, Viterbi, Turbo, Reed Solomon, NCO
  - AMPP Third-Party Partners
- Development Kits
  - Altera
  - Third-Parties
- Design Services
  - ACAP Third-Party Partners
- Training

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