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ALTERA®

INNOVATION

SOPC WORLD 2003

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Advanced Clock Management Design Guideline

Clock Management & PLL Capabilities

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Agenda

- Stratix™ Clock networks
- Introduction to Stratix™ PLLs
- Stratix™ Enhanced PLL
- Advanced Features
  - Programmable Bandwidth
  - Clock Switchover
  - Spread Spectrum
  - PLL Reconfiguration
- Stratix™ Fast PLL

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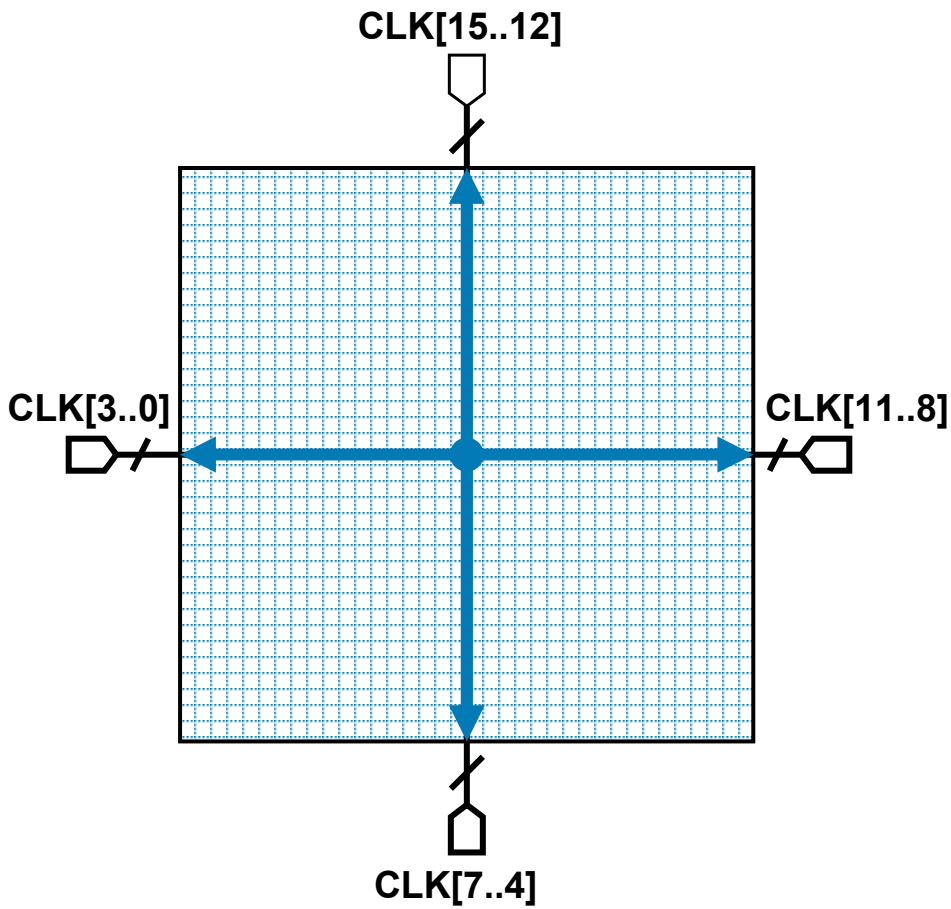
Global Clock Networks

- Sixteen Networks Feed Entire Device
  - 16 Dedicated Clock Input Pins
  - PLL Outputs
  - Internal Logic
- Used as Clock or Control Sources for All Device Structures & Blocks



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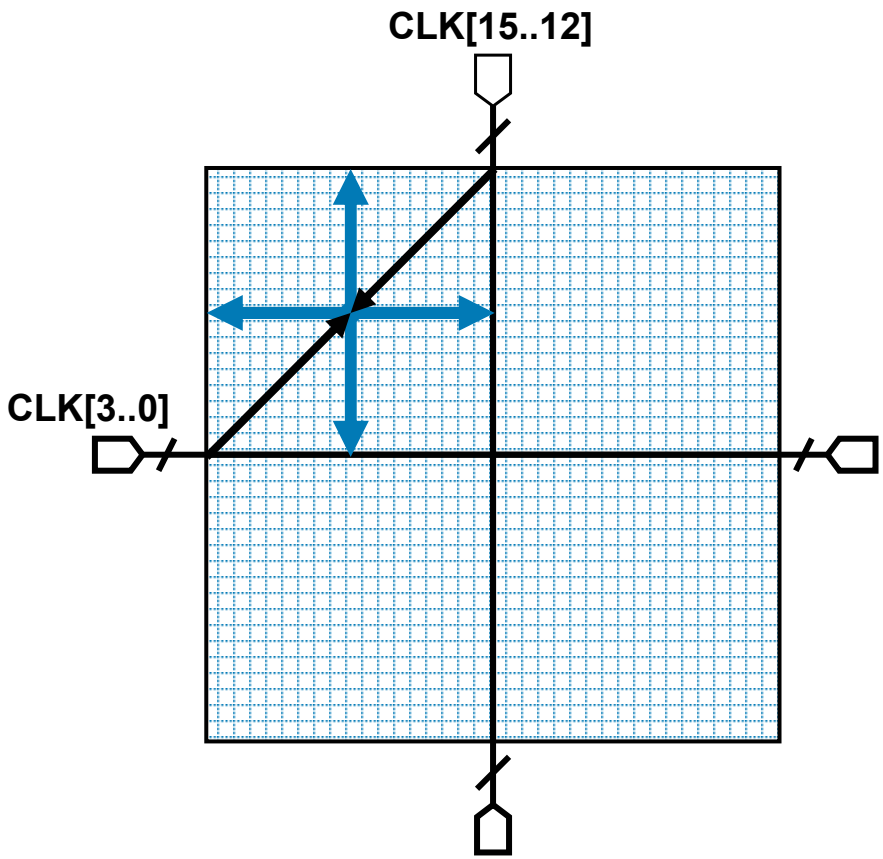
Regional Clock Networks

- Four Networks that Feed Single Device Quadrant
  - 16 Dedicated Clock Input Pins
  - PLL Outputs
- Lowest Clock Delay & Skew within Quadrant



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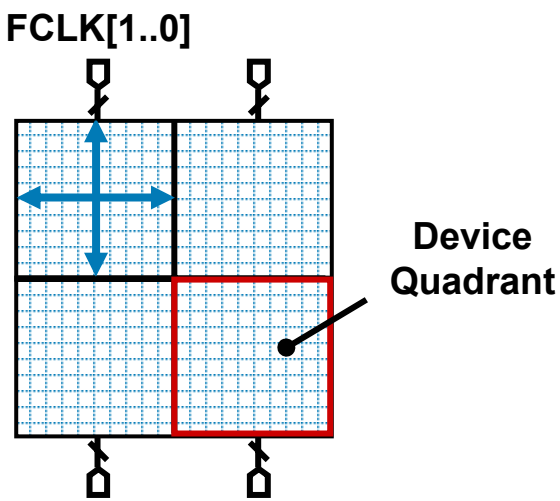
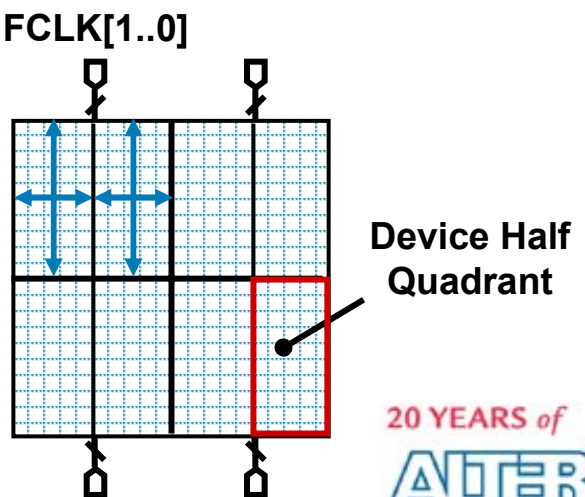
Fast Regional Clock Networks

- Fastest t_{CO} & t_{SU}
  - Ideal for Localized Clock & Control Signals
- 8 Input Pins per Device
  - EP1S10, EP1S20, EP1S25 & EP1S30: 8 Clock Networks
  - EP1S40, EP1S60, & EP1S80 : 16 Clock Networks

EP1S10, EP1S20, EP1S25 & EP1S30



EP1S40, EP1S60, & EP1S80



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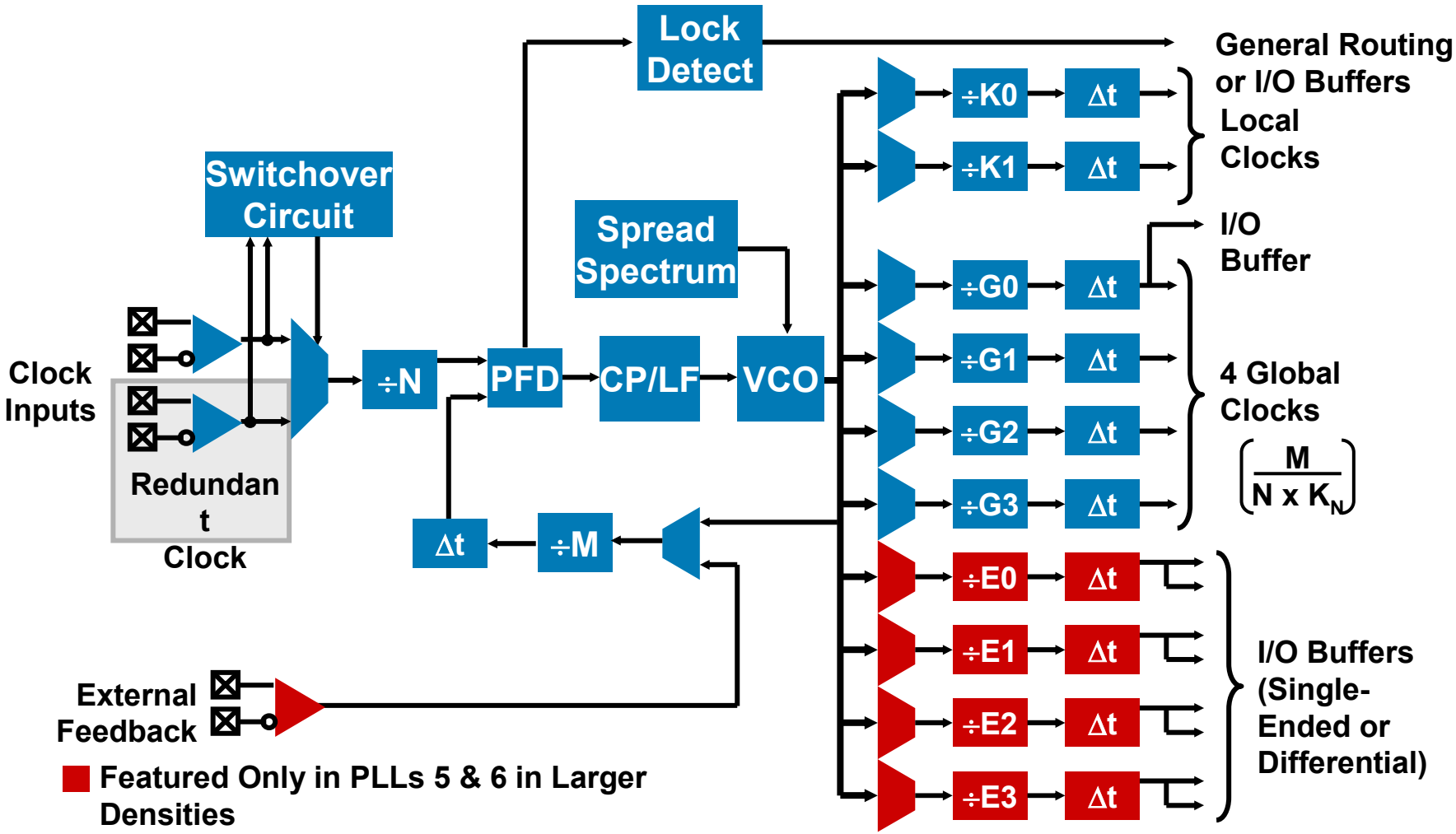
Stratix Enhanced PLL Details



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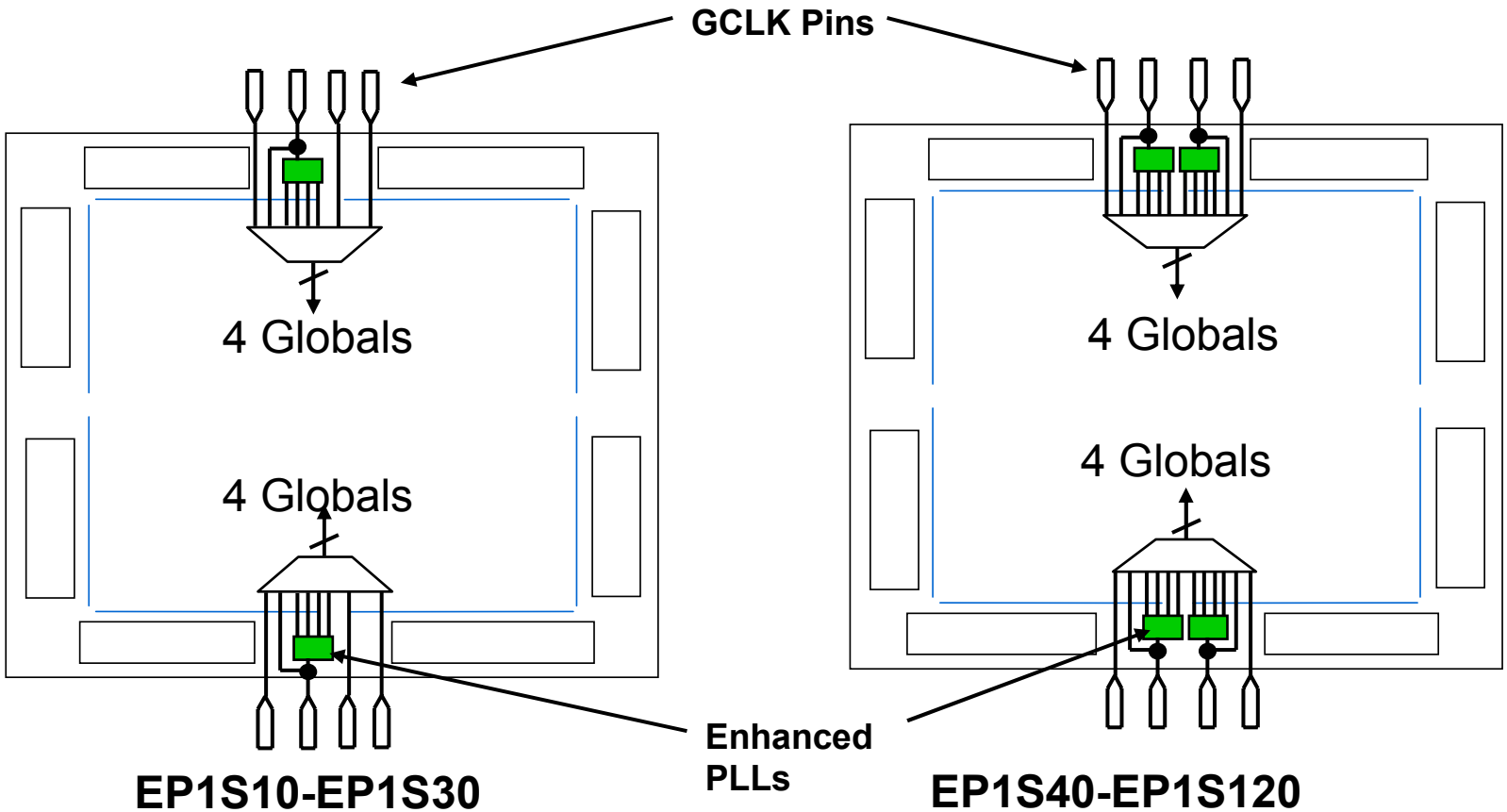
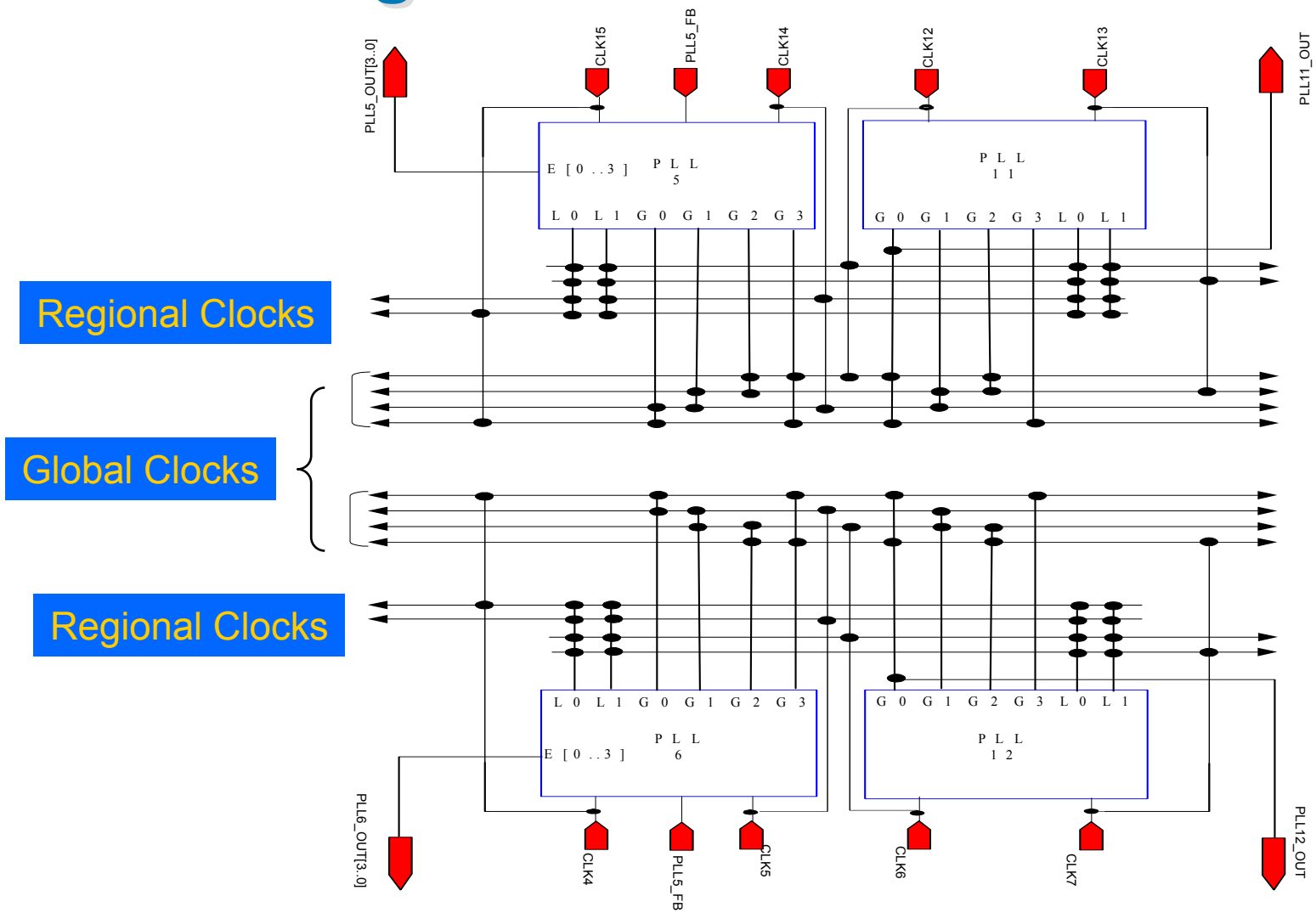
Stratix Enhanced PLL

- Total of 8 Global Outputs From Enhanced PLLs
  - Additional Outputs Allowed Via 8 Regional Clocks



Global & Regional Clock Connections



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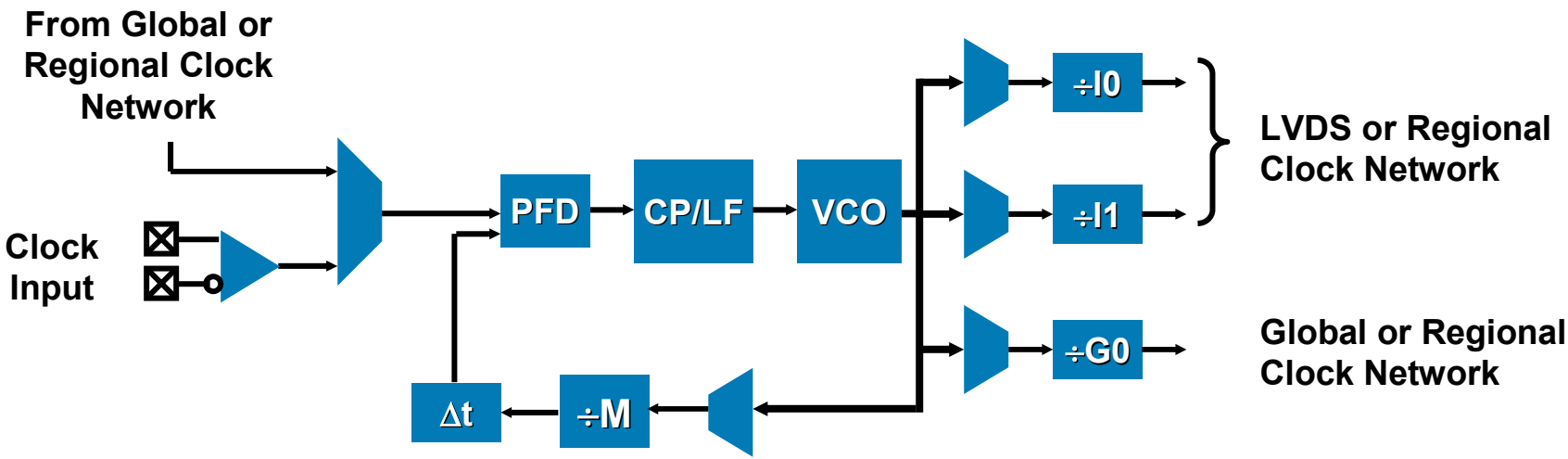
Stratix Fast PLL Details



PLL Resources per Device

Device	Fast PLLs	Enhanced PLLs	Total Number of Distinct Frequencies	Total Number of Taps	Total External Outputs *(1)*
EP1S10	4	2	32	40	16
EP1S20	4	2	32	40	16
EP1S25	4	2	32	40	16
EP1S30	8	2	44	52	16
EP1S40	8	4	56	66	16
EP1S60	8	4	56	66	16
EP1S80	8	4	56	66	16

(1) Excludes Fast PLL External Outputs Using High-Speed Differential I/O Channels

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Stratix Enhanced PLL Features

Feature	Description
Off-Chip Output Clocks	16 Single-Ended / 8 Differential per Device
Multiplication/Division	$f_{OUT} = f_{IN}\left(\frac{M}{N \times K_N}\right)$ M, N: 1 to 512 K: 1 to 512
Programmable Phase	Adjustable in Steps as Small as 160 ps
Programmable Delay	250 ps Increments (Up to ± 3 ns)
PLL Reconfiguration	M, N, K & Delay Parameters Change on the Fly
Programmable Lock Detect	User-Specified Lock Signal Assertion
Programmable Bandwidth	Adjustable Bandwidth (200 KHz to 1.5 MHz)
Clock Switchover	Backup Clock During Loss-of-Lock
Output Clock Enable	Output Clock Enable on Each Output Counter
Phase Frequency Detector (PFD) Enable	Enable/Disable PFD Outputs
Spread Spectrum Clocking	Reduction of Electromagnetic Interference

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New Features

- PLL Reconfiguration
  - Allows Changing of M, N, & K_N (G, L, E) Counters & Delay Elements without Cycling Power
- Clock Switchover
  - Provides Primary & Secondary Clocks for Loss-of-Lock/Clock Conditions
- Spread Spectrum
  - Modulate Output Frequency in a Controlled Manner to Reduce EMI Emissions
- Programmable Bandwidth
  - Customizes Bandwidth Characteristics to Better Suit End Application (200kHz – 1.5MHz)

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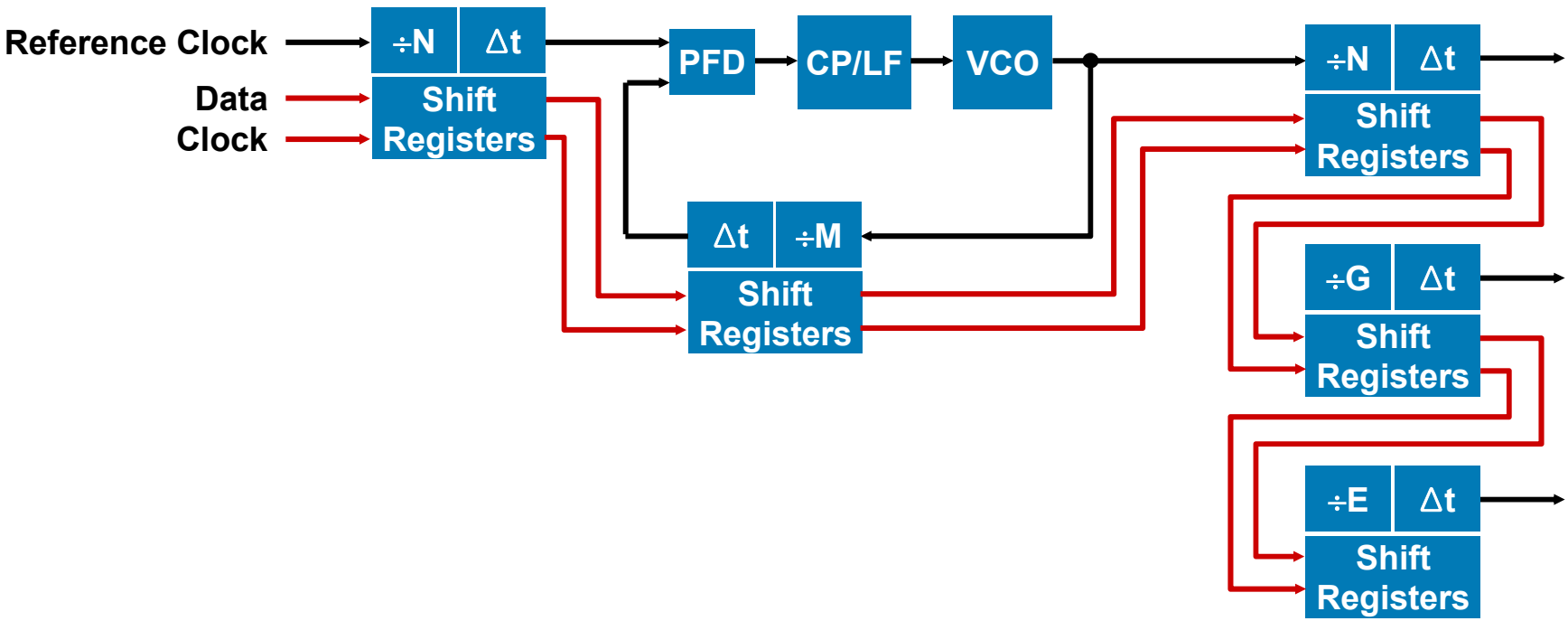
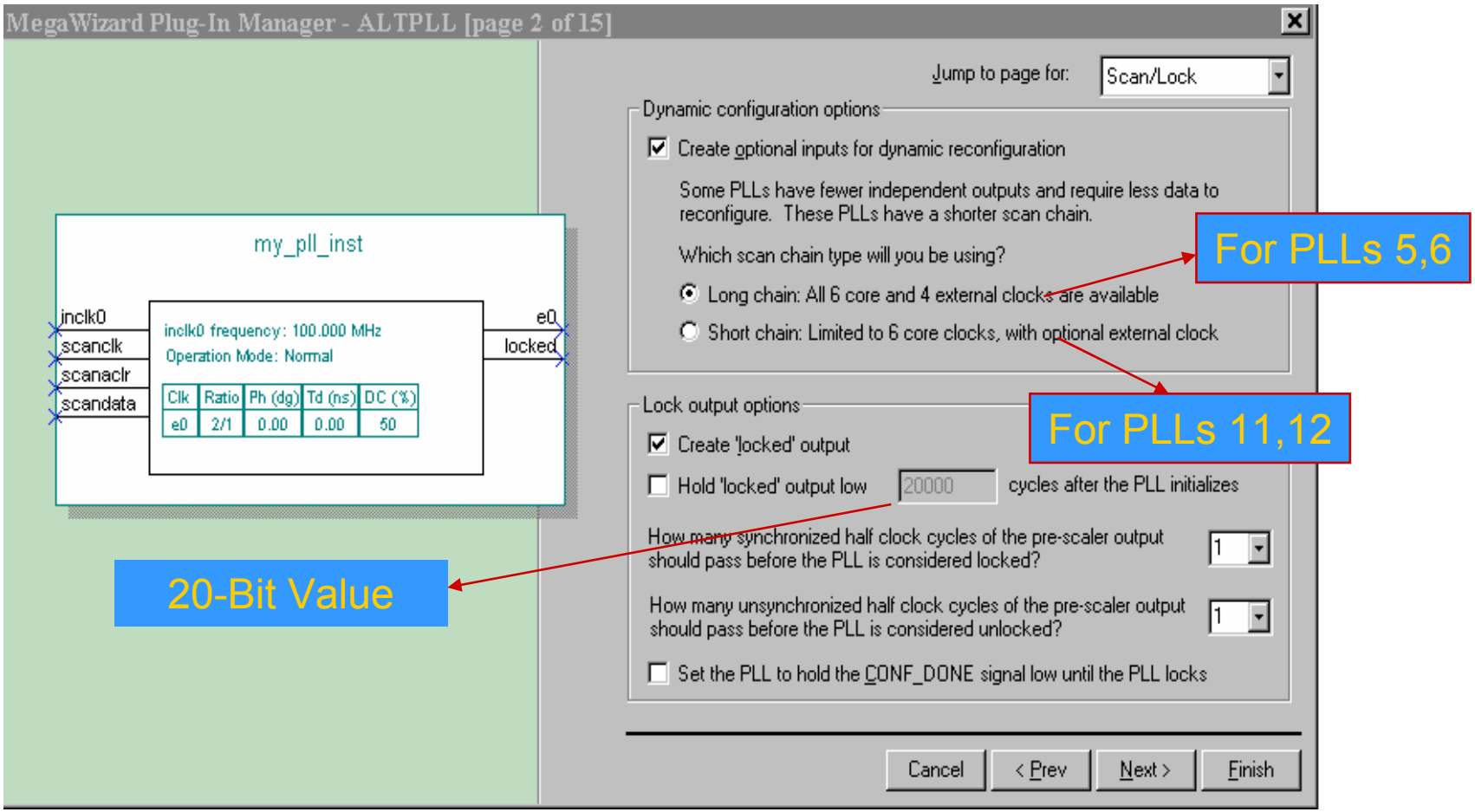
PLL Reconfiguration

- **Real-Time Reconfiguration of PLL Parameters**
  - Used in Applications that Require Real-Time Variations in Output Frequency & Delay
  - Reconfigured Serially Using General Routing Resources or I/O Pins
  - Requires Less than 100 us Using 25-MHz Clock



Quartus II MegaWizard Plug-in



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Design Guidelines

- Delay Elements May Also Be Changed
  - Should Change Slowly
    - Sudden Large Changes Can Result in Glitching
  - If Delay Is in the PLL Loop, Resynchronization Will Have to Occur
- Allows User to Dynamically Shift Clocks
  - VCO and Counter Phase Changes Can Only Be Made Through POF

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Design Guidelines

- Recommended Reconfiguration Sequence
  - Disable PLL Outputs
  - Scan-in New Counter and Delay Element Settings Using *SCANCLK* and *SCANDATA*
  - Restart the PLL Using *ARESET*
  - Monitor *LOCK* Output From PLL
  - Enable PLL Outputs After Lock

  Don't Have to Worry About Glitches Due to Large Increments!

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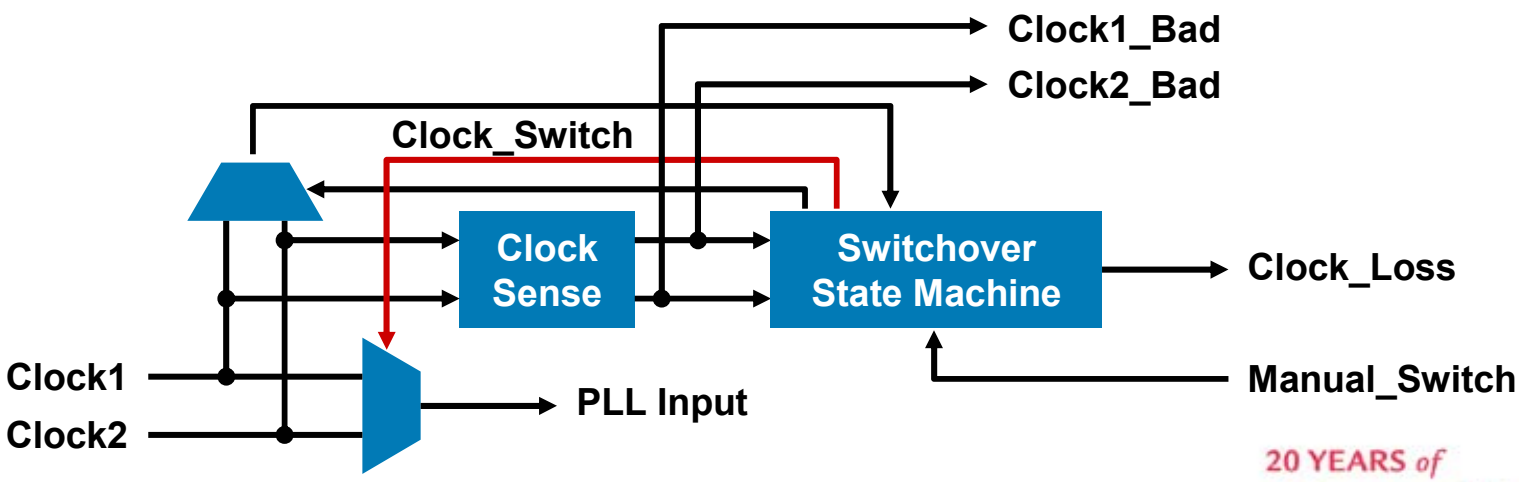
Clock Switchover

- Useful in High-Reliability Systems Requiring Backup Clock
  - Automatic Switchover Achieved with Clock Sense Circuitry
- Can Also be Used in Multi-Frequency Systems
  - Manual Switchover
- VCO Continuously Running
  - Frequency Decreases Until Secondary Clock is Locked



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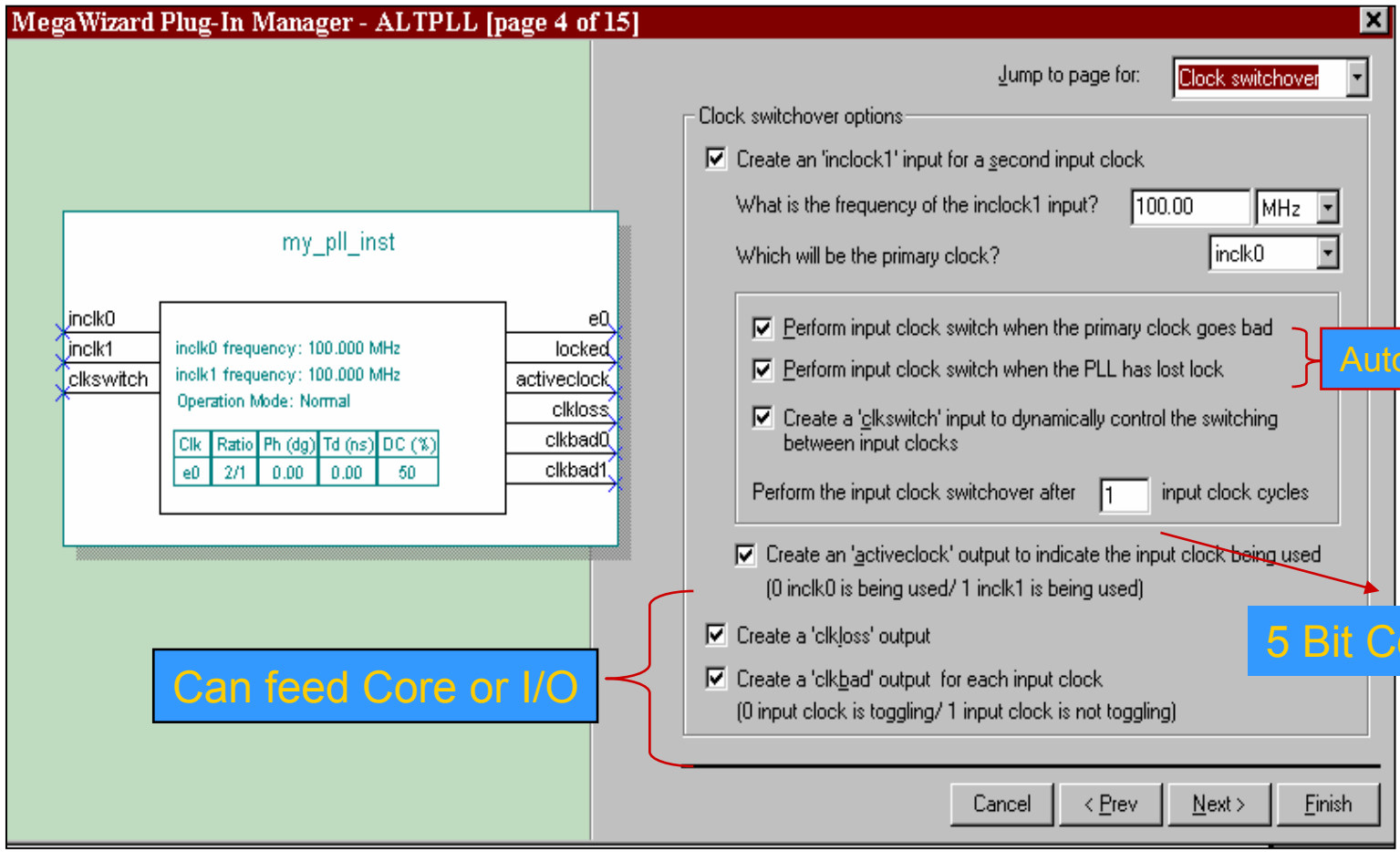
Quartus II MegaWizard Plug-in



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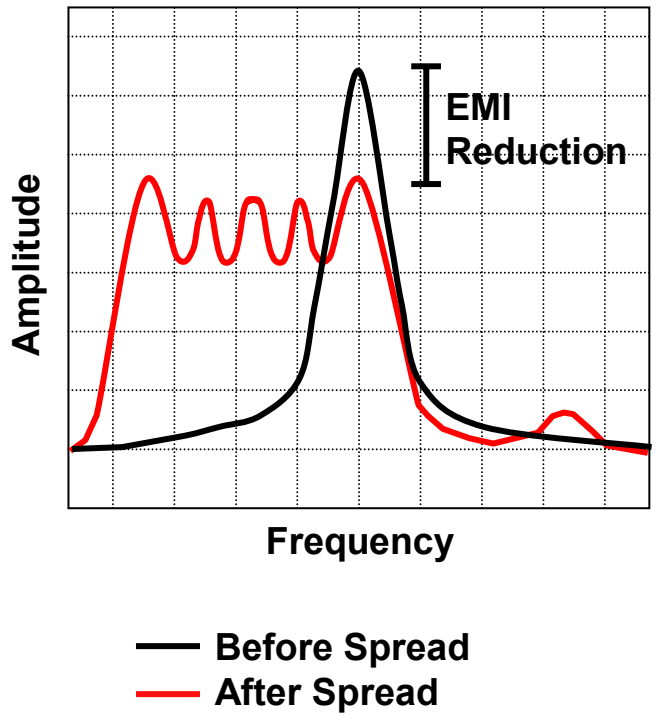
Control Signals

- Clk0bad, Clk1bad
  - Output From Clock Sense Circuit to Indicate When One of the Clocks Has Gone Bad
- Active Clock
  - Indicates Which Clock Is Driving the PLL. ‘0’ for Inclk0 and ‘1’ for Inclk1
- Clkloss
  - A ‘0’ Indicates That the Primary Clock Has Stopped Running

The Need for Spread Spectrum

- High-Speed Clocks Generate Significant Amount of Energy
  - Concentrated in Narrow Frequency Range
  - Results in High Peak Electromagnetic Interference (EMI) Emissions
- Peak EMI Emissions Must be Reduced to Meet FCC Regulations
  - Common Techniques Include Shielding
    - Significant Design Costs Associated with Reduction Measures



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Stratix Spread Spectrum

- Significantly Reduces EMI Emissions
  - Minimizes Costs Associated with Reduction Measures
- Modulates the Target Frequency over a Small Range
  - Redistributes Energy over Wider Band of Frequencies
- Provides up to 0.5% Downspread
  - Triangular (Linear) Modulation of 100 to 500 KHz
  - 4 to 6 dB Reduction in Peak Energy
- Affects All PLL Outputs

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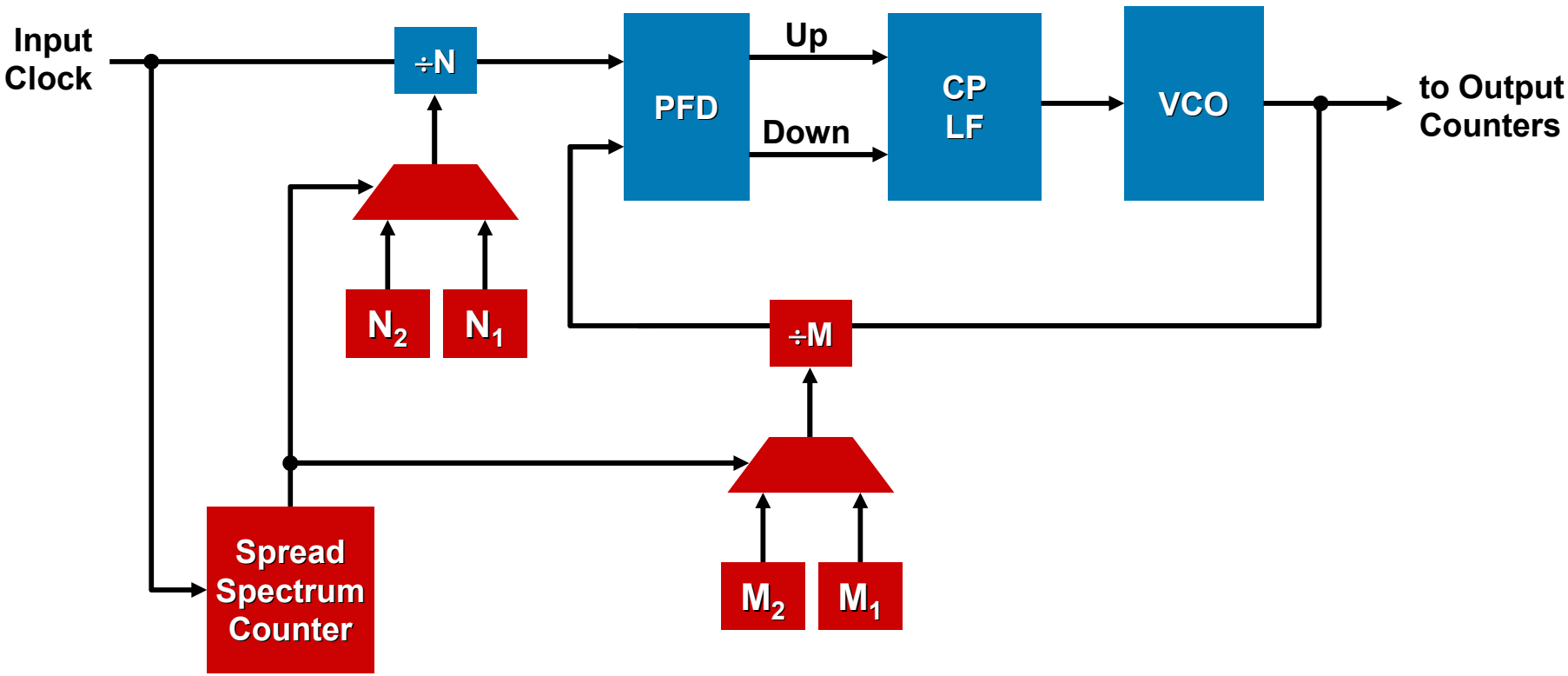
Spread Spectrum Implementation



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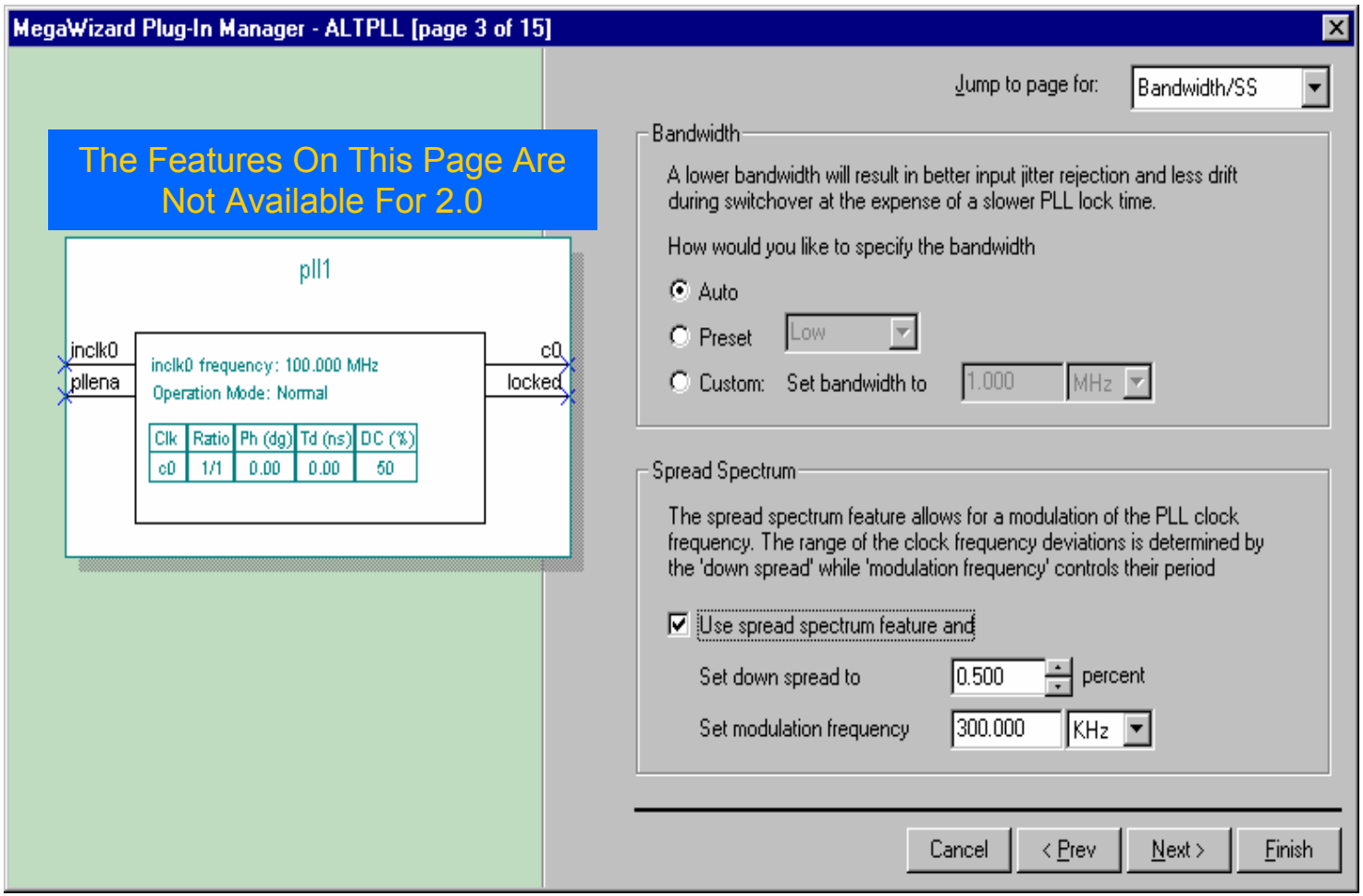
Quartus II Megawizard Plug-in



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Design Guidelines

- All PLL Outputs Are Affected
  - Spread Spectrum Modulates the M Counter Value
- OK to Use With Clock Switchover
- Cannot Use the Programmable Bandwidth Feature With Spread Spectrum
  - If Using One Feature, the Other Option Will Be Grayed Out in the Megawizard

Design Guidelines

- Cascading PLLs That Use Spread Spectrum
  - The Downstream PLL, Receiving the Spread Spectrum Signal, Should Have a High Bandwidth to Track the Jitter
- Stratix Devices Are Able to Lock Onto a Spread Spectrum Input Signal
  - The Incoming Spread Spectrum Signal Looks Like Jitter
- Increased Period Jitter
- Lower Average Clock Speed

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Programmable Bandwidth

- Allows Customization of PLL Bandwidth to Suit End Application
  - Lock-Time Tradeoff with Jitter Filtration
- Bandwidth Settings
  - Automatically Selected
    - To Preset Values
      - Low, Medium & High
    - To Customized Values Specified by User
- Bandwidth Ranges from 200 KHz to 1.5 MHz

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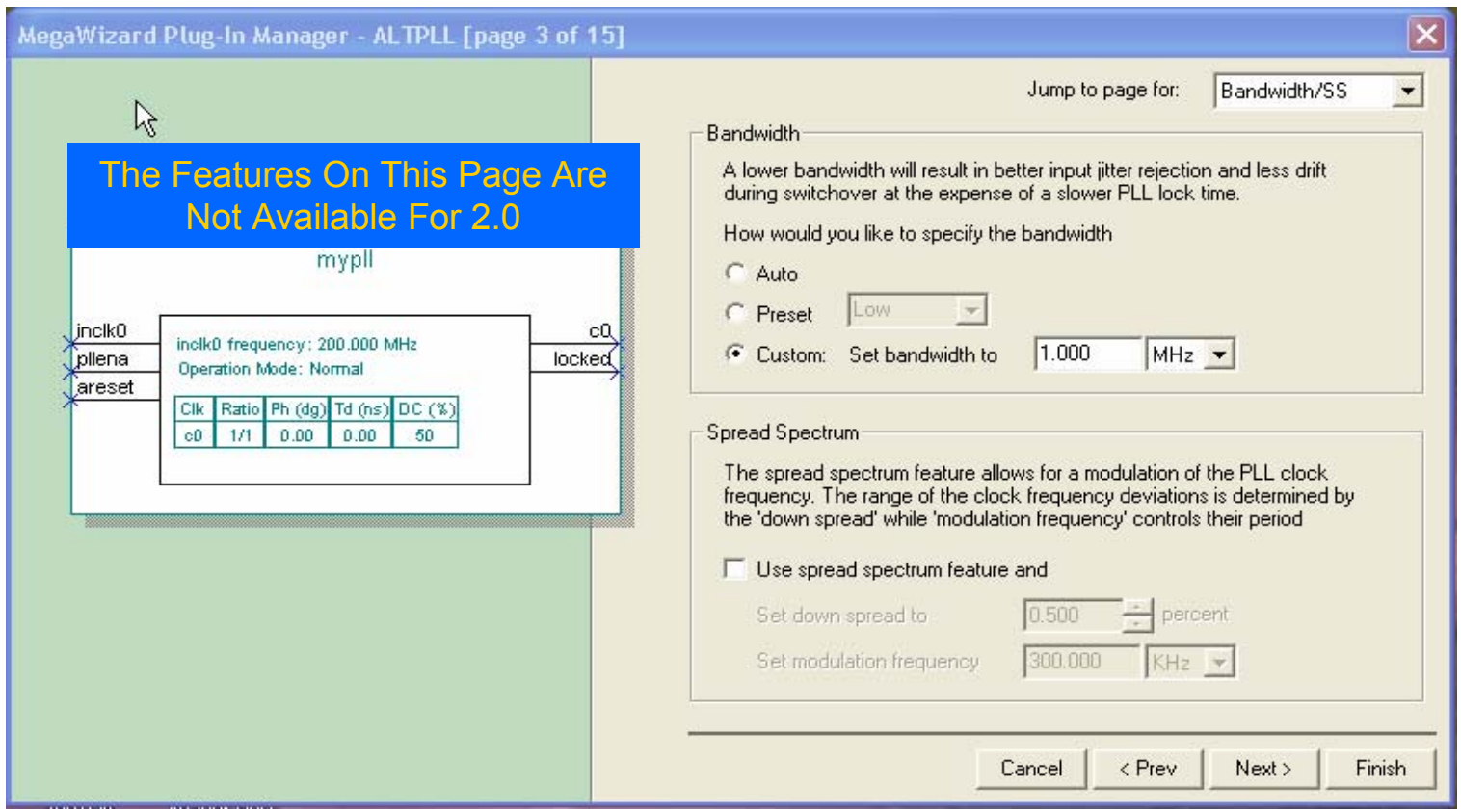
Quartus II Software Settings

- Set Bandwidth Via MegaWizard®



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Quartus II Software Settings

- Set Bandwidth Type Using MegaWizard
  - **Auto**: Let Quartus® II Choose Bandwidth Setting
  - **Preset**
    - **Low**: Low Bandwidth
    - **Medium**: Medium Bandwidth
    - **High**: High Bandwidth
  - **Custom**: Enter Desired Bandwidth Value
    - Quartus II Will Automatically Adjust Other Bandwidth Settings in Order to Achieve This Value

Enhanced & Fast PLL Specifications

Parameter	Enhanced PLL	Fast PLL
Input Frequency	3 to 462 MHz	33 to 644.5 MHz
Output Frequency	1.2 to 462 MHz	9.4 to 644.5 MHz
Lock Time	1 ms	100 µs
Dynamic Lock Time	100 µs	-
Maximum Input Jitter	±150 ps (p-p)	±100 ps (p-p)
Maximum Output Jitter	±100 ps (p-p)	±100 ps (p-p)
VCO Operating Range	300 to 800 MHz	300 to 840 MHz

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