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DDR SDRAM Interface in Stratix/GX and Cyclone

MJL Technology. LD Team 1

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Agenda

- DDR SDRAM Memory Overview
- Stratix & Stratix GX DDR SDRAM Support
- Cyclone Support
- IP Support
- FAQ
- References

DDR SDRAM Memory Overview

- Data is sent at double data rate
- Commands and addresses are output at single data rate
- A strobe is normally sent along with the data
  - Strobe is center-aligned when writing to the memory
  - Strobe is edge-aligned when reading from the memory

DDR vs SDR Functionality

PARAMETER	SDR	DDR	NOTES
DQM	Yes	No	Used for write data mask and read OE
DM (Data Mask)	No	Yes	Replaces DQM, used to mask write data only
DQS (Data Strobe)	No	Yes	New, used to capture data
DK# (System Clock)	No	Yes	New, DDR utilizes differential clocks
Vref	No	Yes	Reference Voltage For Differential inputs (1/2 VDD)
VDD and VDDQ	3.3 V	2.5V	Reduced Supply and power for DDR
Signal Interface	LVTTL	SSTL_2	DDR utilizes differential I/O
Output Drive	Fixed	Variable	X16 DDR devices offer a reduced drive option
Data Rate	1x Clock	2x Clock	Data transfer is twice the clock rate for DDR
Architecture	Synchronous	Source-Synchronous	DDR utilizes a bidirectional data strobe

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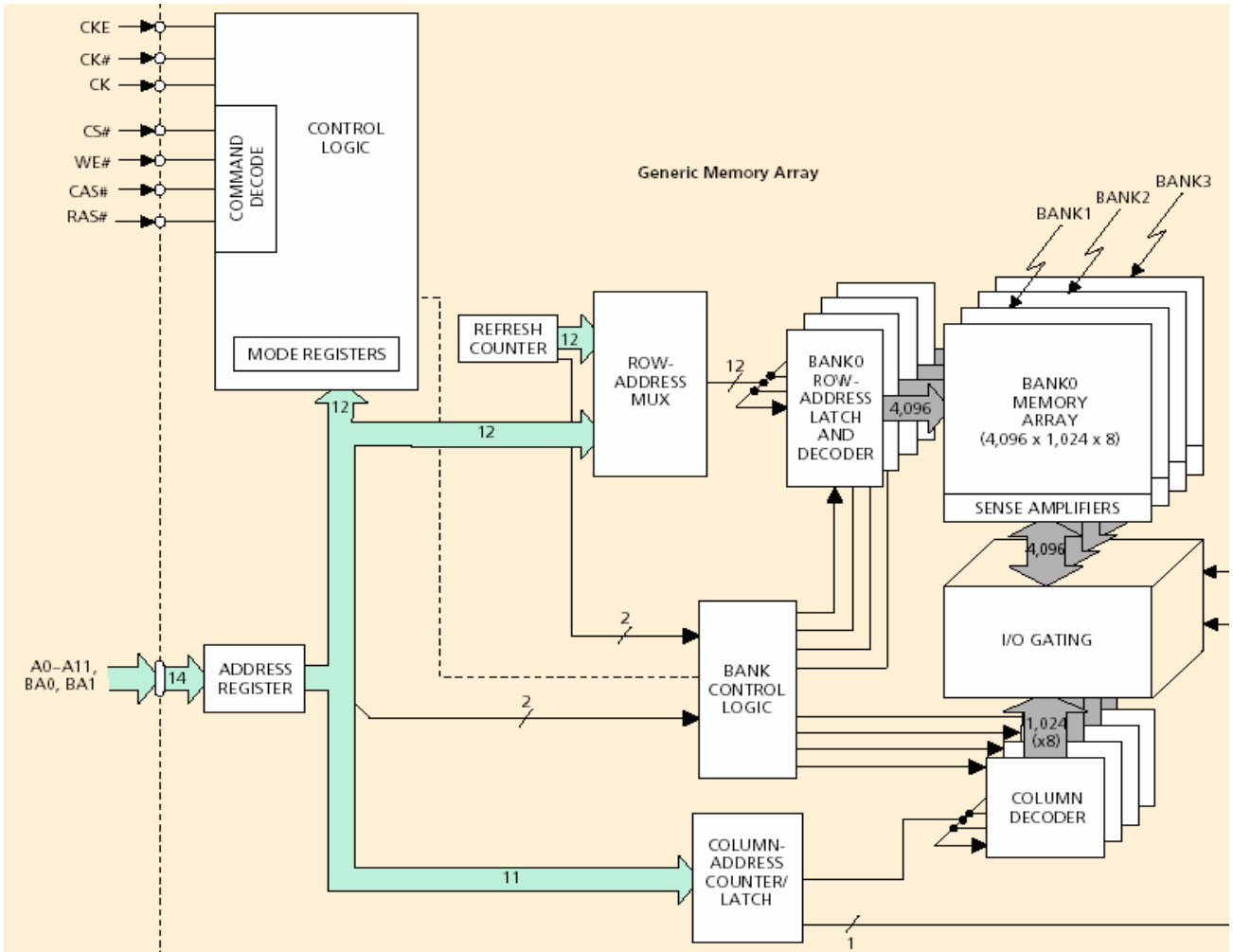
Generic Memory Array



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Stratix and Stratix GX Support

- Device Support Overview
- Sampling Window Calculation
- Software Support and Implementation
- Timing Analysis in Quartus II
- Round Trip Delay
- Characterization Data Summary
- Board Guidelines
- Non-dedicated DQS Circuitry Support

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Dedicated DQS Support Summary

Device	Package	Number of X8 DQ/DQS groups	Number of X16 DQ/DQS groups	Number of X32 DQ/DQS groups
EP1S10	672-pin BGA 672-pin FBGA	12	0	0
	484-pin FBGA 780-pin FBGA	16	0	4
EP1S20	484-pin FBGA	18	7	4
	672-pin BGA 672-pin FBGA	16	7	4
	780-pin FBGA	20	7	4
EP1S25	672-pin BGA 672-pin FBGA	16	8	4
	780-pin FBGA 1020-pin FBGA	20	8	4
EP1S30/ EP1S40 EP1S60/ EP1S80	All packages	20	8	4

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Device Support Overview

- Dedicated DQS phase shift circuitry applies to top and bottom I/Os only
  - There are 2 DLLs per device
  - Up to 20 DQ/DQS groups in x8 mode
    - 8 DQ/DQS group in x16 mode, 4 in x32 mode
    - Up to 5 DQ/DQS x8 group per I/O bank
    - x8: 1 DQS 8 DQ pins, x16: 1DQS 16 DQ pins, x32: 1 DQS 32 DQ pins
    - Not the same definition as memory vendor x16 and x32 mode!

Speed Grade	C5	C6	C7
SDRAM Support (MHz)	**200**	**167**	**134**

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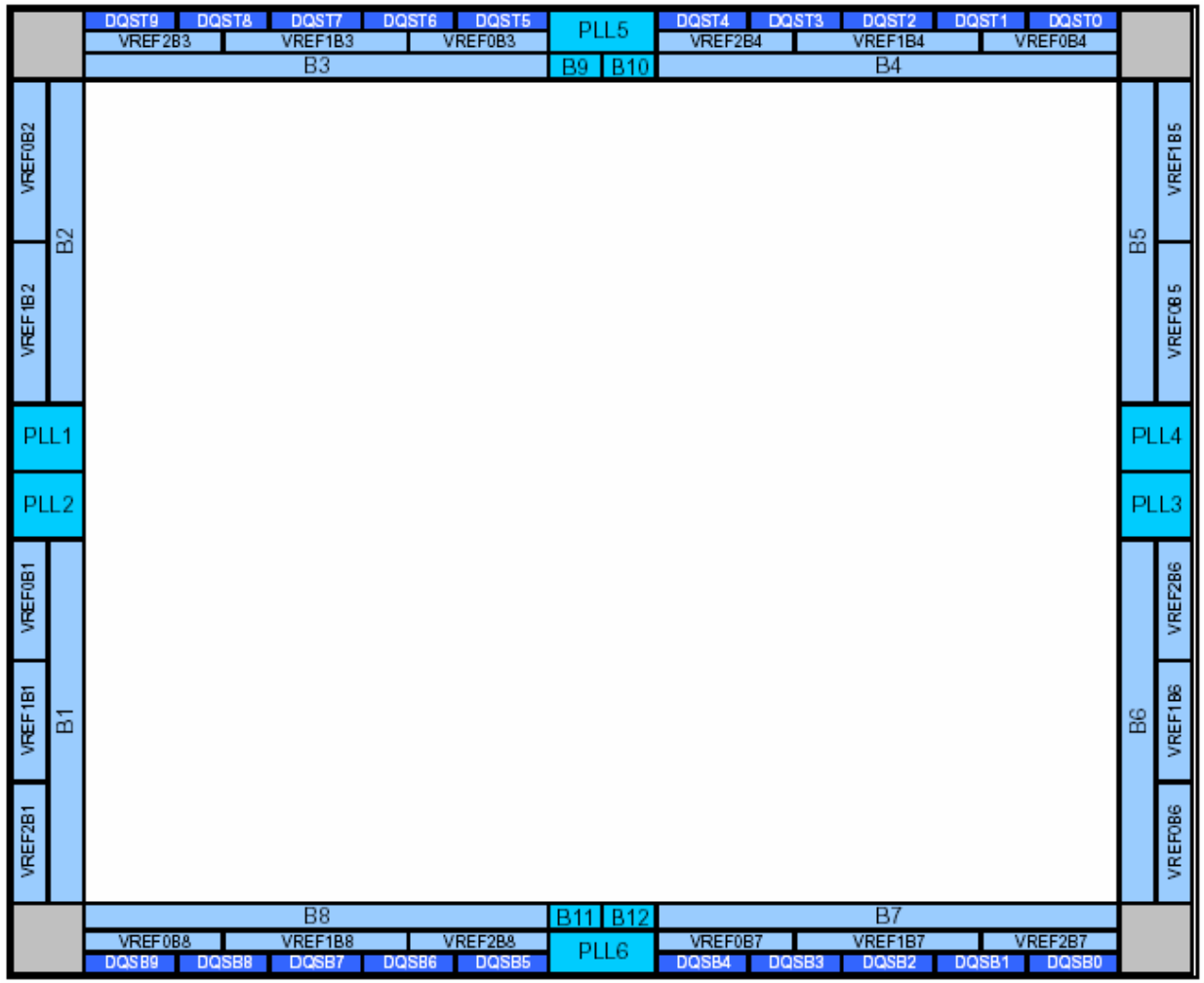
Device Support Overview (cont'd)

- DDR SDRAM support on side I/Os
  - Need a different scheme that does not use the DQS Phase Shift Circuitry
  - Crucial when top/bottom I/Os are used for PCI
  - Or if many DDR devices are used instead of DIMM modules
  - Limited by either the side I/Os clock Fmax (150 MHz on C5 Flip-Chip devices) or by the scheme's robustness itself

PLL and Bank Diagram



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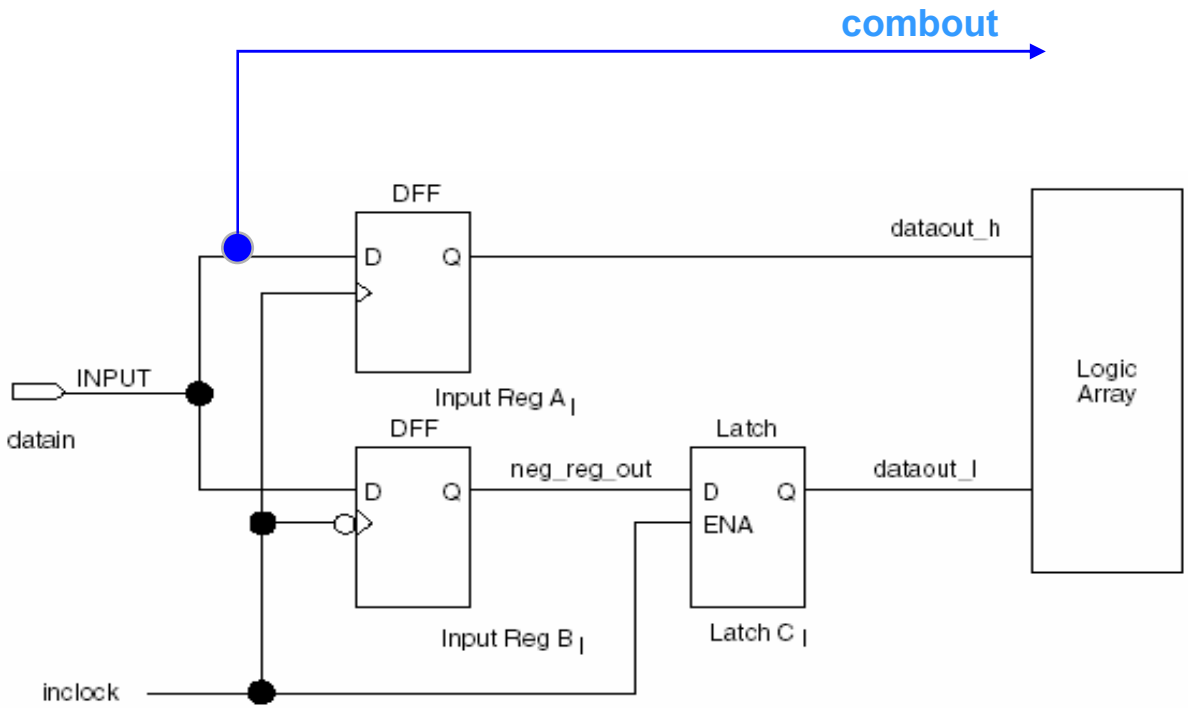
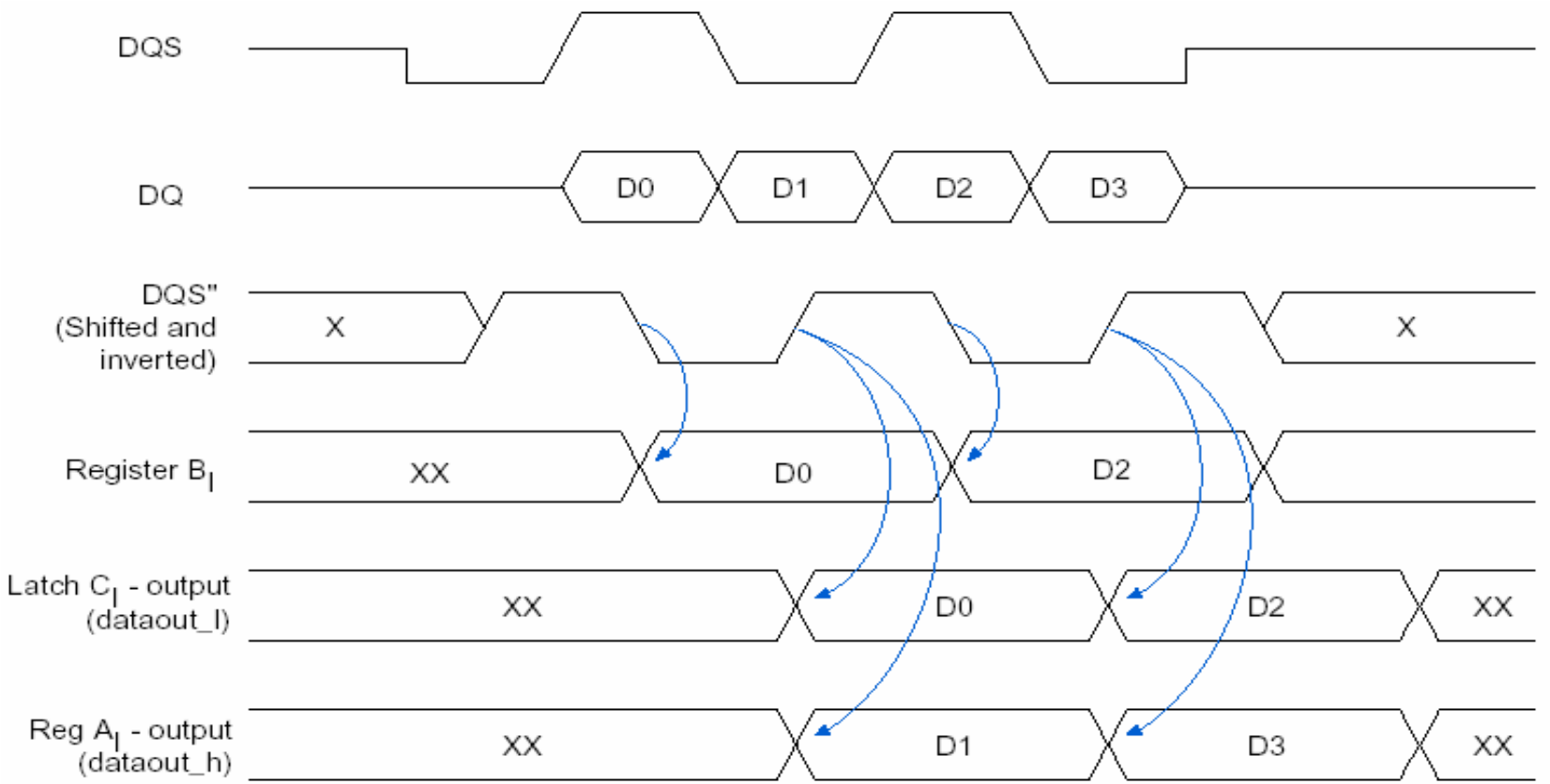
Input DDR I/O Path Configuration



DDR Memory Interface Read Operation



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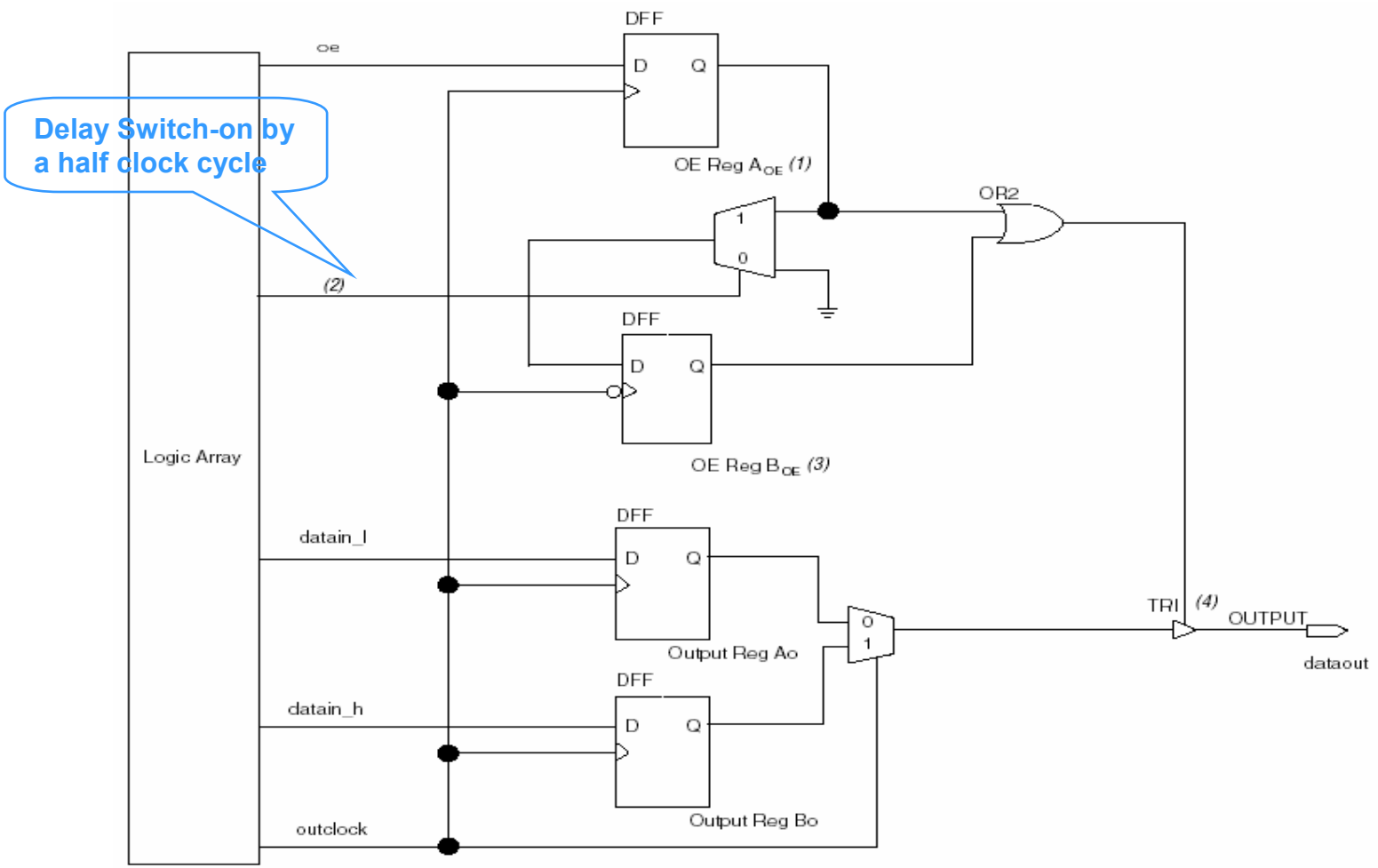
Output DDR I/O Path Configuration



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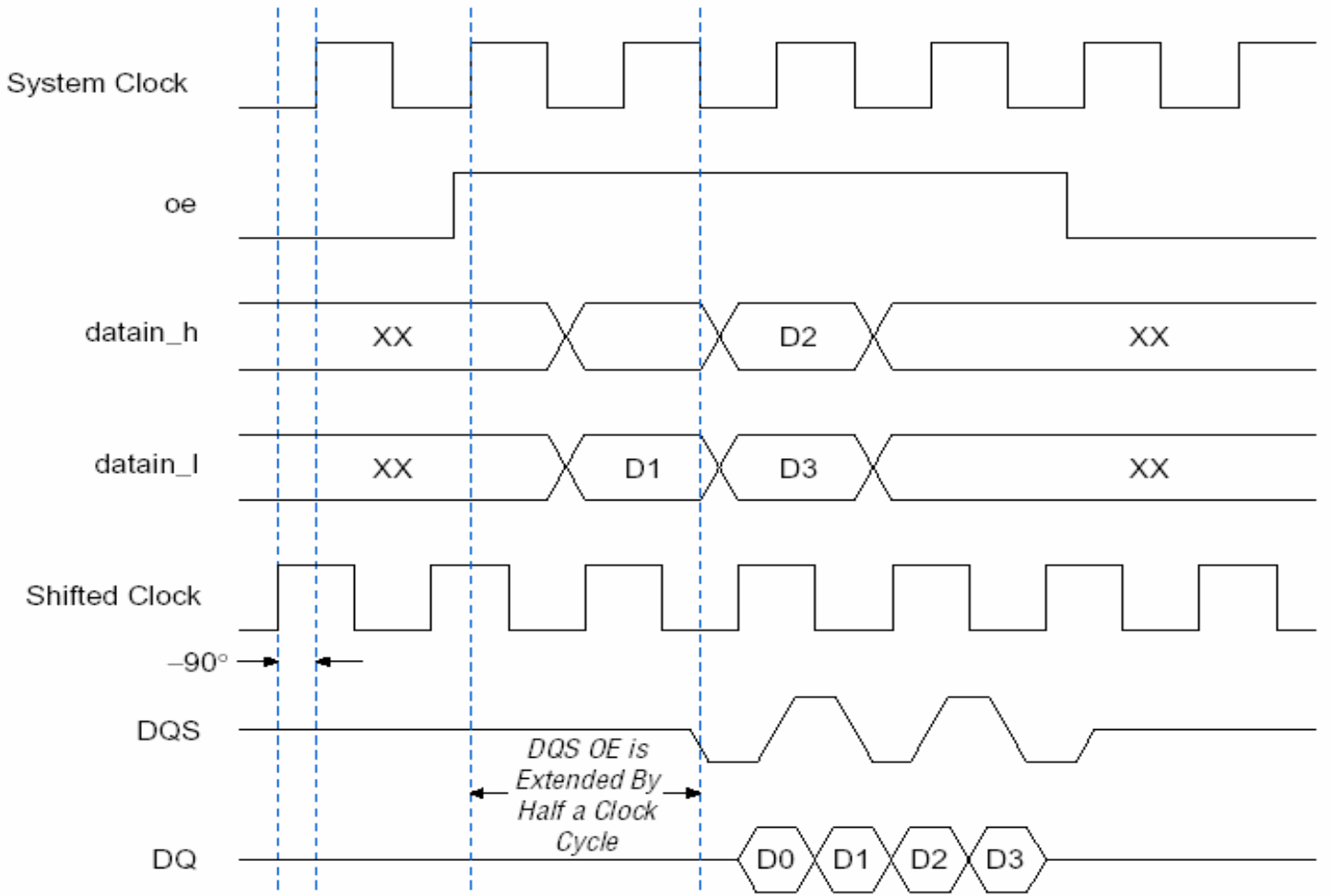
DDR Memory Interface Write Operation



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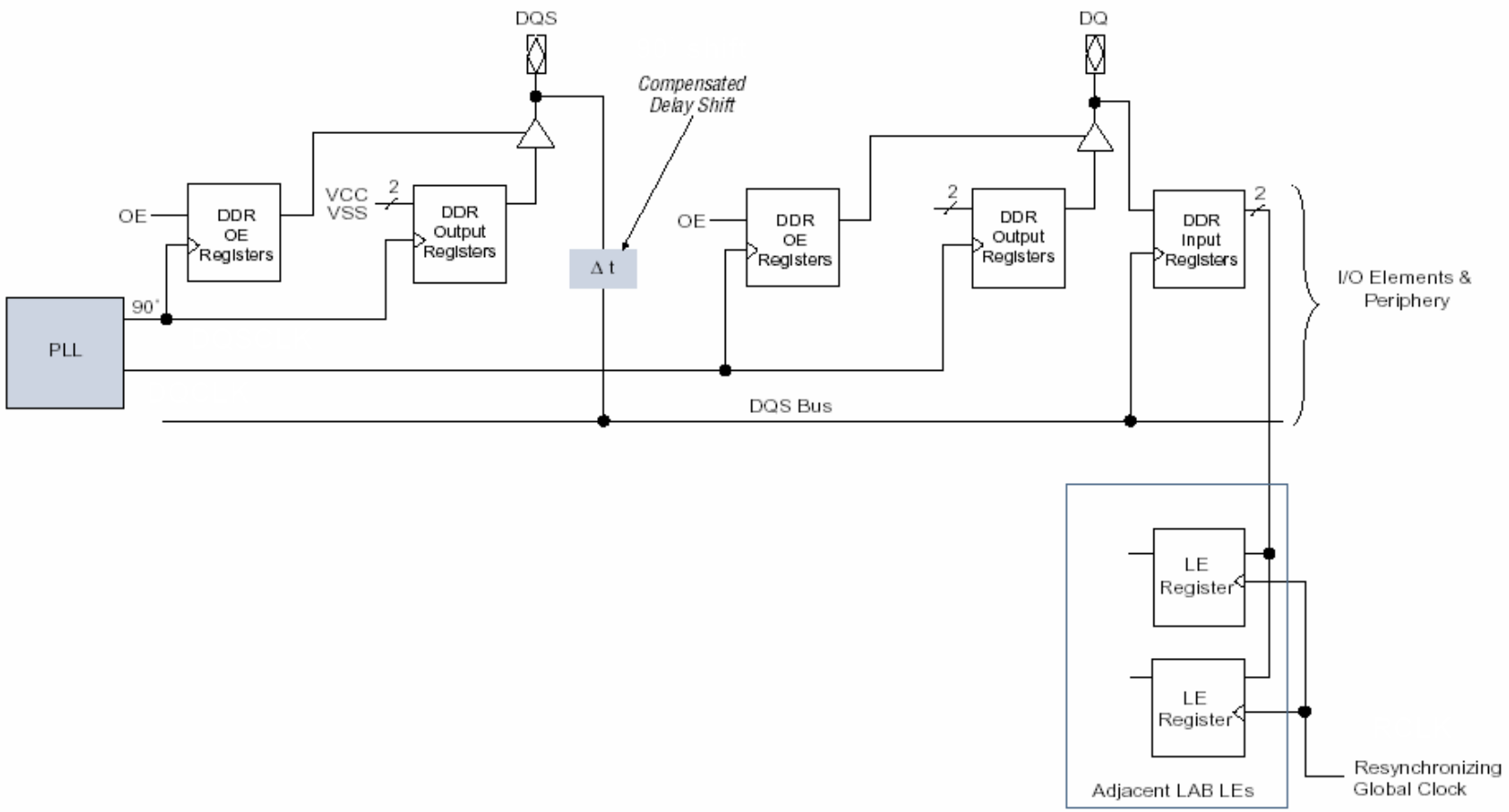
Bidirectional DDR I/O Path



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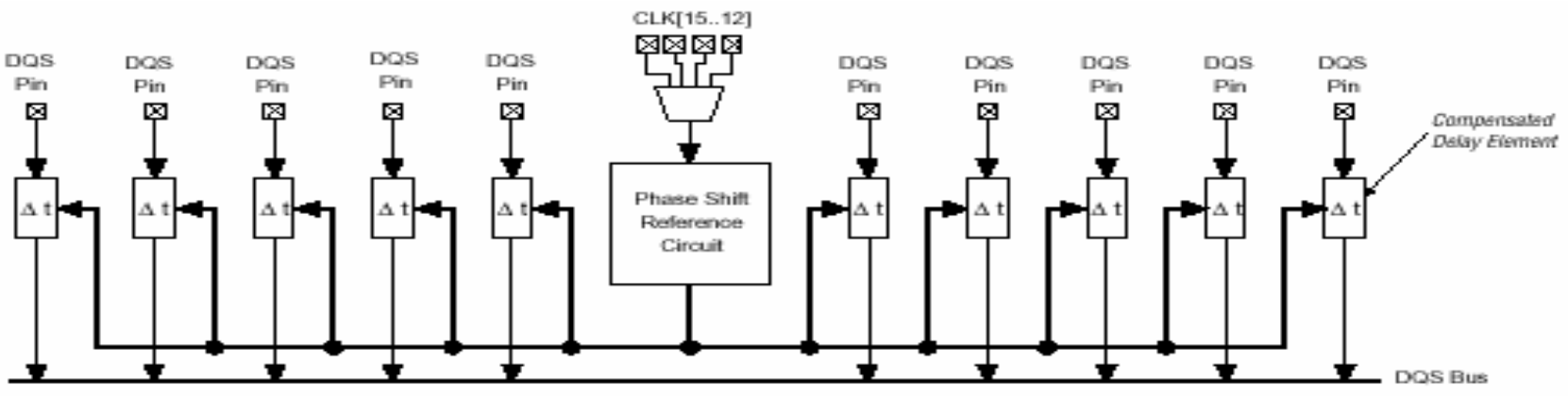
DQS Phase Shift Circuitry

- Self-Compensated Delay Chain (DLL) Generates Shift on Data Read
  - Only 2 available per device (one on top, one on bottom)
  - 90 Degrees for DDR SDRAM, 72 Degrees for FCRAM
- Drive Associated Data (DQ) Pins
  - Uses Balanced, Local Clock Network
  - DQS bus only goes to the IOE clock ports
- Needs to have 256 clock cycles to initialize



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Software implementation

Signals	Megafunction	Comments
DQS	altdqs	New in Quartus II 3.0 (only for Stratix and StratixGX)
DQ	altddio_bidir	No change in Quartus II 3.0
DM*	altddio_out	No change in Quartus II 3.0

*DM pins are only used in DDR SDRAM and RLDRAM (not in DDR FCRAM)

Available under I/O
in the Megawizard Plug-In Manager

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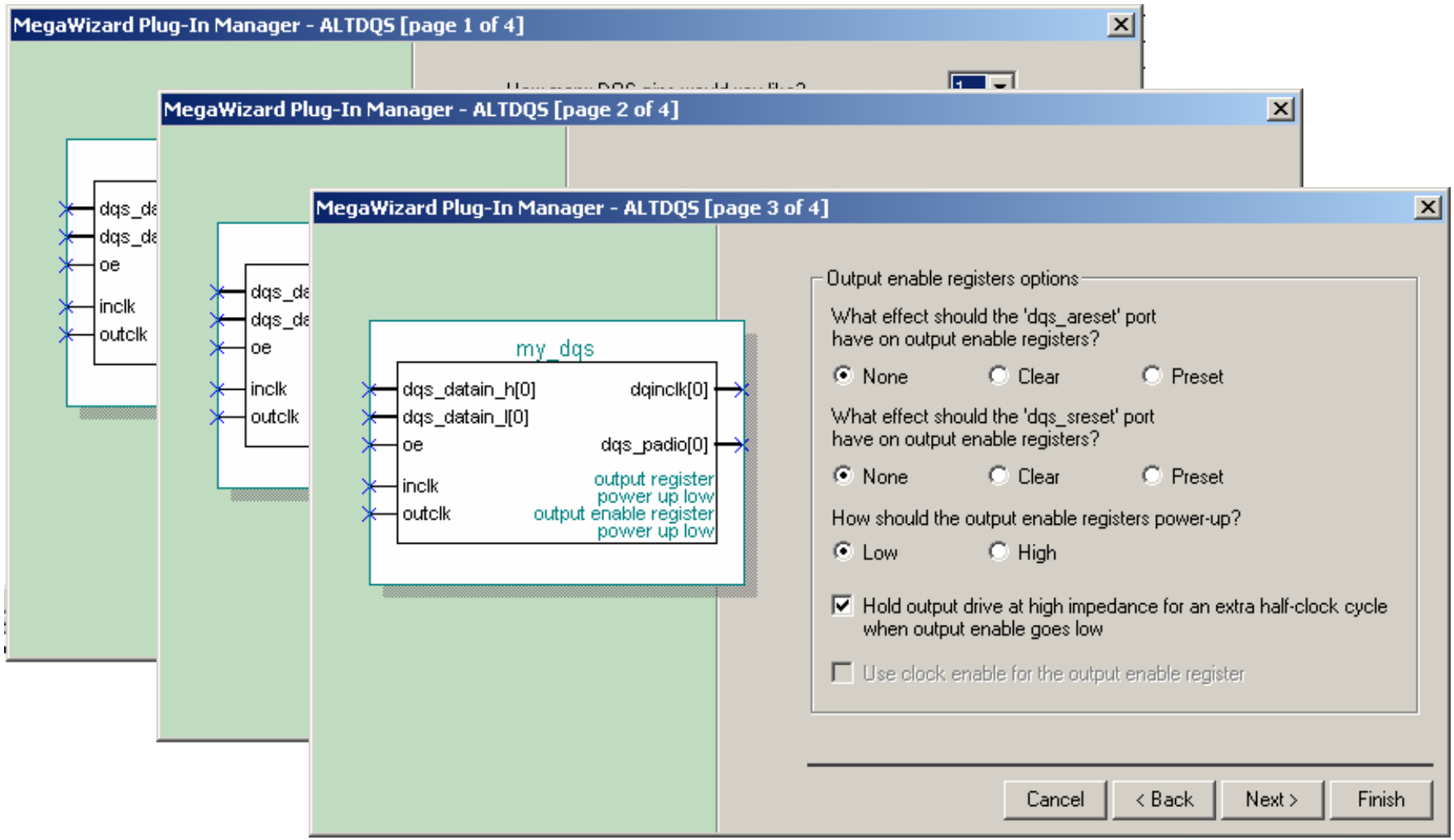
MegaWizard for DQS Pins



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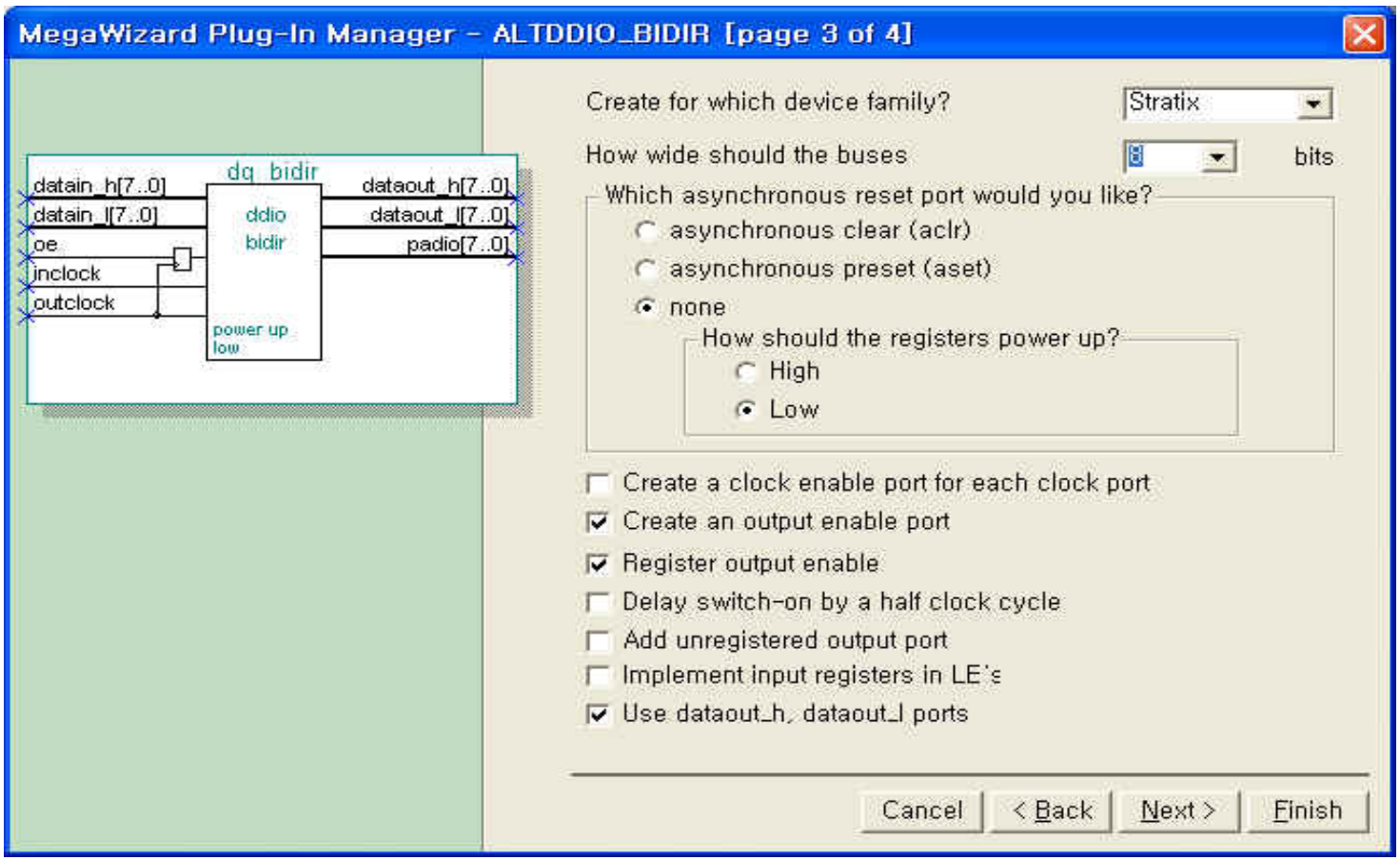
MegaWizard for DQ Pins



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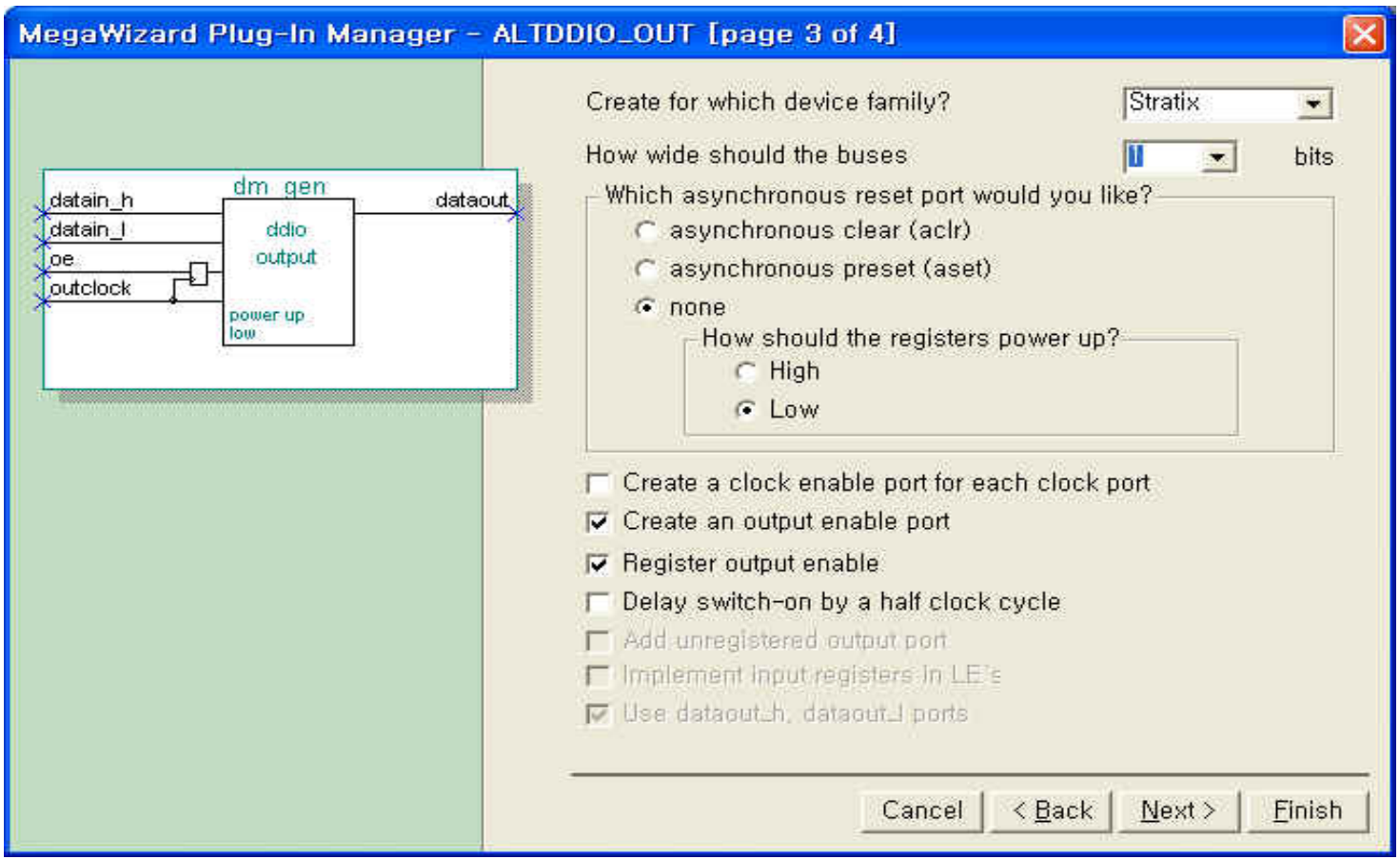
MegaWizard for DM Pins



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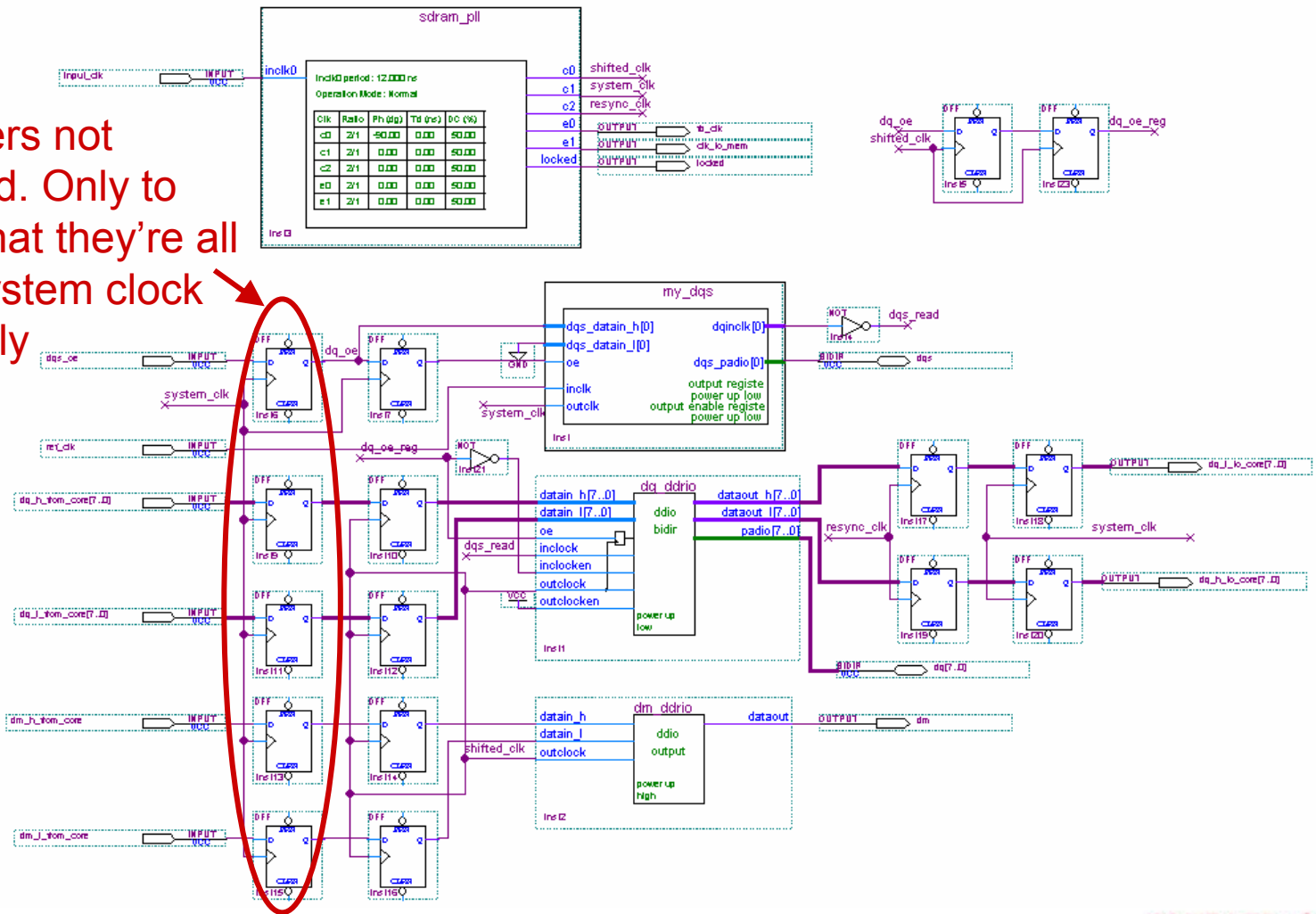
DDR SDRAM I/O Interface Example

Registers not required. Only to show that they're all from system clock originally



Design available on the web!

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Design Example Details

- Left side of the megafunctions block serves as the write side; right side as the read side
- DQS “write” signal is generated with the system clock
- DQ and DM “write” signals are generated using the -90° shifted clock
  - Double registers to switch clock domain from system clock to -90° shifted clock domain
- DQ “read” signals are captured in the LE with a resync_clock before going to the system clock domain
  - Phase for resync_clock may vary
  - resync_clock is optional (dependent on your RTD)

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Design Example Features

- DQS Frequency is 2X input clock
  - Details how an extra input clock is needed
- DQS signal is inverted before going to the DQ IOE inclock port
  - Needed for the interface or else last data is not captured
- Placeholder for resync clock
  - If you need one… (optional)
- datain_h port of the altdqs not connected to VCC
  - Provides better write preamble time
  - Recommended but not a must

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Timing Analysis in Quartus II

- Read Side
  - Done with respect to the non-shifted DQS signal (as it is at the FPGA pin)
    - DQS gets extra delay due to 90° shifting, while DQ goes straight to the IOE registers
  - Expect negative setup and positive hold time
- Write Side
  - Done with respect to input clock to the PLL
    - PLL is in normal mode
  - Possibility of negative tco on the DQ pins
    - DQ pins are clocked 90° ahead

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Logic options to the DQ/DQS pins

- DQS Frequency – the frequency of your DDR SDRAM device
- DQS Phase Shift – either 72 or 90 degrees
- DQS Input reference clock – the input clock to be used for your DQS Phase Shift circuitry
- Make sure to add an inverter between the combout port of the dqs_ddrio module and the inclock port of the dq_ddrio module
- VREF Constraints - Quartus II only allows a maximum of 20 outputs or bidirectional pins per dedicated VREF pin.
- On-Chip Termination

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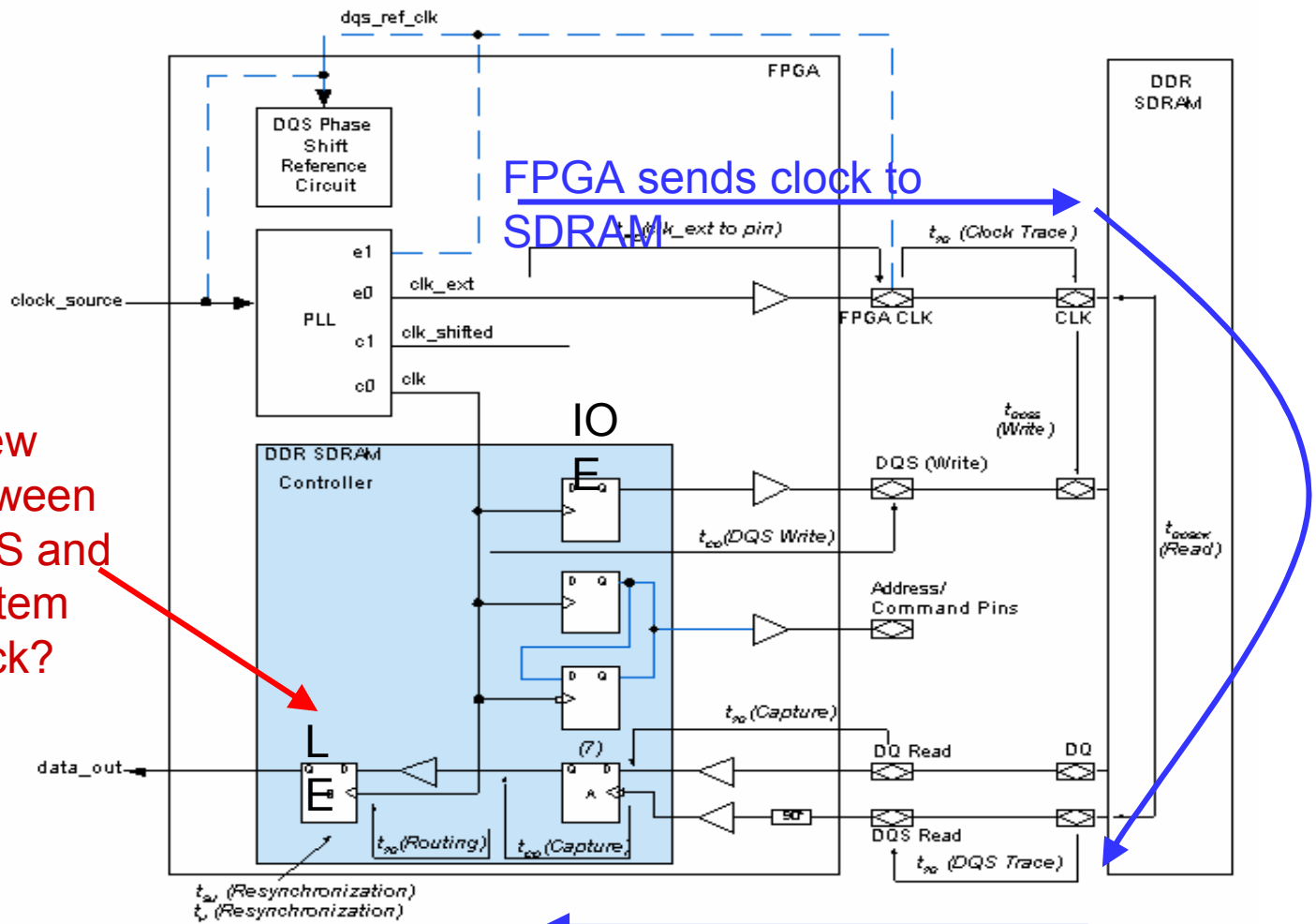
Round Trip Delay – Why?

- Skew between DQS and System clock unknown
  - Skew between DQS and CK: tDQSCK
  - DQS position may vary from burst to burst

- Need to calculate min and max timing round trip delay to get the safe resynchronization window from IOE to LE

Round Trip Delay - Illustration



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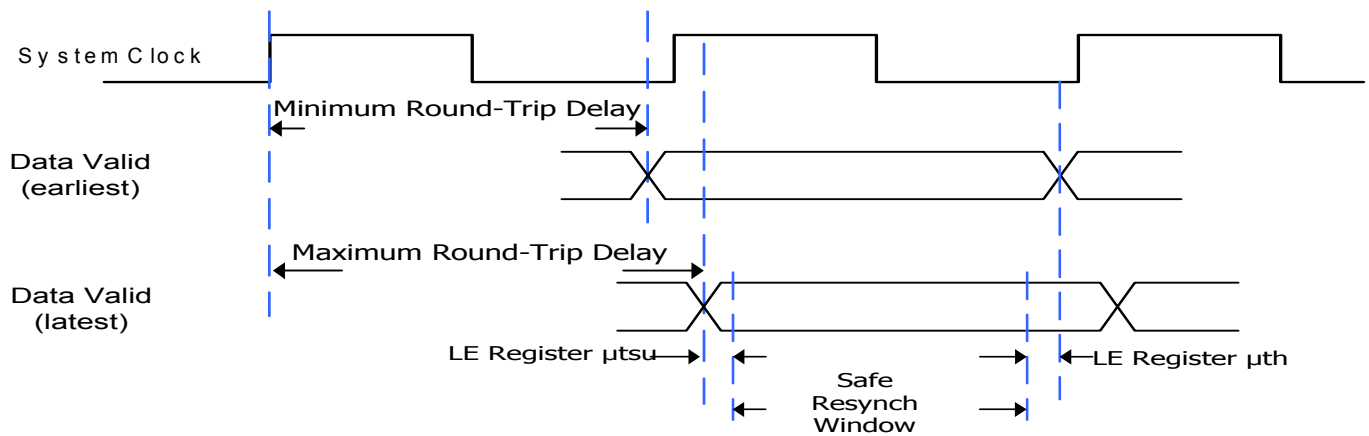
Round Trip Delay - Effects

- First calculate min and max delay
- Then find out the data valid overlap (resynch window) and make sure it's big enough for resynchronization
- If there's a clock edge in the resynch window, use it.
- Else, use an extra PLL output (phase shifted)



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Round Trip Delay Calculator

- In the form of a spreadsheet
  - Serves as a guideline only, not a hard rule
- Preliminary release
  - Have not been correlated with characterization data
- You need to know:
  - The board traces length and skew
  - Quartus reported tco for DQS (TCO TAN)
  - Quartus reported IOE to LE delay (DQS TAN)
- Also shows where the signals are with respect with the system clock
- Once finalized, the calculator may be incorporated inside the Quartus II software

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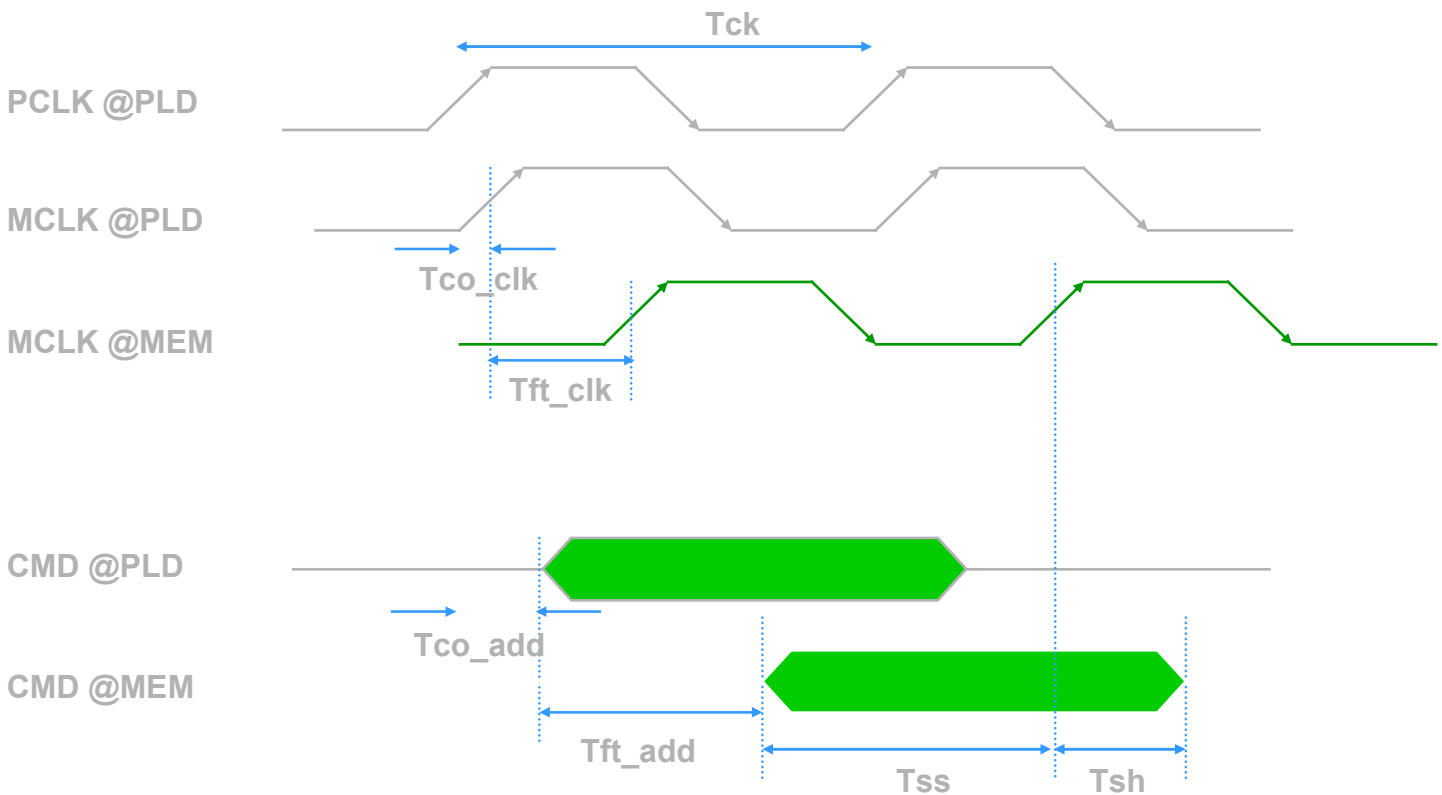
Address Timing Margin



Tsh = (Tco_add + Tft_add) - (Tco_clk + Tft_clk)

Tss = Tck – Tsh

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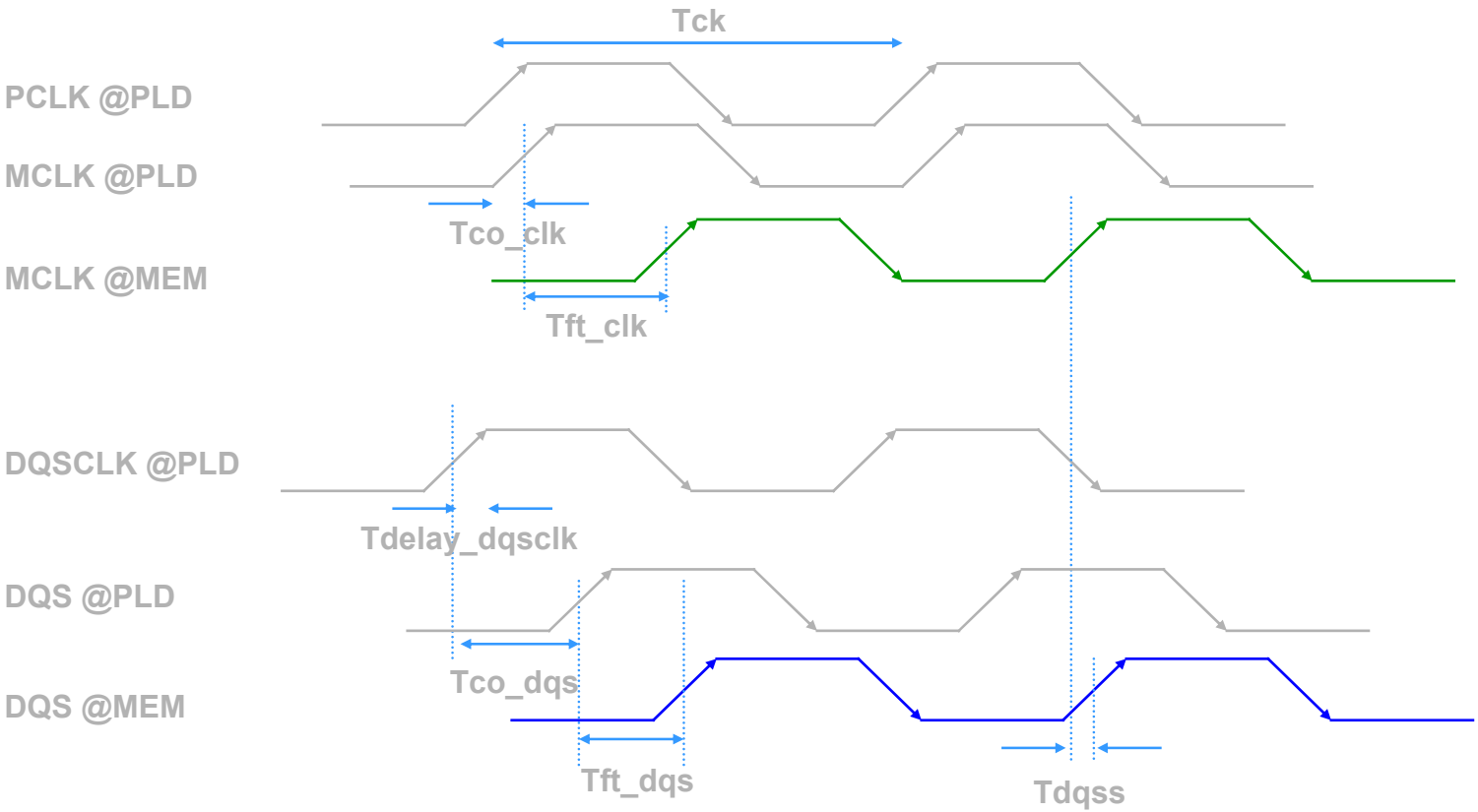
Write Timing Margin



Tdqss = (Tco_clk + Tft_clk) - (Tco_dqs + Tft_dqs + Tdelay_dqsclk)

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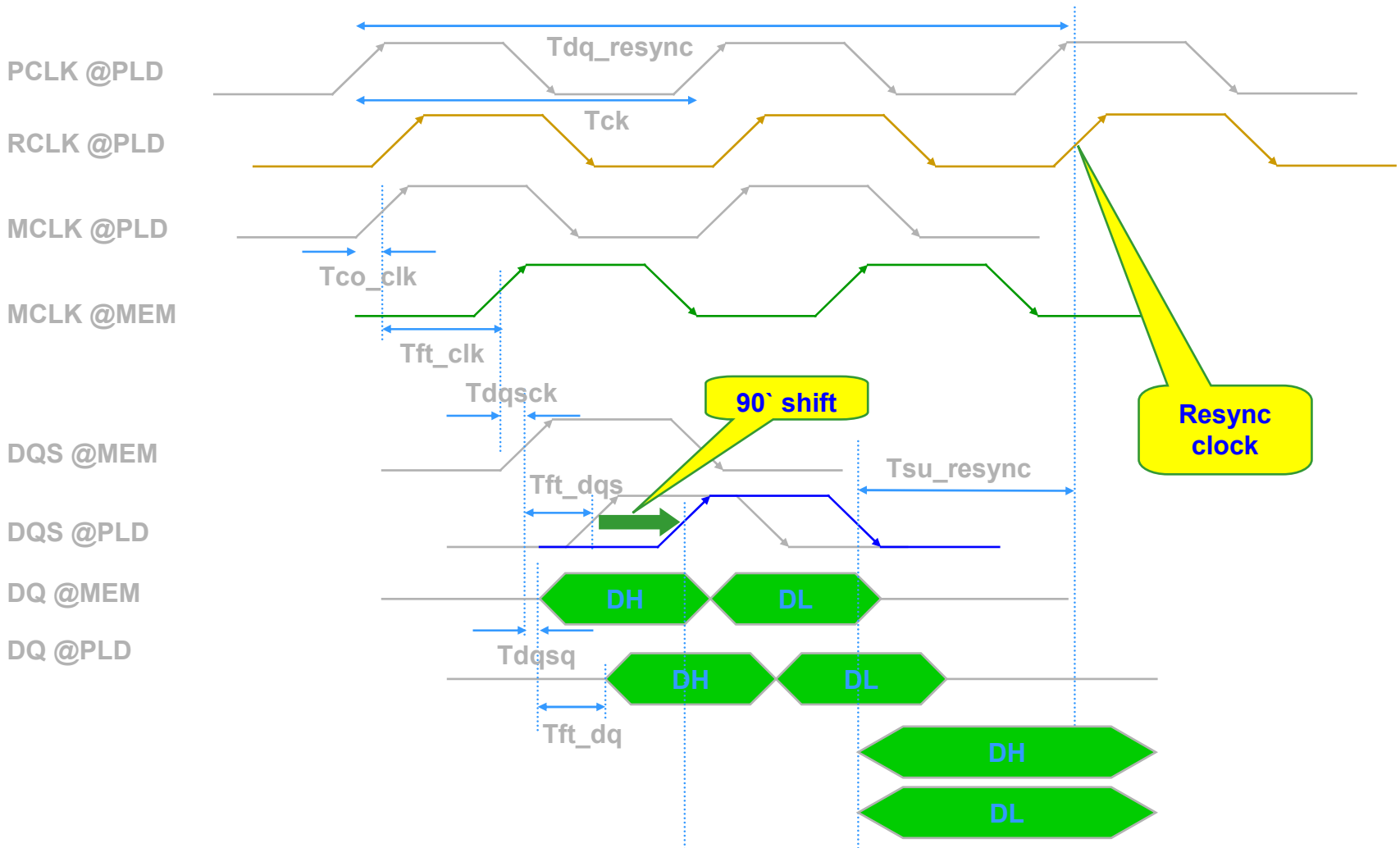
Read Timing Margin



Tdq_resync = (Tco_clk + Tft_clk) + Tft_dqs + 90'shift + Tck/2 +Tsu_resync

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Characterization Data Summary

- Characterization is finished
  - Altera IP core used as the controller
- Shows Stratix C5 devices can interface with 200 MHz DDR SDRAM DIMM
  - Only Micron DIMM passes all patterns at worst conditions (has strongest drive)
  - On-Chip Termination is not used
  - Current setting of Stratix device is set to Min
  - Still investigating worst case pattern with Infineon and Samsung 200 MHz operation
- Reports are available in Molson

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Board Guidelines

- Micron website as a source
- Details are in Stratix DDR SDRAM 166 MHz Characterization Report
- More guidelines can be found in DDR Memory Controller User Guide Appendix C
- Some simple rules
  - Matched length between Address and Control signals; DQ, DM and DQS signals; CK and CK# signals
  - DQ, DQS, CLK routed at least 30 mil away from other signals (to reduce cross talk)
  - DQ, DQS, and DM should not share R-pack series resistors (to reduce cross talk between signals)
  - One 0.1uF Cap Per Two Termination Resistors
    - Each Cap Two Vias
  - Use precision resistors (within 1-2 %)

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VREF and VTT Guidelines

- VTT
  - Use An Integrated VTT Regulator Specially Designed for DDR VTT
- VREF
  - Can use Voltage Divider
  - Routed at least 20mm (~800 mil) away from other signals
  - Routed over a reference plane
  - Shield Vref with Vss on one side, and with VDDQ on the other side to maintain symmetry in the presence of noise

Non-dedicated DQS Circuitry Support

- Static PLL
  - Use an extra PLL output that mimics DQS coming into the FPGA
- Dynamic PLL
  - Use calibration sequence to pick a phase to capture data
- Matching Trace Length
  - DQS Phase Shift is taken care of on the board trace

Non-Dedicated DQS support - Static PLL scheme

- Advantages:
  - Easy to implement
  - No extra logic needed
  - Fmax limited by PVT variations
- Disadvantage:
  - May miss data sampling window if PVT variations are too large
- Status
  - Paper Calculation ready (133 MHz Fmax in C5)
  - Need to do H/W proof-of-concept

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Non-Dedicated DQS support - Dynamic PLL scheme

- Advantages:
  - Can achieve better Fmax
  - Much less dependency on speed grade
- Disadvantages:
  - Additional 'refresh-like' down time impacts efficiency
  - LE count increased for the calibration circuitry
- Status
  - Paper Calculation ready (150 MHz Fmax buffer limit)
  - IP is underway
  - Option to train on DQS removes main disadvantages

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Non-Dedicated DQS support - Matching Trace Length scheme

- Advantage:
  - DQS is still used, so DQ-DQS relationship is still maintained
- Disadvantages:
  - Cannot simply reconfigure the FPGA if you need to run at a different speed
  - Need to make sure the board process variations are not too large
  - Need to ensure DQ and DQS skew inside FPGA is not too large
- Status:
  - Still under study, no paper calculation yet

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Cyclone Support

- Device Support Overview
- Characterization update

Device Support Summary

Device	Package	Number of DQ/DQS groups
EP1C3	100-pin TQFP	3
	144-pin TQFP	4
EP1C4	324-pin FineLine BGA	8
	400-pin FineLine BGA	8
EP1C6	144-pin TQFP	4
	240-pin PQFP	4
	256-pin FineLine BGA	4
EP1C12	240-pin PQFP	4
	256-pin FineLine BGA	4
	324-pin FineLine BGA	8
EP1C20	324-pin FineLine BGA	8
	400-pin FineLine BGA	8

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Device Support Overview

- Up to 8 DQS/DQ groups in x8 mode (2 per bank)
  - X8 mode means 1 DQS per 8 DQ pins
  - X16 and X32 are currently not supported
  - Configuration pins uses 2.5V when Bank 1 and/or Bank 3 are used
- DQS Phase Shift achieved using a programmable delay chain
  - Each DQS can work at different frequency
- DDR I/O interface implemented in the LEs
- Target F_{max} is 133 MHz

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Device Support Overview (cont'd)

- DQS signals can be routed into the FPGA
  - Each DQS signal uses a global clock net line
  - Limited to 48-bit interface due to lack of global clock net resources
    - 6 global clock nets are used for DQS
    - 2 global clock nets are used for the system clock and -90° shifted clock
    - All other logic in the design must use either the system clock or the -90°shifted clock
  - 64-bit support under study
    - Mention any opportunity to the factory

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Cyclone vs. Stratix DDR SDRAM Interface

- DQS signal can go to the core and not just IOEs
- Used up a global clock net
- Up to 48-bit interface only
- DDR I/Os are implemented in the LEs
- DQS Phase shift uses programmable delay chains
- DQS Phase shift not limited to top/bottom banks
- Each DQS can work at different frequencies
- Target is 133 MHz instead of 200 MHz
- Each bank has a maximum of 2 DQ/DQS groups
- Only x8 is supported, no x16 or x32 support currently (x8, x16, x32: 1DQS per 8, 16, or 32 DQ pins respectively)

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Characterization update

- To be finished by WW32
- Designs to be characterized:
  - 16 bit interface at 133 MHz
  - 32 bit interface at 133 MHz
  - 48 bit interface at 133 MHz
  - Multiple DIMMs

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IP Support

- DDR SDRAM Controller Megacore
  - Version 1.2.0 available on the website
    - 200 MHz support with CAS latency=3
    - Cyclone support
  - Version 2.0.0 in Q4 2003
    - To include Stratix non-DQS mode implementations
- RLDRAM II Controller Megacore
  - In Concept Phase
- Cores from AMPP Partners
  - DDR SDRAM cores from DCM Technologies and Northwest Logic

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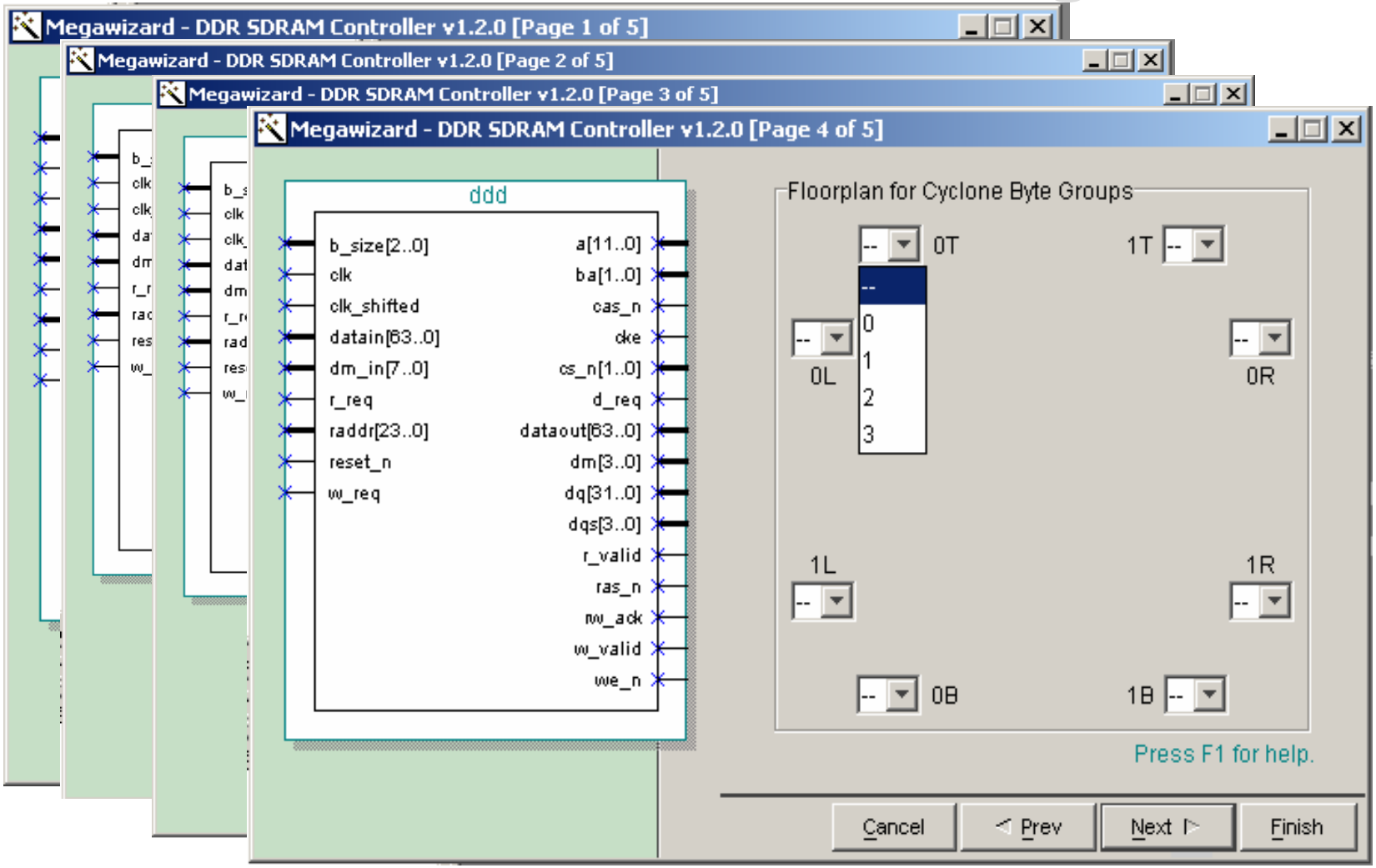
Advantages of using the MegaCore

- Easily implemented
  - 5 MegaWizard pages
- Design constraints are provided
  - Encourage customer to use the MegaWizard, even if it is only for the constraints
- The only way to get LE placement constraints for critical paths in Cyclone

DDR SDRAM Controller MegaWizard



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FAQs

- Error on DQ pins being too close to VREF
  - Check the VREF/pad placement guidelines in AN201
  - If in compliance, use the “Output Enable Group” option
- When DQS frequency != input clock frequency
  - Remember that DQS inclock must come from an input pin
- Can I just connect dqs_datain_h of the altdqs megafunction to VCC?
  - Yes. Having the unregistered OE signal connected to dqs_datain_h port helps with the write preamble time (timing simulation only, not in silicon)

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FAQs (cont'd)

- Does simulation show the DQS phase shift?
  - Yes, both functional and timing simulation show the 72° or 90° shift
- What if I have a 9:1 (DQ:DQS) relationship?
  - Quartus will create a x16 mode, where the seven extra DQ pins are not connected to the DQS bus (can be used as regular I/O)
- Not getting the last data (simulation and silicon)
  - Remember to invert the DQS signal coming in

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FAQs (cont'd)

- Can I use OCT?
  - Maybe. Depending on the interface, you may violate the current limit set for any ten adjacent pins in Stratix
  - If you are interfacing with a 200 MHz DDR SDRAM, Altera recommends setting the SSTL-2 current setting to MIN and OCT cannot be used with this current setting
- Does DQS have to be a bidirectional pin?
  - Yes, if for some reason you only need it for reading (in case of RLDRAM), you can tie the OE to GND. Do not tie outclock to GND in Quartus II 3.0!

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References

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References (www.altera.com)

- Quartus II Design Example: DDR SDRAM I/O Interface
  - http://www.altera.com/support/examples/quartus/q-ddr.html
- DDR SDRAM Controller
  - http://www.altera.com/products/ip/iup/memory/m-dcm-ddr_sdram.html
- Stratix Hand Book
  - http://www.altera.com/literature/lit-stx.html
- Double Data Rate I/O Signaling in Stratix & Stratix GX Devices(Altera DataSheet)
  - AN212.pdf / AN201.pdf / Startix_handbook.pdf
- External Memory Device Interfaces in Stratix Devices
  - http://www.altera.com/products/devices/stratix/features/stx-ext_mem_int.html

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