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StratixGX Design Guideline

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The Low-Risk Path to 3.125-Gbps Transceiver Applications

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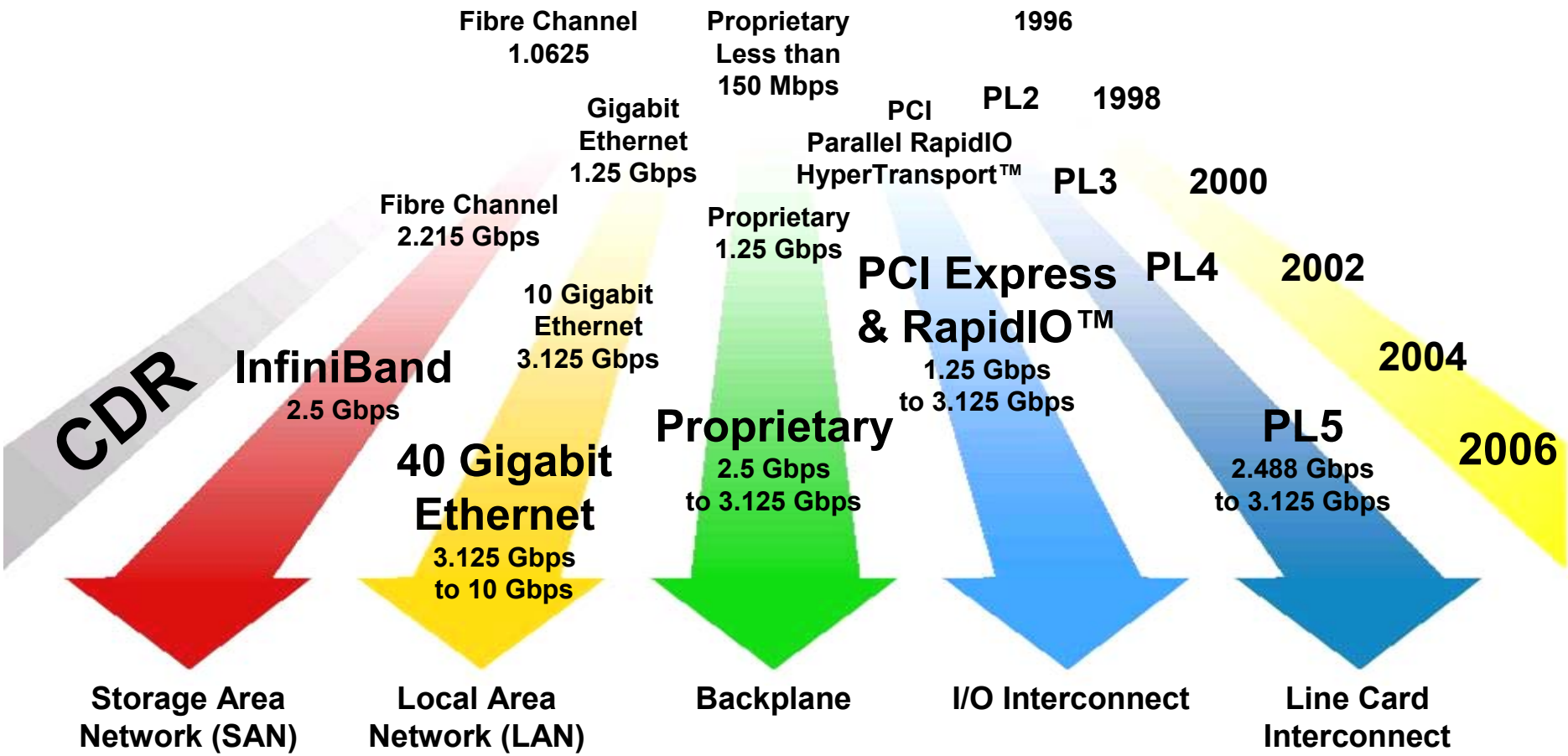
Bandwidth Demand



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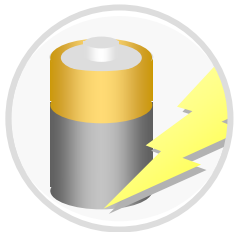
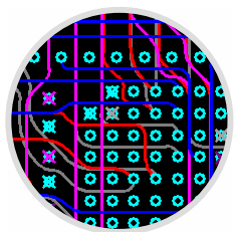
Benefits of Transceiver Integration

Easy Interface Protocol Bridging



Reduced Power Consumption

Eliminated Interoperability Issues



Simplified PCB Design & Real Estate Savings

Integration Reduces Time-to-Market & Lowers System Cost

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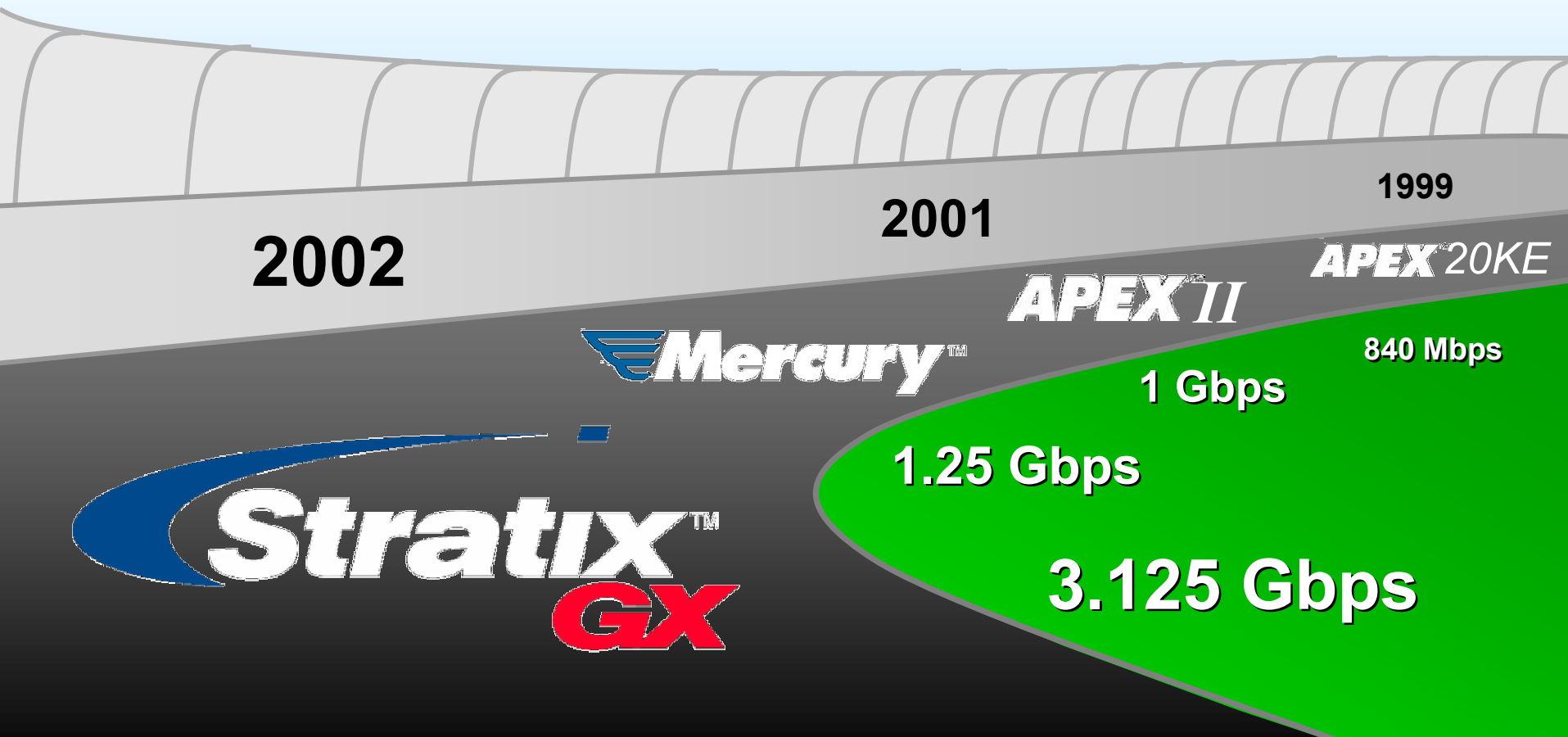
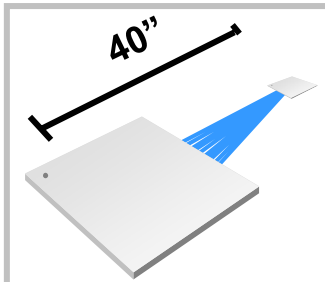
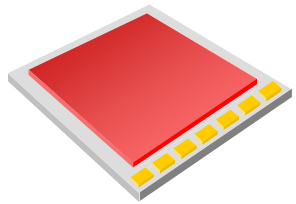
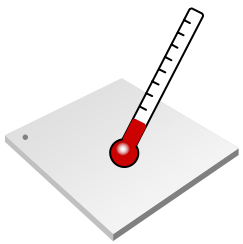
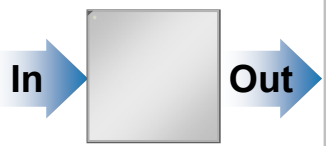
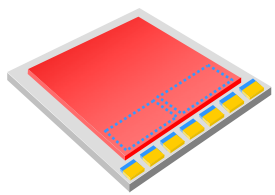
Building on Experience

- Industry Leadership in High-Speed I/O Innovation & Expertise



Experience Drives Success

	Drive Capabilities Suitable for Data Transmission across Backplanes		Optimized Logic-to-Transceiver Channel Ratio & Channel Configuration
	Minimized Power Consumption in Both Transceiver & FPGA		Complete Soft IP Portfolio for Higher-Layer Function Implementation
	Balanced Data Throughput on Transceiver & Source-Synchronous Side		Implementation of Resource-Intensive Functions in Hard IP

Customer End-Product Delivery Is the Goal

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Stratix GX Device Family

Device	Logic Elements	Full-Duplex Transceiver Channels	Source-Synchronous Channels with DPA	Total Memory Bits	DSP Blocks
EP1SGX10C	10,570	4	22	920,448	6
EP1SGX10D	10,570	8	22	920,448	6
EP1SGX25C	25,660	4	39	1,944,576	10
EP1SGX25D	25,660	8	39	1,944,576	10
EP1SGX25F	25,660	16	39	1,944,576	10
EP1SGX40D	41,250	8	45	3,423,744	14
EP1SGX40G	41,250	20	45	3,423,744	14

Supported in Quartus® II Software Version 2.1 Today

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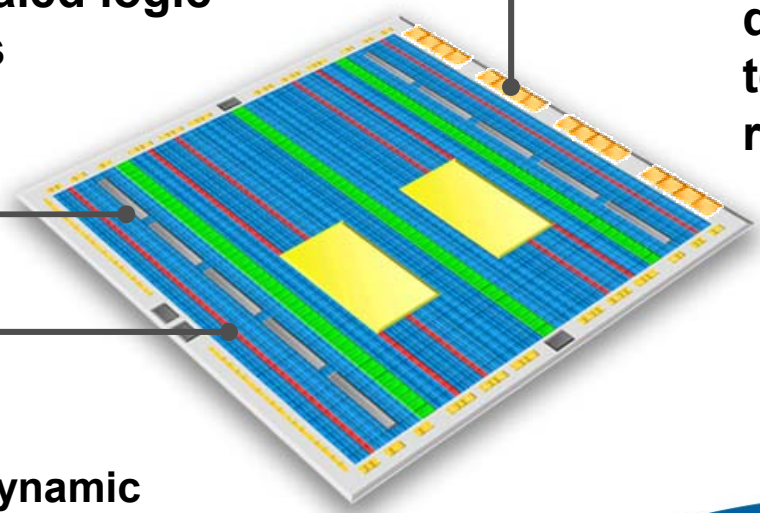
Building on Stratix Architecture

Stratix (străt′ĭks) **n. The industry's fastest FPGA device family offering unrivaled logic & memory resources**

Transceiver (trăn-se′vər) **n. Clock data recovery-based data transmission technology supporting rates up to 3.125 Gbps**



DPA (dē′pē ā) **n. (dynamic phase alignment) Dedicated circuitry for resolving clock-to-channel and channel-to-channel skew, only found in Stratix GX devices**

Stratix™ GX

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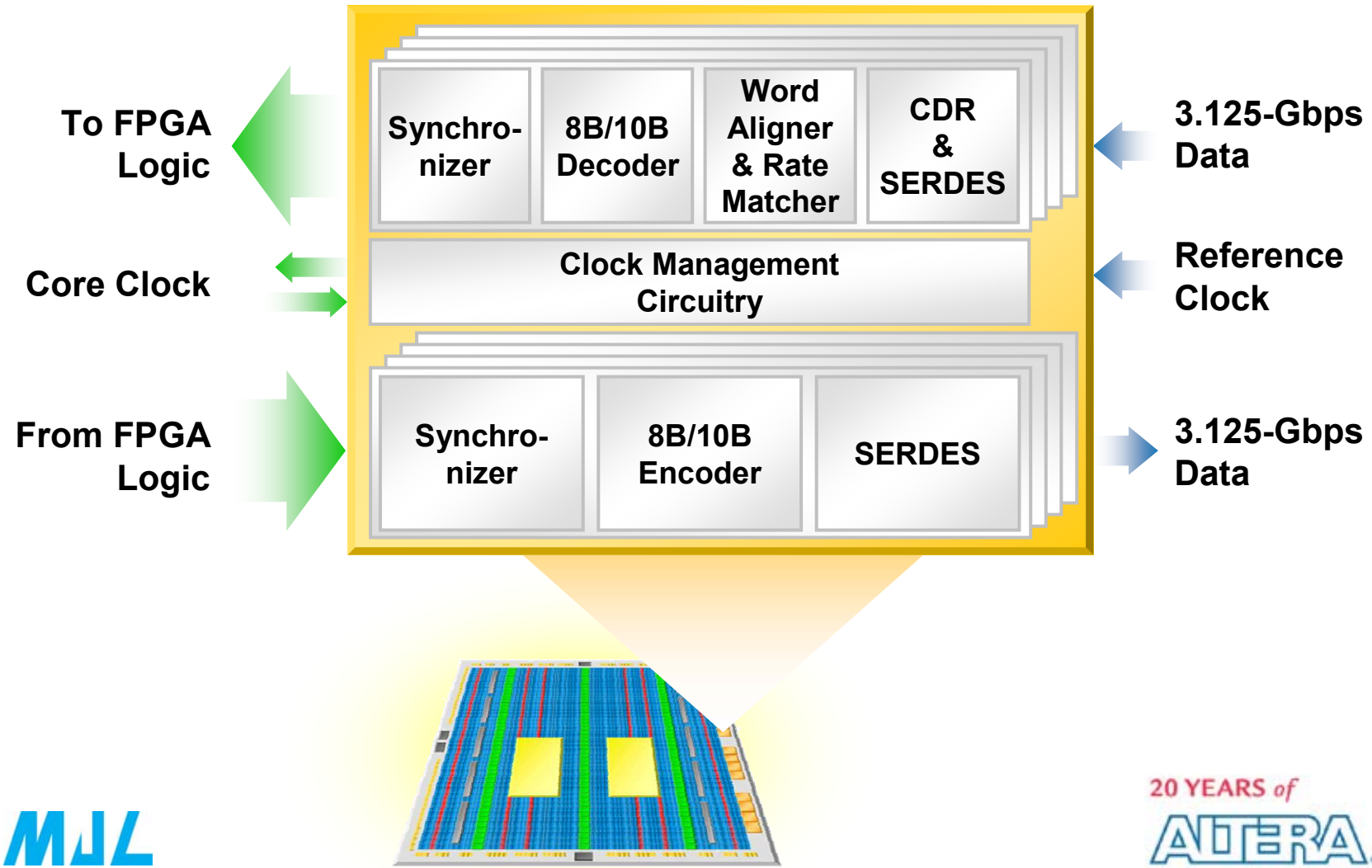
Gigabit Transceiver Block



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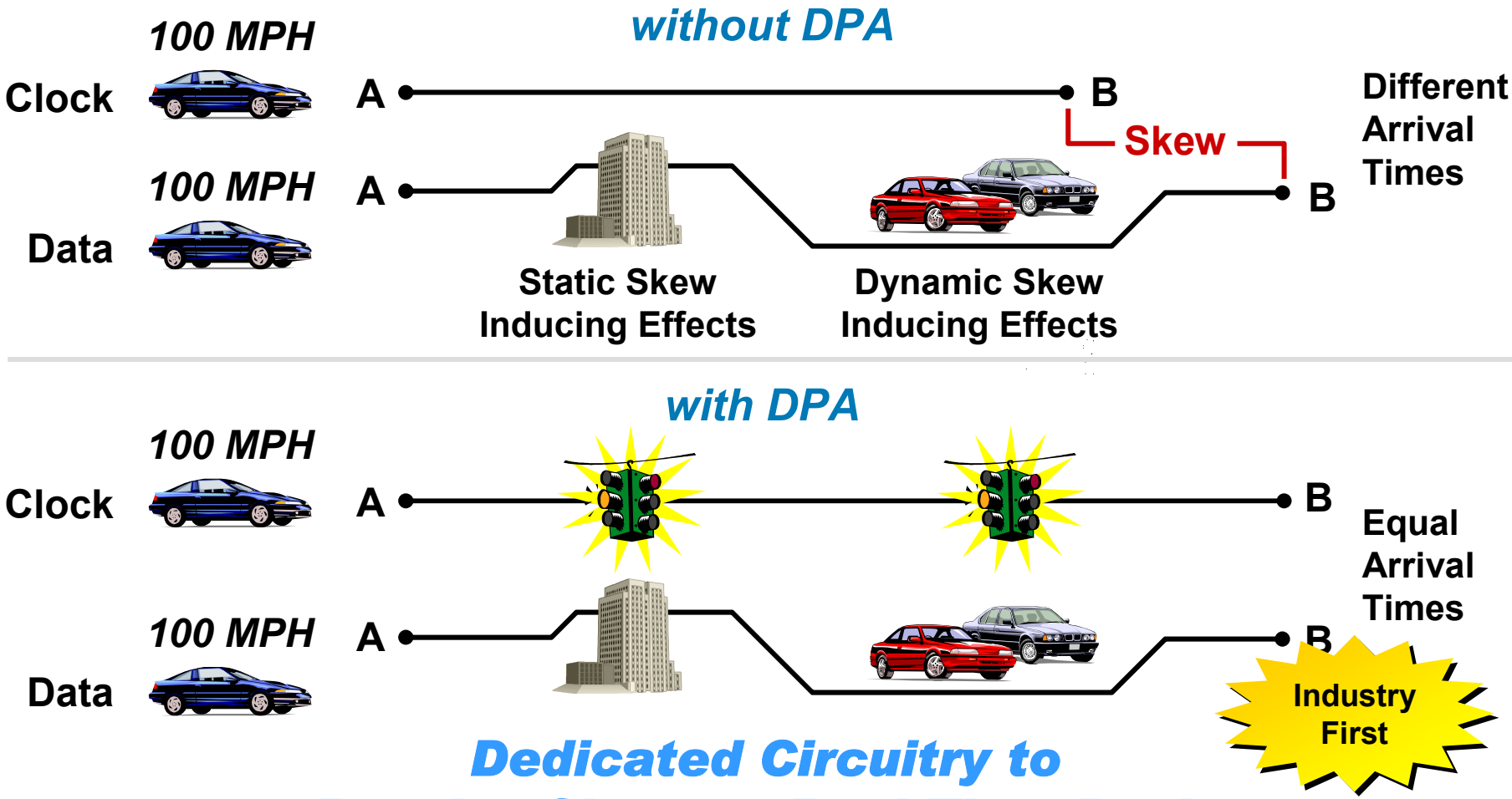
Dynamic Phase Alignment



Dedicated Circuitry to Resolve Skew on Real-Time Basis

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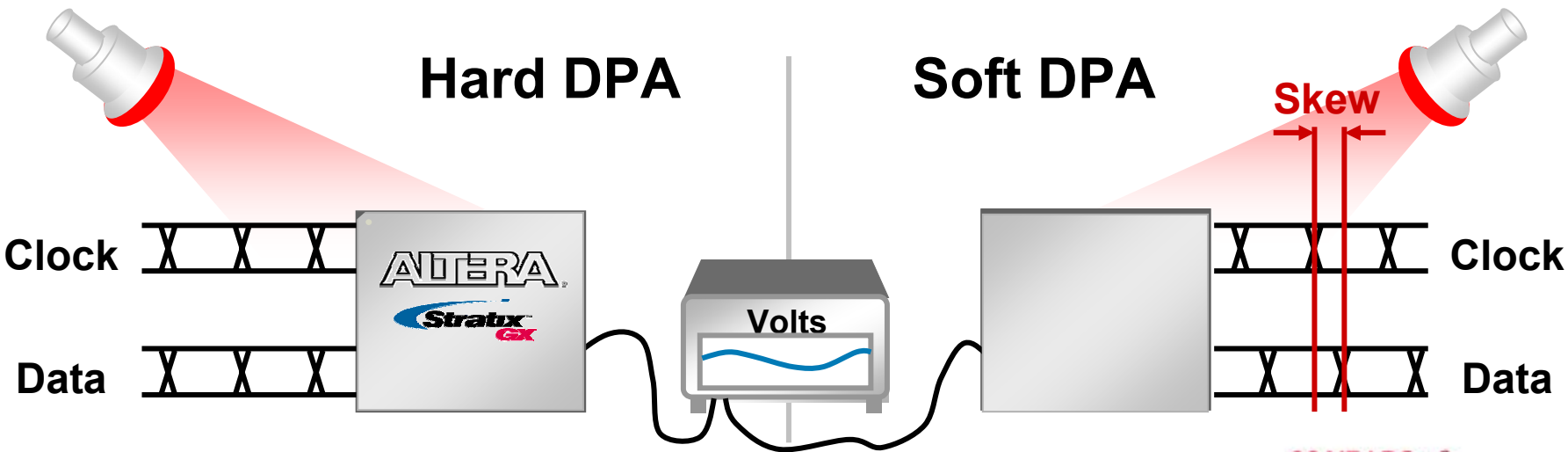
Hard DPA Advantages

- Ease of Implementation
  - Simplifies Complex Clock Management
- Conserves General-Purpose Resources
  - Logic, Global Clocks & PLLs
- Adjusts to Temperature & Voltage Changes



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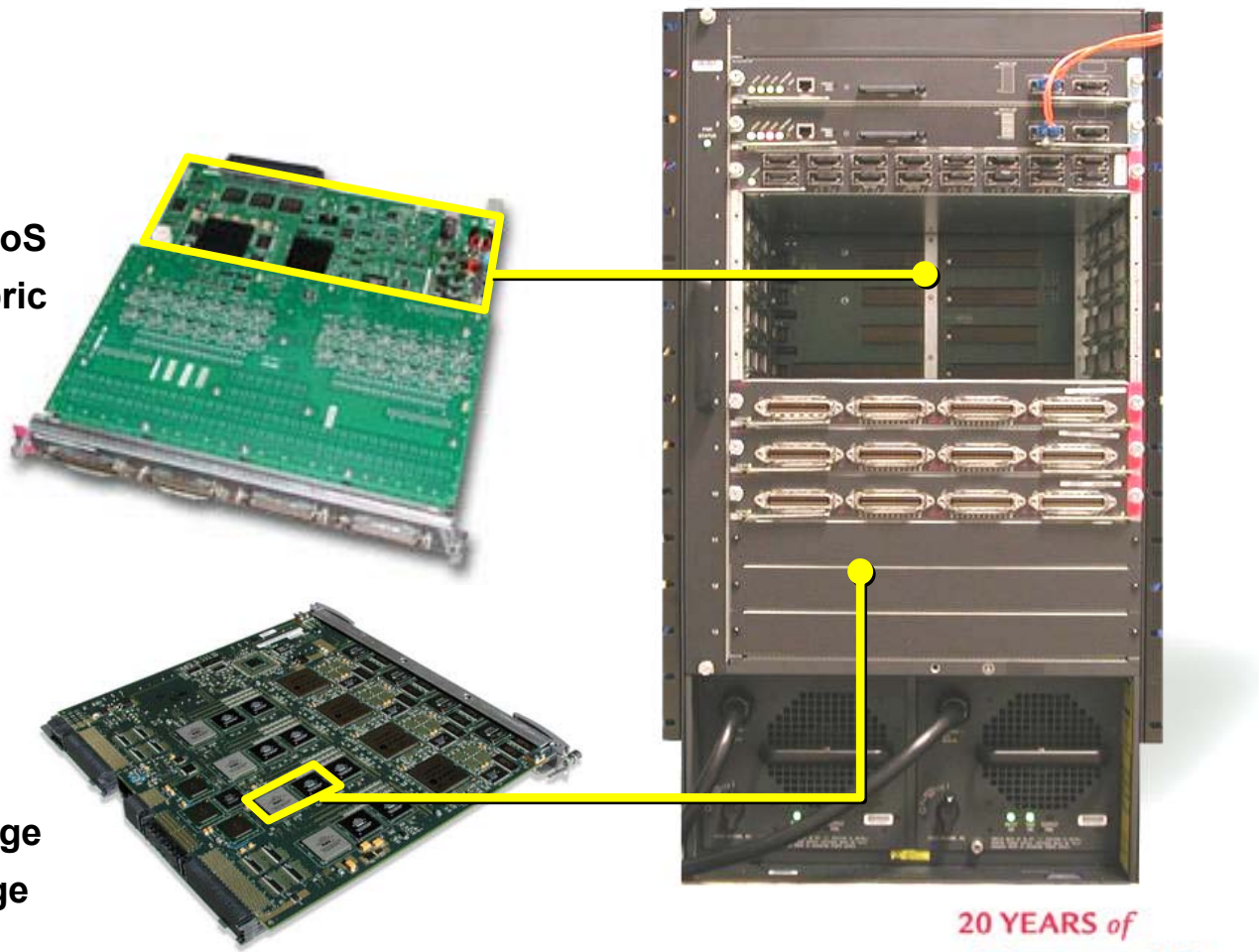
Stratix GX Applications Overview

Backplane Interfaces

- Traffic Management & QoS
- Backplane & Switch Fabric Transceiver

Chip-to-Chip Interfaces

- 10G Ethernet XAUI to XGMII Interface
- 10G Ethernet XAUI to POS-PHY 4 Bridge
- POS-PHY 4 to NPSI Bridge
- NPSI to Backplane Bridge



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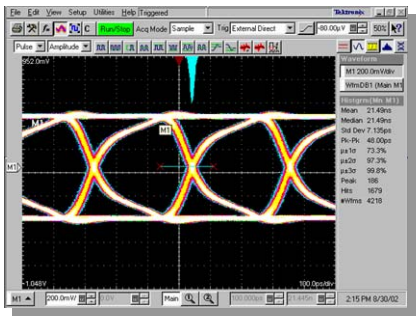
Working 3.125-Gbps Silicon

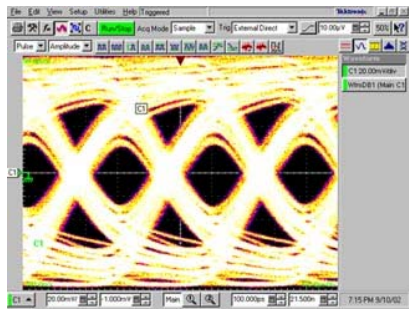
Eye Diagram at Transmitter

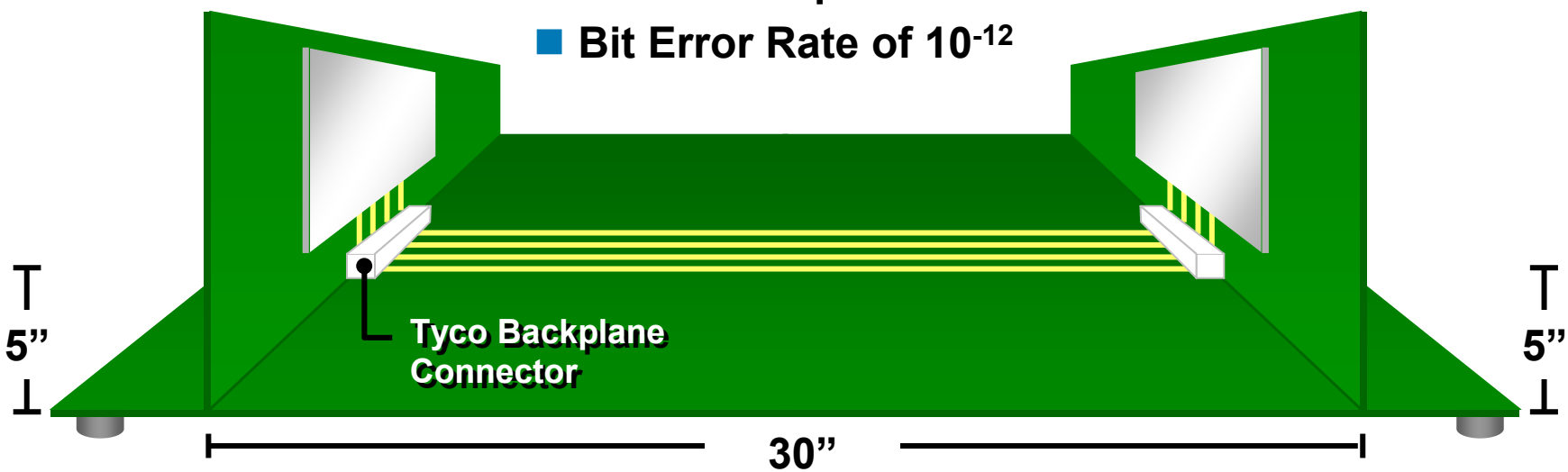


Conditions

- 3.125-Gbps Data Rate
- 40-Inch Trace Length
- PRBS 7 Data
- 0% Pre-Emphasis
- 85ºC, VCC = 1.425 V
- Receiver Equalization
- Bit Error Rate of 10^{-12}

Eye Diagram at Receiver





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Stratix GX Highlights

- Second-Generation Product Reduces Customer Risk
  - Long Distance Drive Capability
  - Power-Efficient
  - Hard DPA Makes it Easy
  - Right Tools & Support
  - Right Hard & Soft IP
- Complete Set of Efficient Hard IP Functions
  - Significantly Reduces Resource Consumption

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Customer Engagement Plan

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Stratix GX Update

- Stratix™ GX Silicon Characterization Exceeding Expectations
- Stratix GX Product Requires Much More than Silicon & Software
- Short-Term Factory Resources Prioritizing Product Completion
- Factory Resources Also Prioritizing Complete Protocol Support Packages

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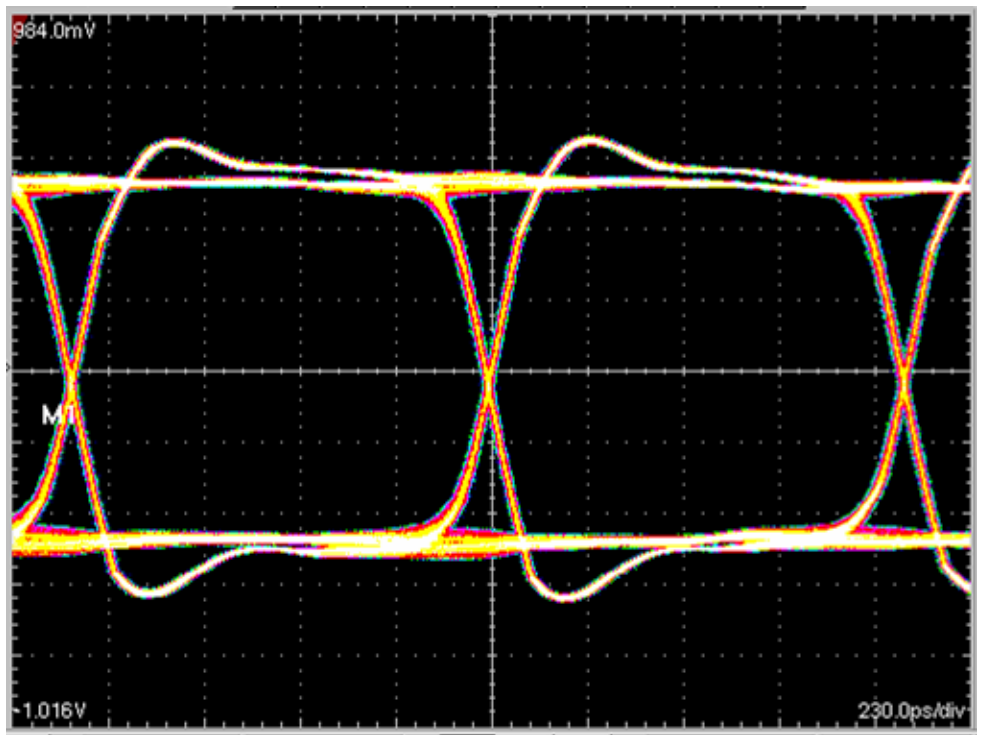
DPA & Source Synch TX

- X8 DPA Loopback Operates beyond 1 Gbps
- TX Output Eye-Pattern at 1 Gbps
- Preliminary Analysis Positive, Characterization Effort Is Ongoing



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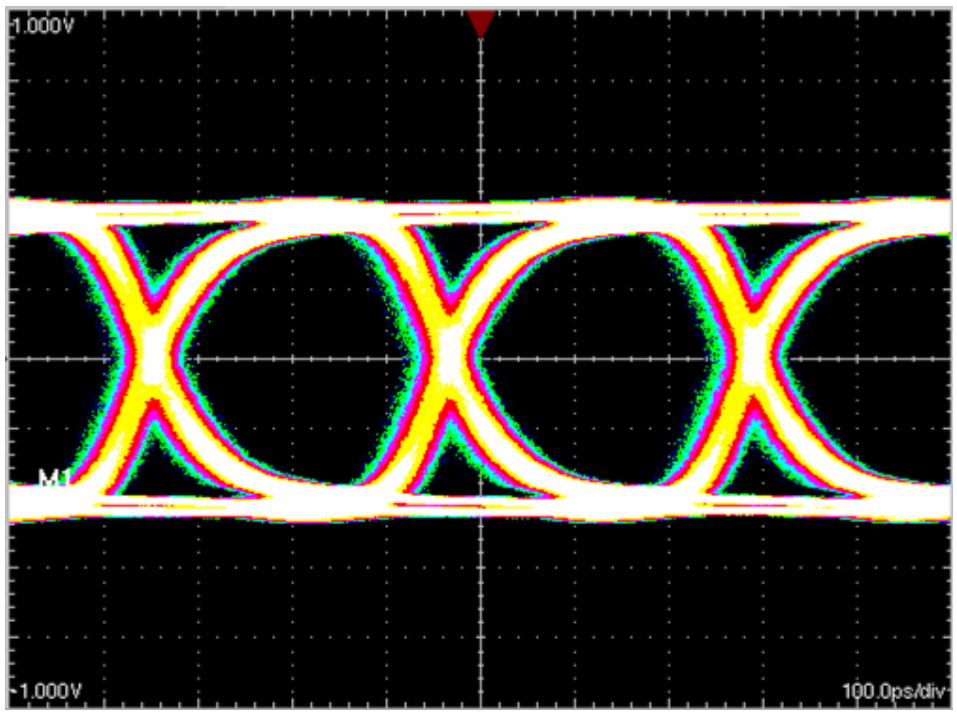
Transceiver Transmitter

- Output Eye Pattern at 3.125 Gbps
- Output Voltage = 1 Volt



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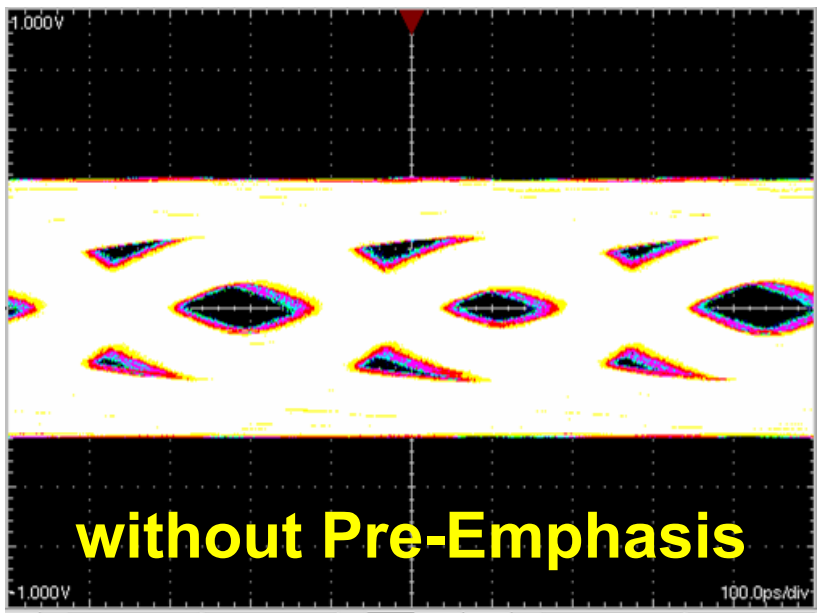
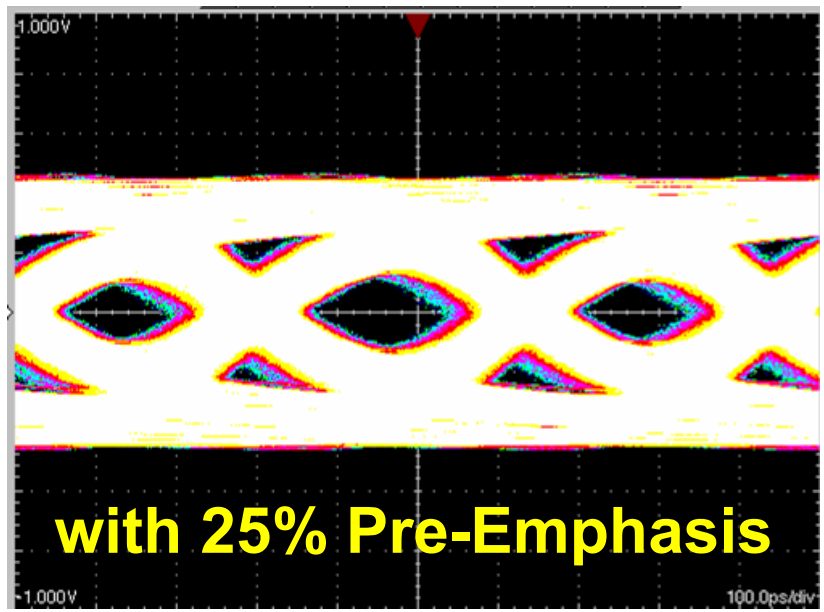
Signal through 40” Backplane

- Transceiver Output Eye-Pattern at 3.125 Gbps
- Output Voltage = 1 Volt





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Stratix GX Whole Product

Stratix GX Whole-Product Components
Working Stratix GX Silicon
Advanced Quartus® II Design Support
Spice Simulation Package
Device-Level Characterization & Documentation
Development Platform
Protocol Characterization & Documentation
IP Cores & Reference Designs
App Notes & Board Design Guidelines
Interoperability Testing
Backplane Characterization

Product Completion Top Priority for 1H-03

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Development Platform

- Development Board
- Board Layout Guidelines
- Reference Designs
- Gerber Files
- Spice Models
- Software Support
- Much More . . .

Development Platform
Dramatically Improves Ease of Design

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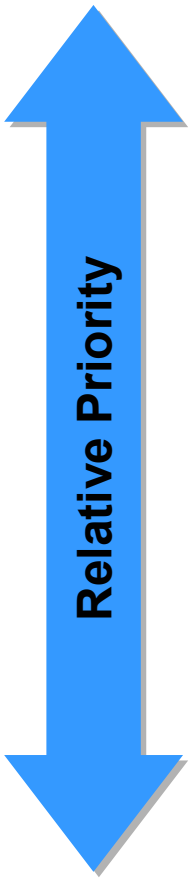
Protocol Prioritization



10 Gigabit Ethernet XAUI SPI-4.2 with DPA SONET/SDH Backplane	First Phase of Rollout Q1 to Q2 2003
Broadcast (SDI – SD/HD) Fibre Channel Gigabit Ethernet	Second Phase of Rollout Q2 to Q3 2003
PCI Express Serial RapidIO SFI-5	2H-03

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Stratix GX Deliverable Schedule

Deliverable	Date
Stratix GX Test Chip Characterization Report	January 2003
Stratix GX Characterization Plan	January 2003
Stratix GX Characterization Regular Updates	January 2003
Stratix GX HSSI Spice Models	February 2003
Stratix GX Development Board Functional Spec	February 2003
Quartus II Compilation Support (No Pinouts)	March 2003
Stratix GX DPA Spice Models	March 2003
Stratix GX Development Platform ($20K)	June 2003
Full Support in Quartus II Version 3.0	June 2003

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Early Adopter Engagement Plan

- Customer / Field Completes Detailed Questionnaire
  - Assess Customer Design Capability & Application (Protocol)
- Altera & Customer Decide if Opportunity Aligns with Stratix GX Schedule & Altera Support Capability
- Service-Level Disclosure with Customer
- Share Deliverables with Customers

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Service-Level Disclosure

- Outlines Nature of Engagement with Customer
  - Altera Commits to Providing Customer with Silicon, Support & Technical Details
  - Customer Must Sign Non-Disclosure Agreement
  - Customer Agrees to Accept Staged Information & Silicon Release
  - Disclosure Clarifies Schedules on Remaining Device & Protocol-Characterization Effort & Collateral Plan

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Engagement Guidelines

- Customer Requirements to Start Engagement
  - Sign Non-Disclosure Agreement
  - Complete Questionnaire
  - Commit to Purchase a Stratix GX Development Platform
  - Agree to Provide Feedback on Evaluation Stratix GX Results

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