20 YEARS *of*

ALTERA®

INNOVATION

SOPC WORLD 2003

Timing-Driven Design for Optimal Area & Performance

October 2003

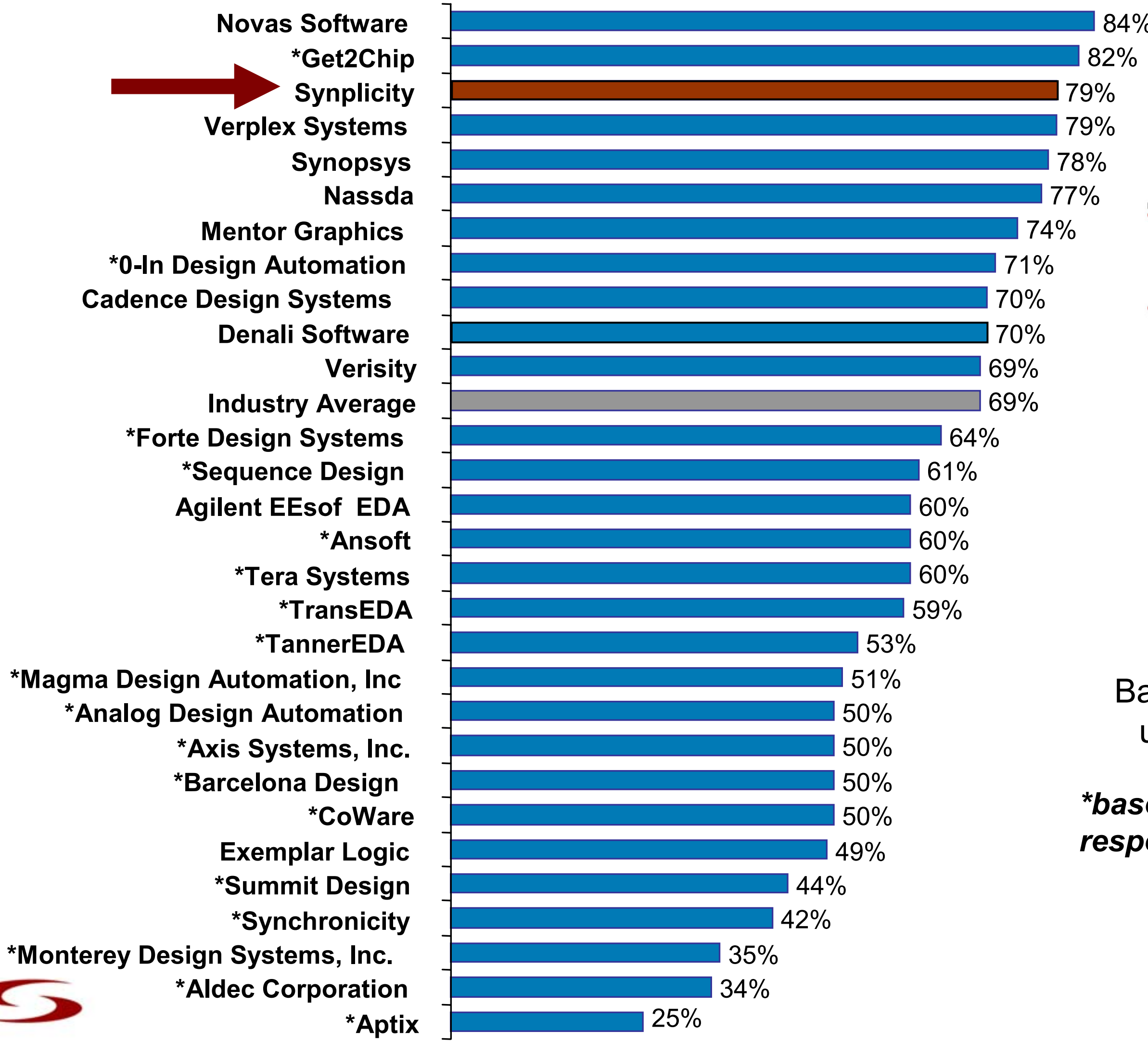
Agenda

- Synplicity Overview
- Synplicity's Solutions
- Identify Demo

Synplicity, Inc.

- EDA software company founded in 1994
- Unique company philosophy
  - Best results don't have to come from hard to use tools
  - Flexible and easy to work with company
  - Dedicated to providing the best technical support
- FPGA expertise
  - Synthesis
  - Physical Synthesis
  - Debug

Top Ranking in Customer Satisfaction



ELECTRONIC ENGINEERING EETIMES

Customer Satisfaction June 2003

Base = # who have purchased or used a product from the vendor

base too small (20 or fewer responses); interpret data with caution

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Synplicity's Design Solutions

Synthesis SOLUTIONS

- **Synplify® & Synplify Pro®** Advanced FPGA Synthesis
- **Synplify ASIC®** High Performance ASIC Synthesis

Verification SOLUTIONS

- **Certify®** ASIC RTL Prototyping Software
- **Identify™** RTL Debugger

Physical Implementation SOLUTIONS

- **Fortify™** Family of Power Products
- **Amplify® Physical Optimizer™** Physical Synthesis for FPGAs

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Top FPGA Design Challenges

As described by today's FPGA designers

- Achieving Performance Goals
- Timing Closure
- Productivity
- Debug
- Prototyping

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Achieving Performance Goals

(Synplify & Synplify Pro)

Performance Goals

- Synplify (Mappers) are architecture aware
- Optimizations are performed based on timing constraints
  - Hierarchical boundary optimization
- BEST™ algorithms extract high level components
  - RAM's, FSM's, wide muxes, adders/multipliers, etc.
  - Technology-specific optimizations made *after* extraction

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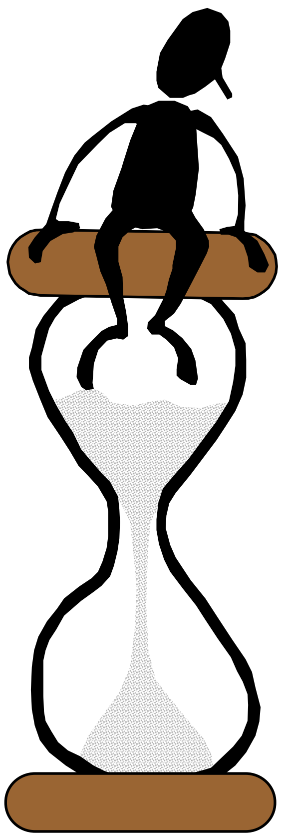
Set Proper Timing Constraints



- Synplify and Synplify Pro are timing driven
  - Optimization decisions are made based on the timing constraints
  - Not simply optimizing for performance or area
  - Saves on device cost by using the smallest part while meeting your timing
- Forward annotation to P&R
  - Timing information is forward annotated to Quartus place & route
  - More detailed and accurate timing constraints yield the best results

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Basic Clock Options

SCOPE®

- **Frequency / Period**
  - Enter one (displayed in bold)
  - Others are automatically derived (regular font)
- **Clock Group**
  - Default clock group: *default_clkgroup*
  - Only paths between clock domain from the same clock group are analyzed
- **Use real constraints for your design – don't over constrain**
- **To optimize strictly for area set frequency to 1MHz**

	Enabled	Clock	Frequency (MHz)	Period (ns)	Clock Group	Clock Rise (ns)	Clock Fall (ns)	Duty Cycle (%)	Route (ns)	Virtual Clock
3	☑	clk3	**100**	10.000	D1			50	2	☐
4	☑	clk4	83.333	**12.000**	D1			50		☑

Clocks | Inputs/Outputs | Registers | Multi-Cycle Paths | False Paths | Attributes | Other

Advanced Clock Options

- Rise, Fall, Duty Cycle
  - Use *Clock Rise/Fall* to specify rising and falling edges
    - duty cycle automatically derived
  - OR Specify the clock cycle as a % of the clock period
    - rise reset to 0, fall automatically derived
  - Default is Rise=0, Fall=period/2, Duty Cycle=50%
- Route
  - Use to shrink the effective clock period without affecting the clock constraint forward-annotated to Quartus P&R
- Virtual Clock
  - Use for external clock signals clocking top-level ports

IP Support

- Altera Clearbox support allows Synplify to perform realistic timing analysis, optimizations, and reporting
  - Synplify Pro only
- Mixed language support
  - Synplify Pro only

Forward Annotation to Quartus

- Timing constraints forward annotated to Quartus Place & Route
  - Frequency
  - Duty Cycle
  - I/O Delay
  - Multi-Cycle Paths
  - False Paths & max_delay path
  - Clock Relationships
  - Pin Assignments
- Accomplished through .vqm & .tcl

Timing Closure
(Amplify Physical Optimizer)

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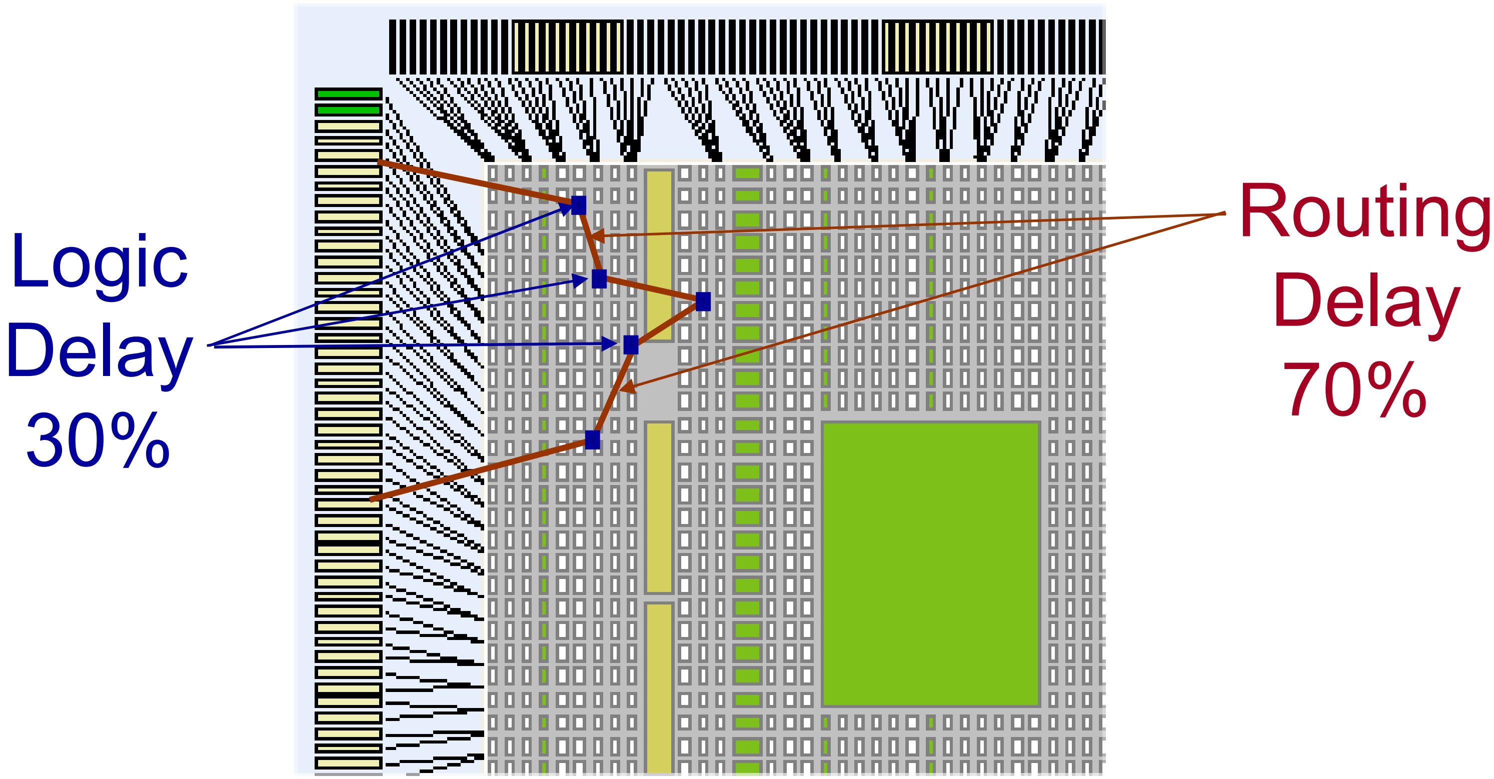
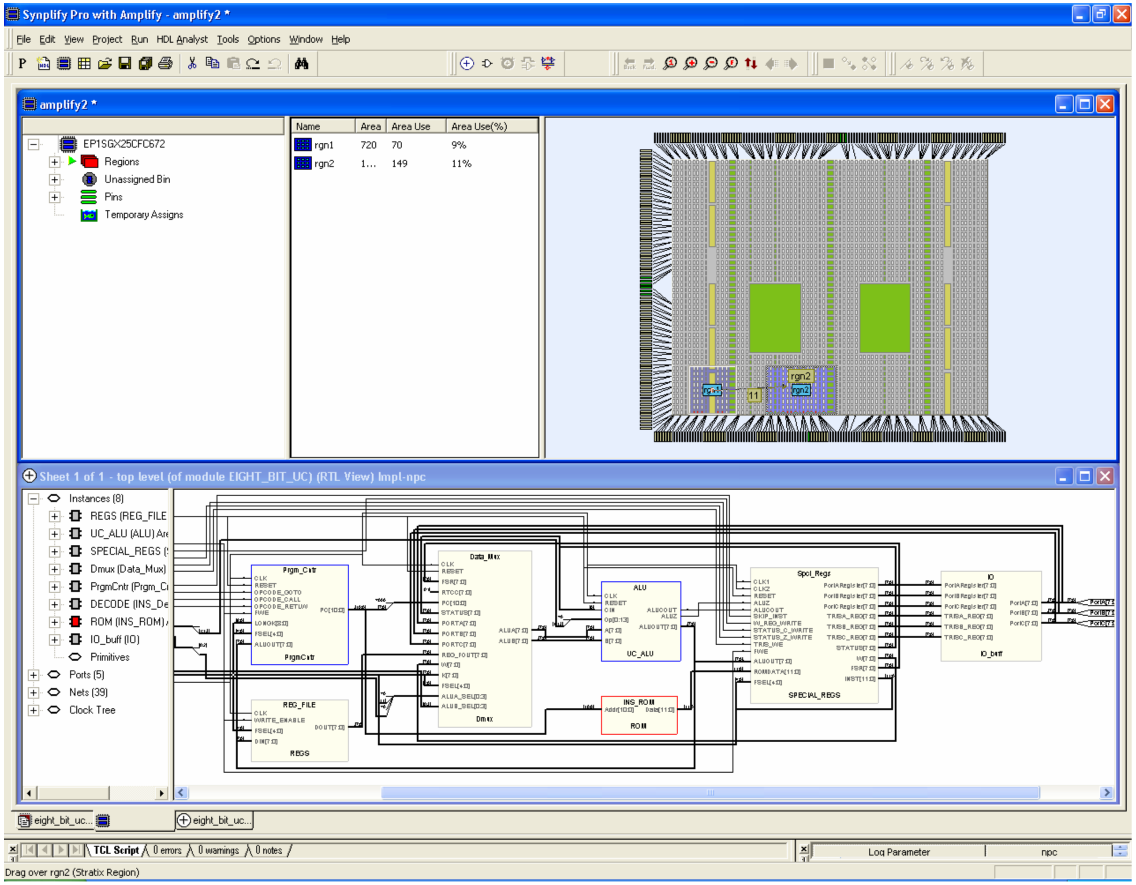
Routing Governs Performance



- Must incorporate physical information into synthesis
- The larger the design, the larger the problem

Amplify Physical Synthesis

- Simultaneous placement and optimization
- Integrated Design Planning guides physical optimization
- Boosts performance an average of 20% over synthesis



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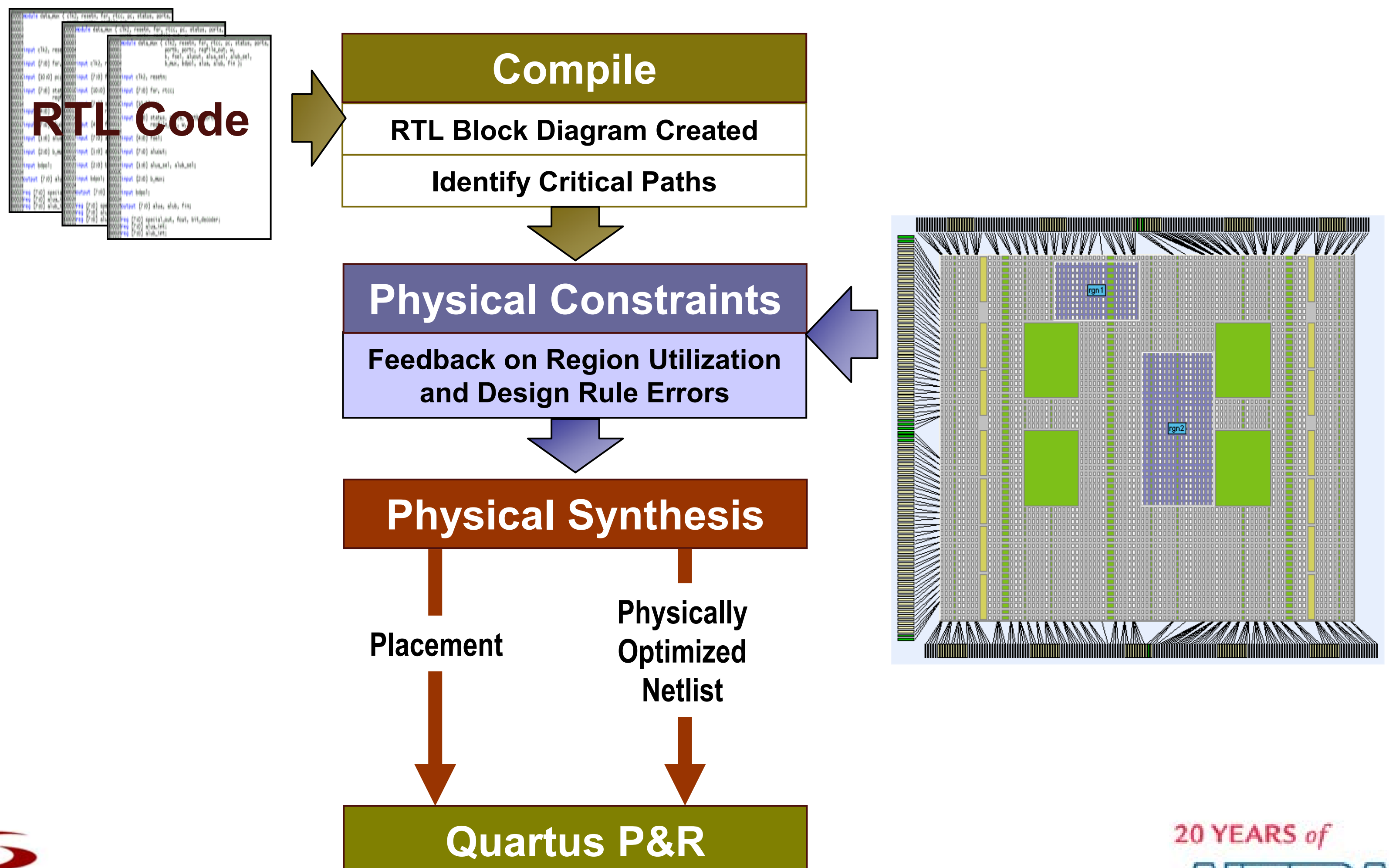
When To Use Amplify

- For fast timing closure
- When you need the highest possible performance
- Need to reduce a speed-grade for cost
- When the majority of delay is in routing

Amplify – Interactive Flow



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Types of Physical Constraints

- Module Level Physical Constraints
  - Logical module
  - Use when critical paths are within logical modules
- Detailed Level Physical Constraints
  - Point to point critical path
  - Use when critical paths cross module boundaries

    OR
  - When meeting timing within a module becomes critical

Benefits of Physical Synthesis

- Synthesis with physical constraints provides
  - Simultaneous placement and logic optimization
  - Placement based optimization
  - Register replication for high fanout nets across region boundaries
  - Register tunneling across boundaries
  - Replication and re-assignment of registers that drive primary I/Os
  - Placement of logic constrained to regions

Value of Using the Best Synthesis

- **Saves you money**

$100 / chip

$120 / chip

$144 / chip

20% premium for 12%-15% performance

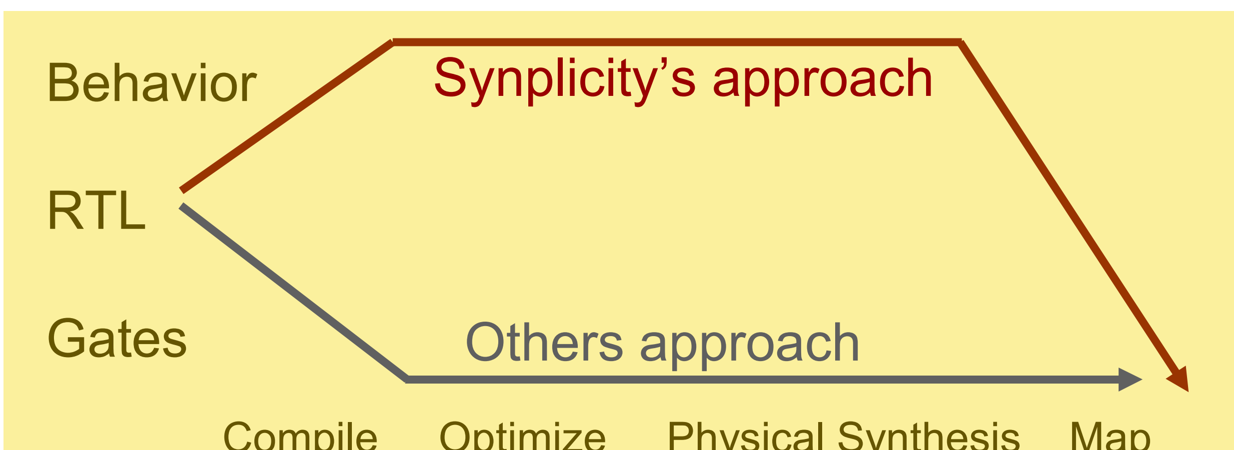
Savings are huge for volume applications

- **Makes your products more competitive**
  - Better performing chips make a better product
  - Reaching timing goals quickly gets you to market sooner

Design Productivity (Synplify & Synplify Pro)

Core Synthesis Technology

- **BEST™ – Behavior Extracting Synthesis Technology®**
  - Infers and optimizes behavior from RTL
  - Optimizes across hierarchical module boundaries
  - Integrated physical synthesis algorithms
  - Multi-million gate capacity
  - Extremely FAST - Unparalleled runtimes



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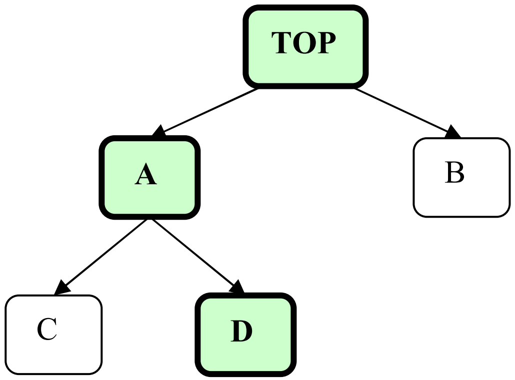
Managing Complex Designs

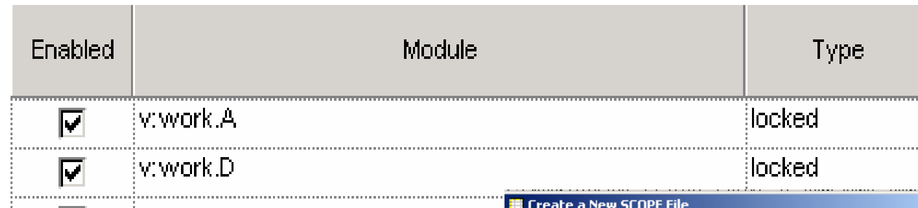
MultiPoint™

- **A Powerful Synthesis Flow for**
  - Incremental design using Synplify Pro or Amplify
  - Unlimited gate capacity
  - Minimal scripting effort
  - No compromise Quality of Results
  - Altera Logic Lock flov

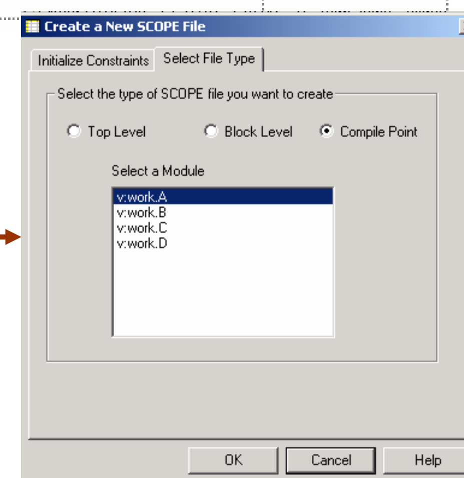
LogicLock™

MultiPoint Flow





Define compile points and compile point constraints



First Run

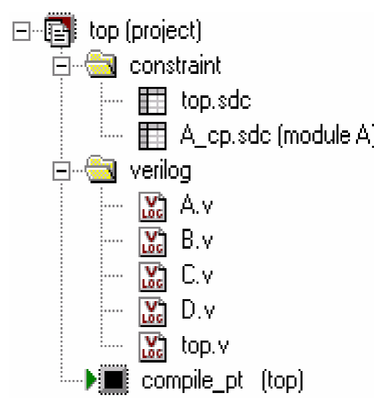
```
Summary of Compile Points

Name        Status      Reason
-------------------------------
D           Mapped      No database
A           Mapped      No database
top         Mapped      No database
===============================
```

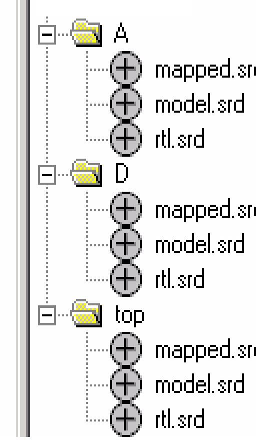
Second Run

```
Summary of Compile Points

Name        Status      Reason
-------------------------------
D           Remapped    Design changed
A           Unchanged   -
top         Unchanged   -
===============================
```



Project View



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MultiPoint Synthesis

Difference Based Incremental Synthesis

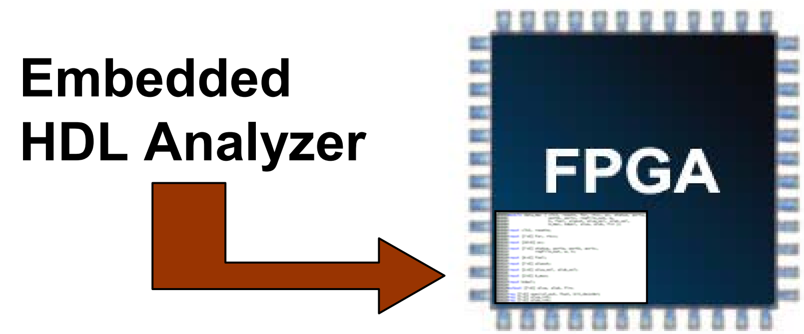
Re-synthesize a locked Compile Point module for:

- A logic change in your RTL code
- Changes to constraints
  - Timing constraints change in the .sdc or Project View
  - Project settings change
    - FSM Compiler or Explorer
    - Retiming
    - Pipelining
- Re-synthesis is not based on time stamp

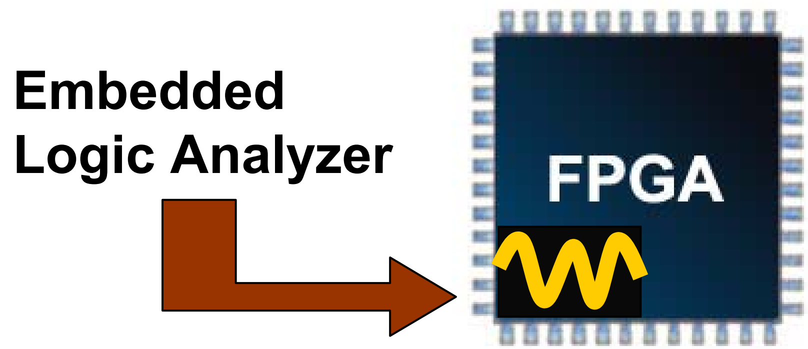
Debug (Identify)

Evolution of Hardware Debug

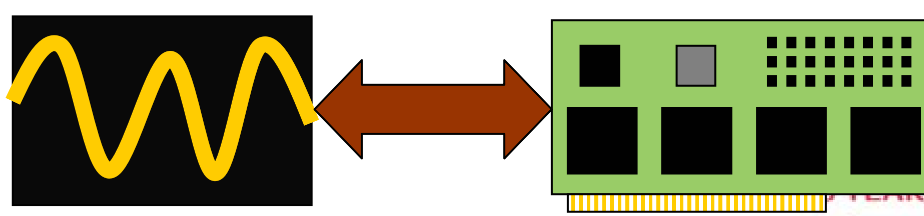
Identify
(Simulator-Like)



SignalTap
(Logic Analyzer-Like)



Logic Analyzer



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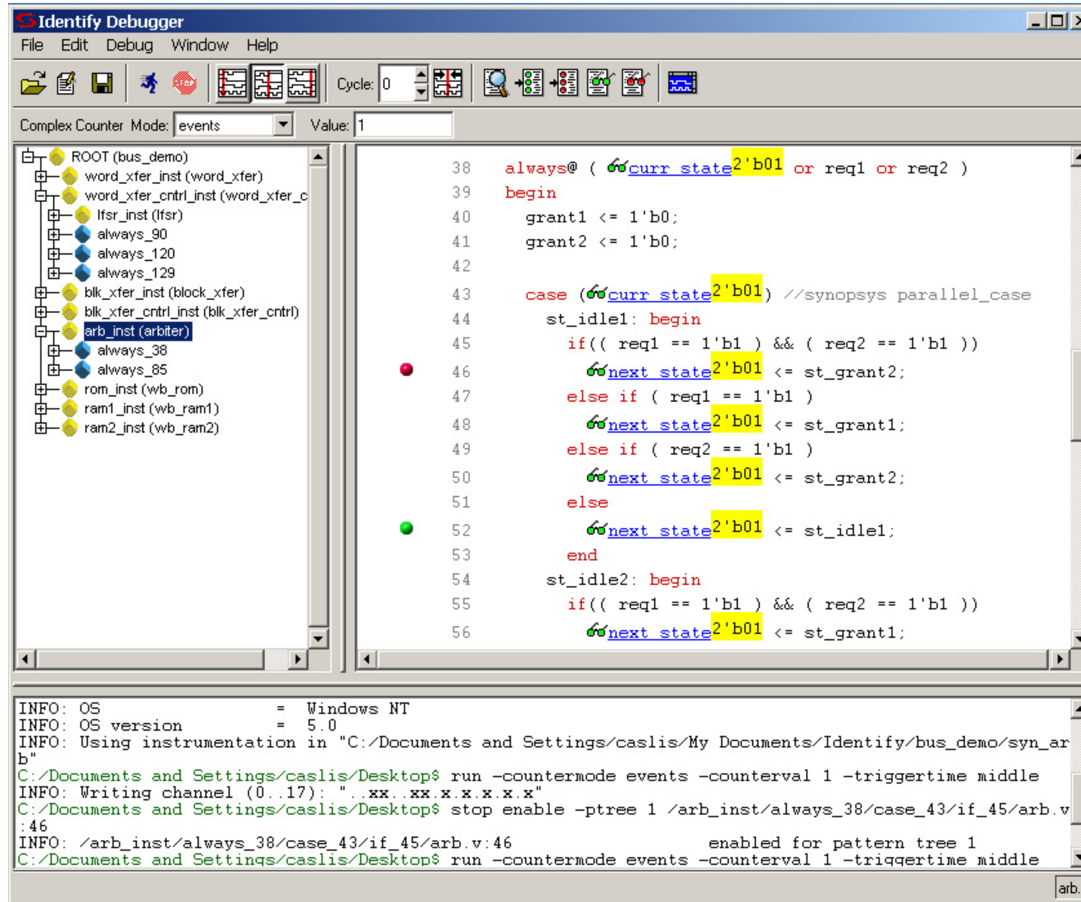
Identify RTL Debugger

- Debug and instrument FPGA directly in RTL code
- Provides internal visibility in the target system at full speed
- Trigger on Data Path and Control Path
- Standard VCD Output for Waveform Display



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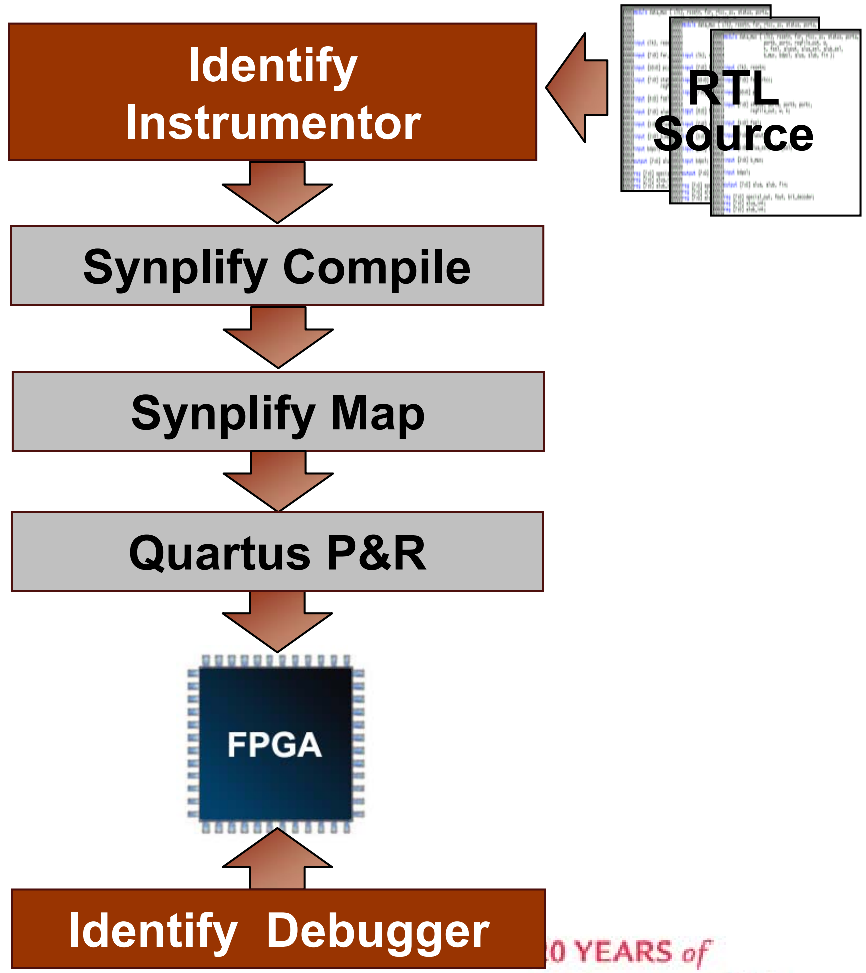
Design Flow with Identify

- Read RTL into Identify Instrumentor
- Compile and map Identify output in Synplify
- FPGA Place & Route
- Use Identify Debugger to view data in FPGA



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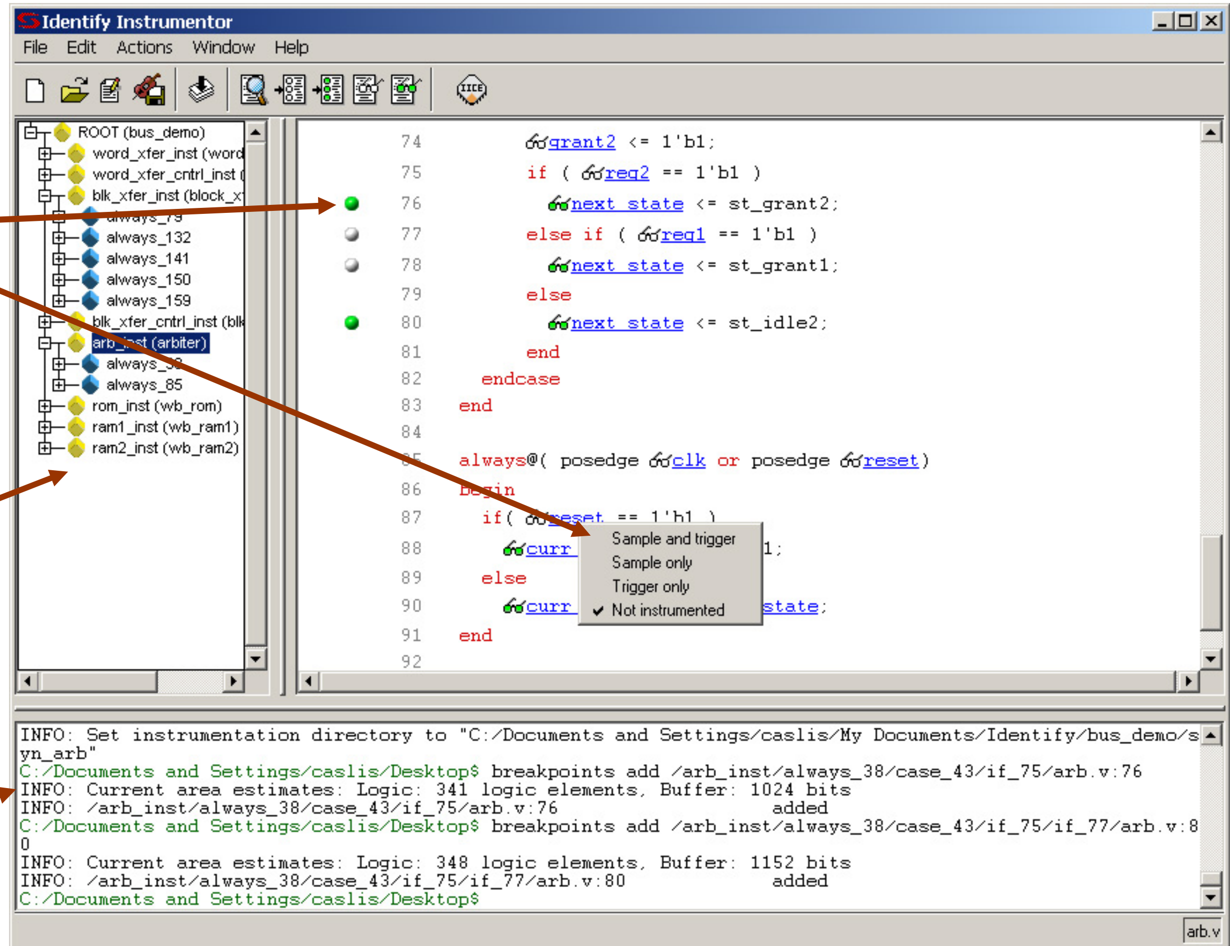
Instrumenting for Debug

Add Signal Visibility

Design Hierarchy

TCL Scripting Interface



Identify Instrumentor

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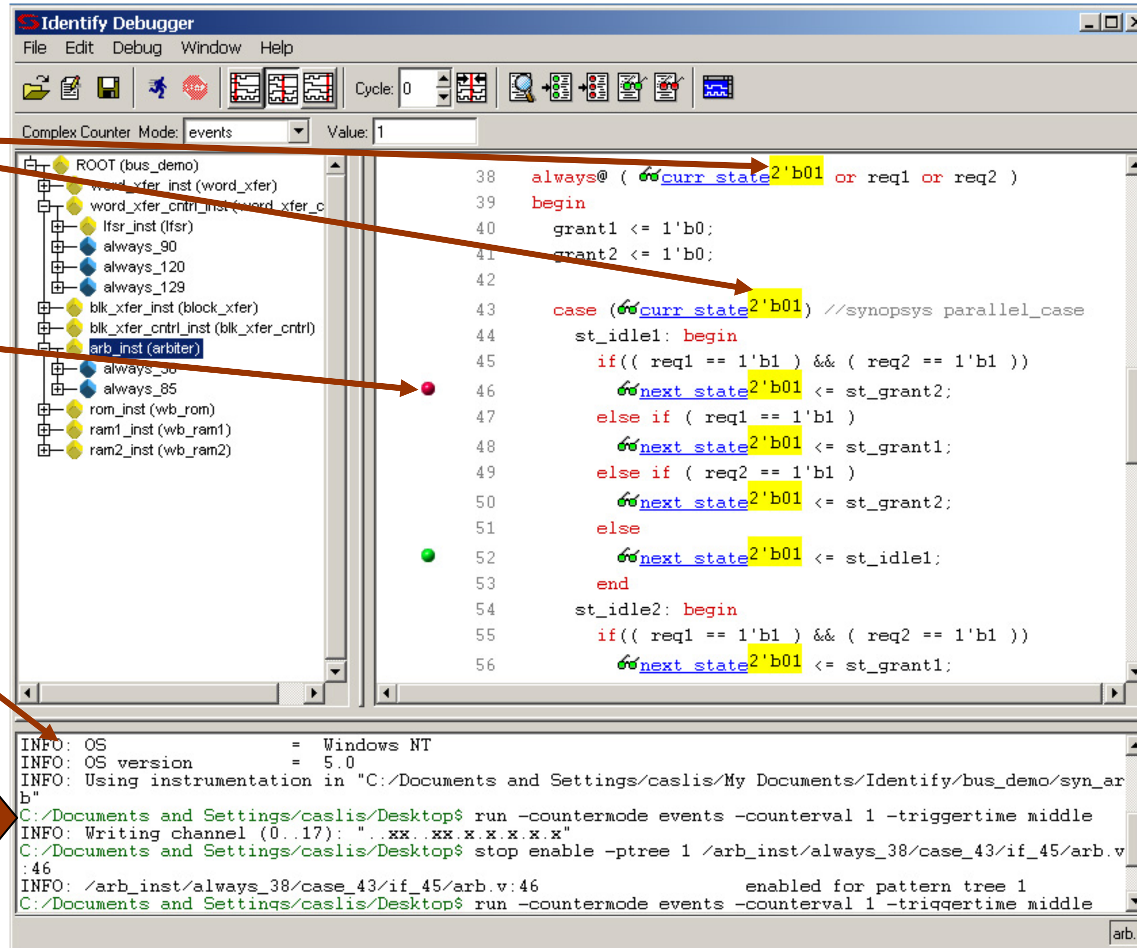
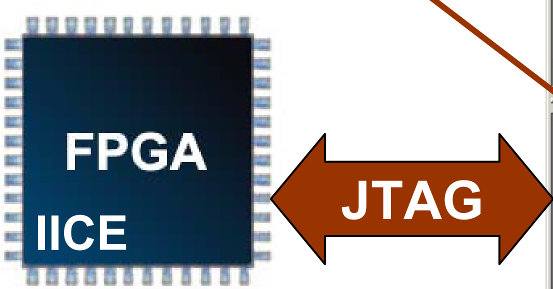
Debugging Data From FPGA

Actual data from FPGA

Click to enable triggers

Automate Debugger with Script





Identify Debugger

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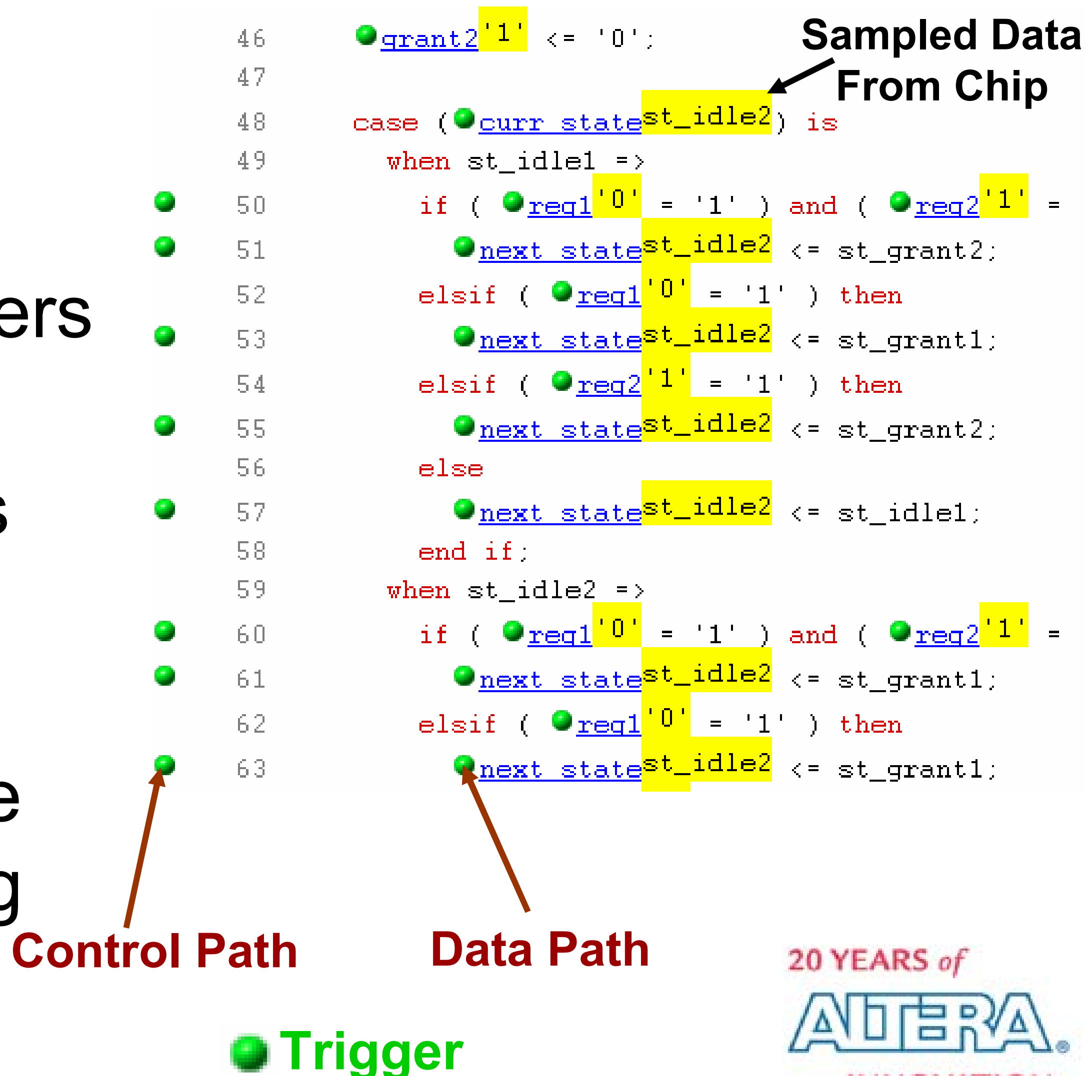
RTL Display of Triggers and Sampled Data

- Full support of symbolic values
- Control Path triggers as breakpoints
- Data Path triggers as watch points
- Configurable counters and state machine triggering



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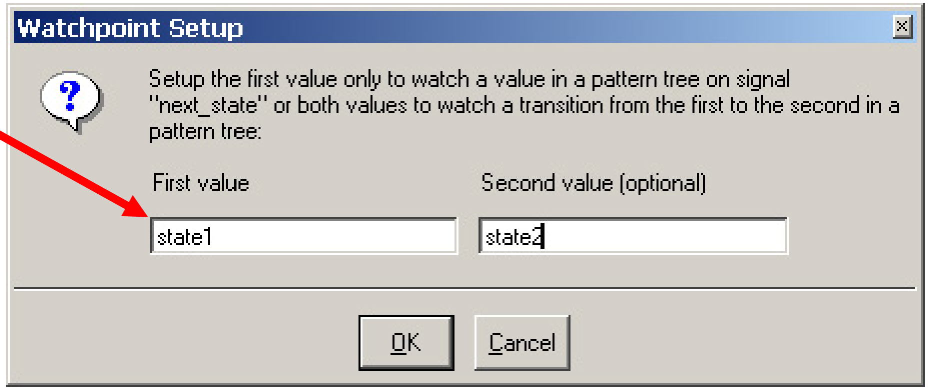
Setting Triggers on Data Path

```
ex : PROCESS (a, b) BEGIN
 CASE curr_state IS
  WHEN read_state  =>
    IF b = "100110" THEN
       o <= "110";
    END IF;
  WHEN OTHERS =>
    o <=  "000";
  END CASE;
END PROCESS;
```



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Setting Triggers on Control Path

```
ex : PROCESS (a, b) BEGIN
 CASE a IS
  WHEN read_state  =>
    IF b = “100110” THEN
       o <= “110”;
    END IF;
  WHEN OTHERS =>
    o <=  “000”;
  END CASE;
END PROCESS;
```

1 — **a == read_state**

2 — **a == read_state && b == “100110”**

3 — **a != read_state**

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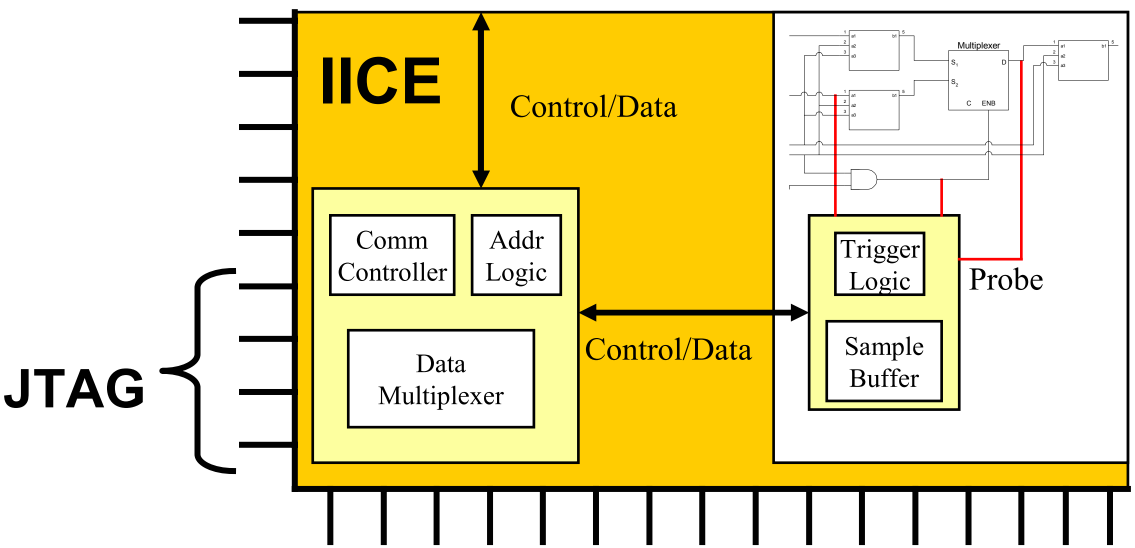
Intelligent In-Circuit Emulator (IICE™)

- Inserted logic used by Instrumentor & Debugger
- Uses dedicated JTAG pins or user-selected pins
- Includes controller, triggering logic, & data storage buffer



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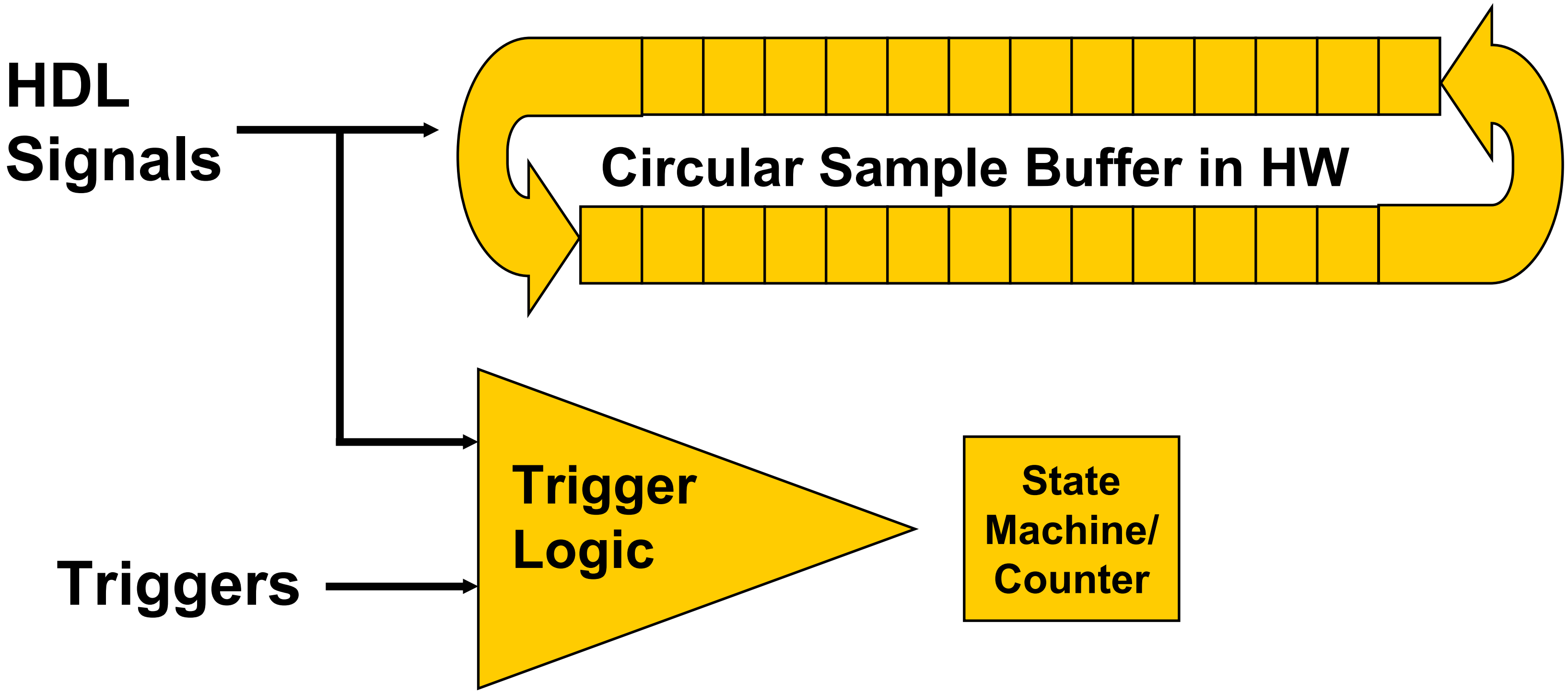
Triggering Logic and Buffer



- Trigger values changed dynamically from debugger
- Trigger halts sampling, Not hardware
- Triggers pipelined, only 2 gate delay

Customer Success

Foundry Networks

"In just our first six weeks with the product, we used it to find and fix bugs in three of our designs. In each case the process was completed within a day. It would have taken 10 to 20 times longer using traditional test-bench methods."

-Richard Grenier

Director of ASIC Development

Multi-FPGA Prototyping (Certify)

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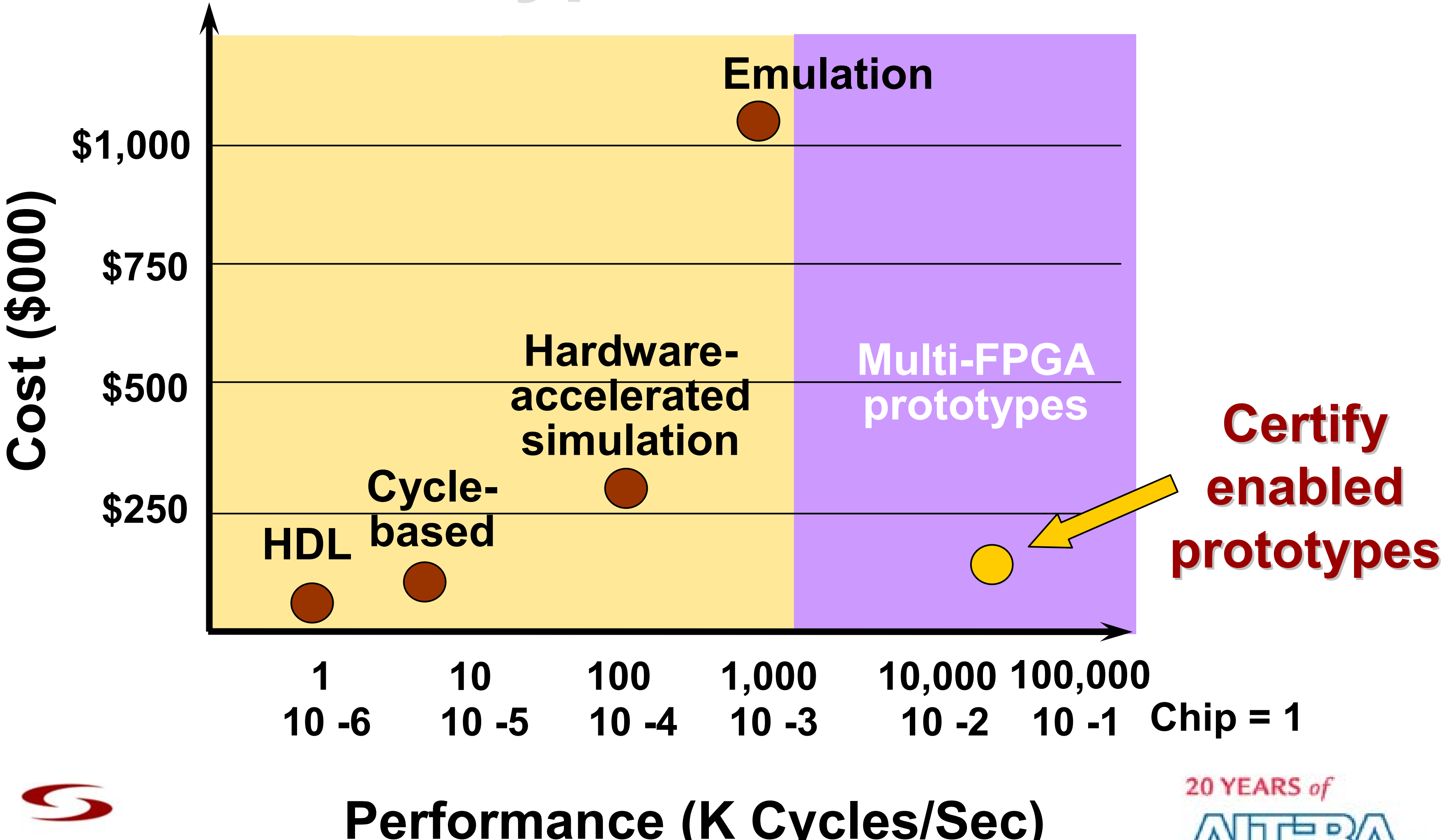
Higher Speed & Lower Cost using FPGA Prototypes



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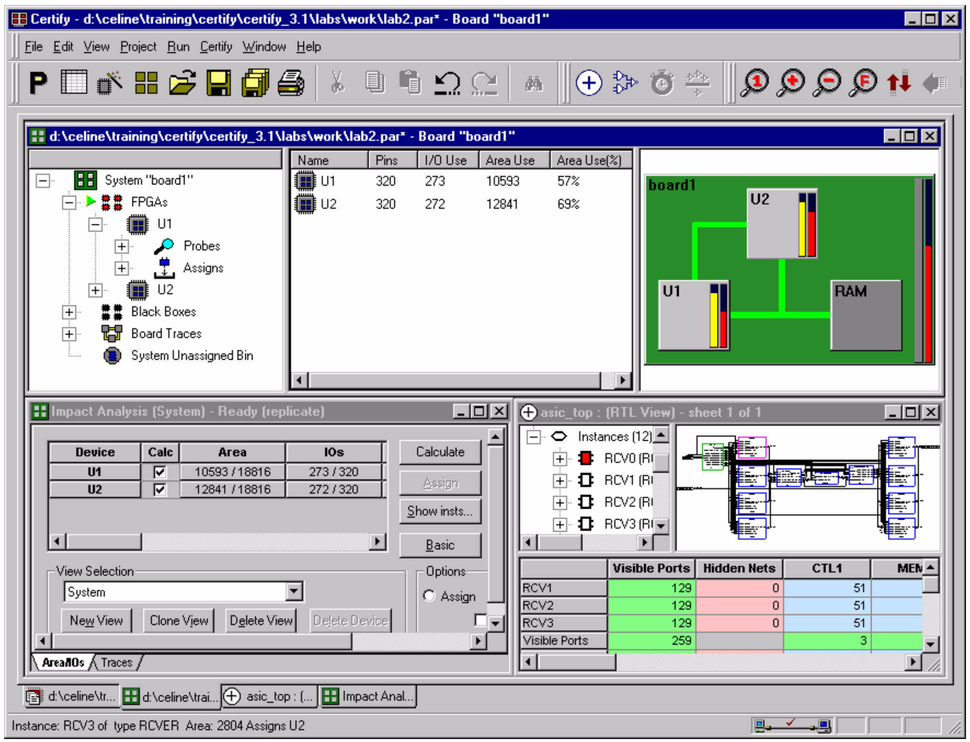
Prototyping Challenges

- ASIC RTL Code
  - Gated Clocks
  - DesignWare™
- Performance
  - Video and signal processing applications
- Partitioning
  - Pin utilization

FPGA-Based ASIC Prototypes



- **Highest performing ASIC prototypes for**
  - Functional verification
  - HW/SW co-verification
- **Automatic RTL partitioning, I/O sharing, and more**
- **Supports all prototyping hardware including off-the-shelf boards**
- **Adopted by Philips, TI, LSI Logic and others**

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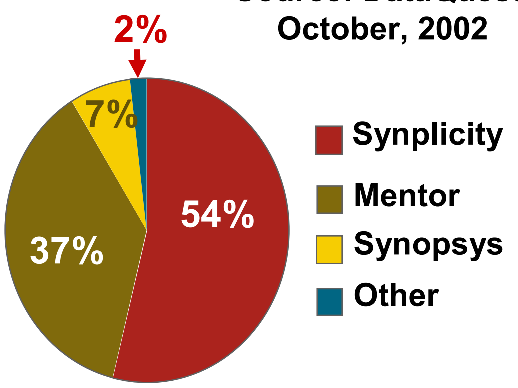
Summary

- The Market Leader in FPGA synthesis & physical synthesis
  - Best Quality of Results
  - Unmatched Productivity
- A Leader in EDA innovation
  - First in FPGA physical synthesis
  - Innovative, at-speed, RT-Level debug technology
  - Unique multi-FPGA prototyping system
- Top-ranked customer service and technical support

FPGA Synthesis Market Share
Source: DataQuest, October, 2002



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END