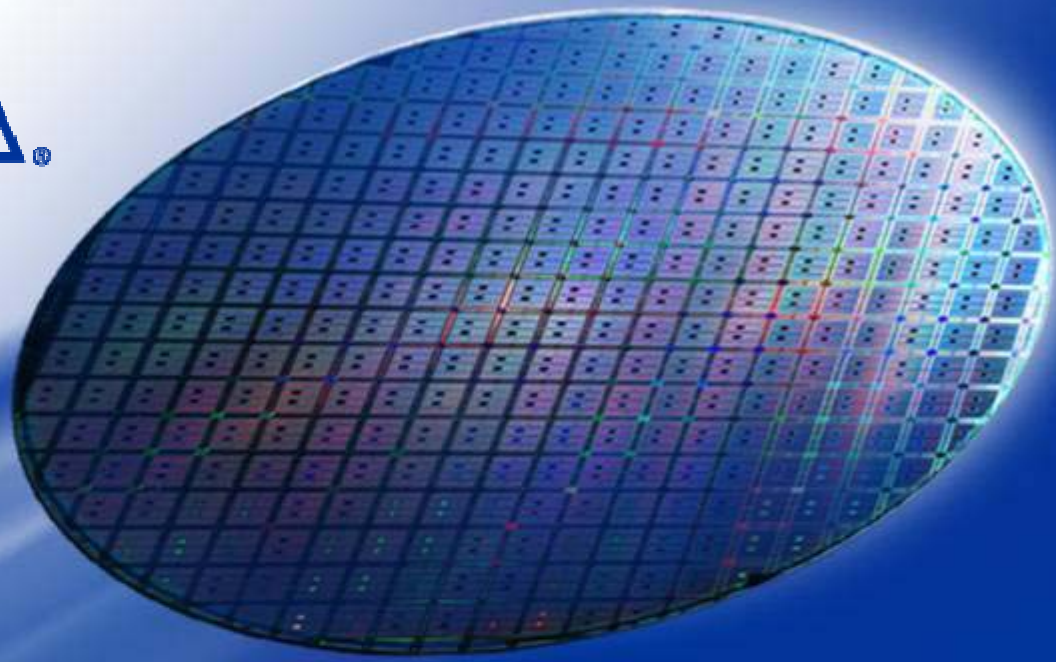
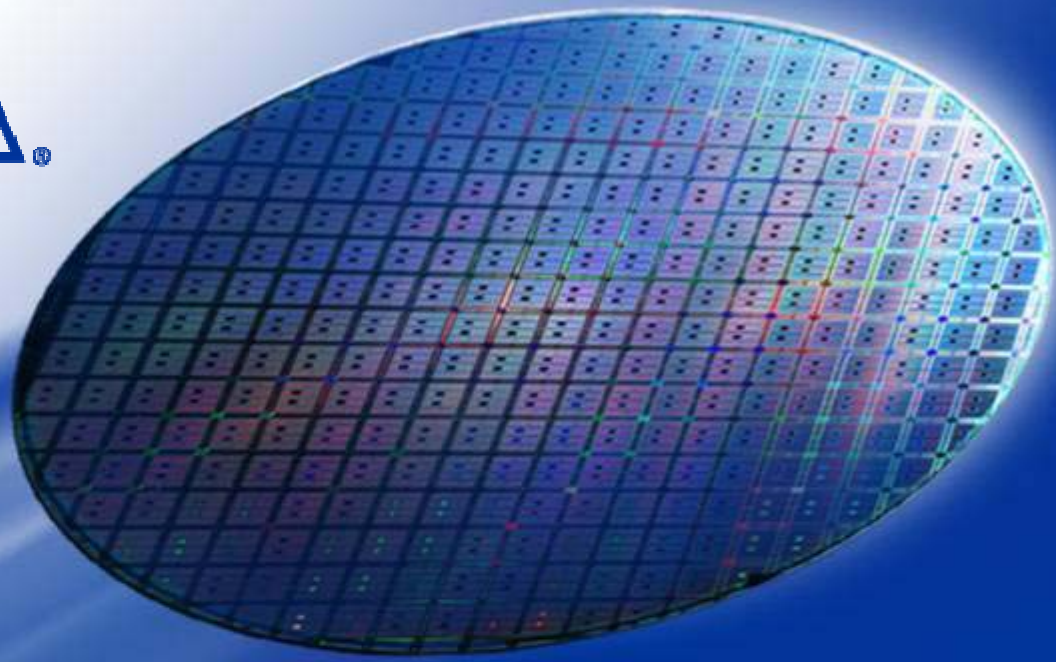


Altera's Roadmap

Looking Forward

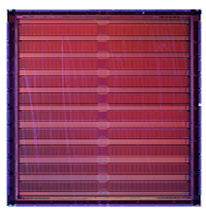
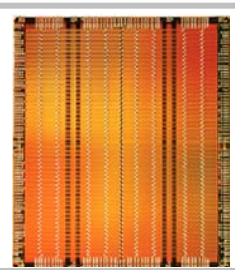
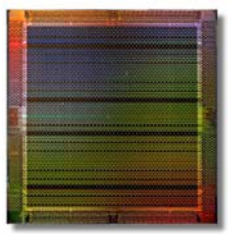
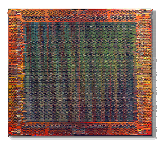
Agenda

- Technology & Process
- Product Roadmap & Challenges
- The Design Environment
- The System Design Decision
- HardCopy® II Structured ASICs



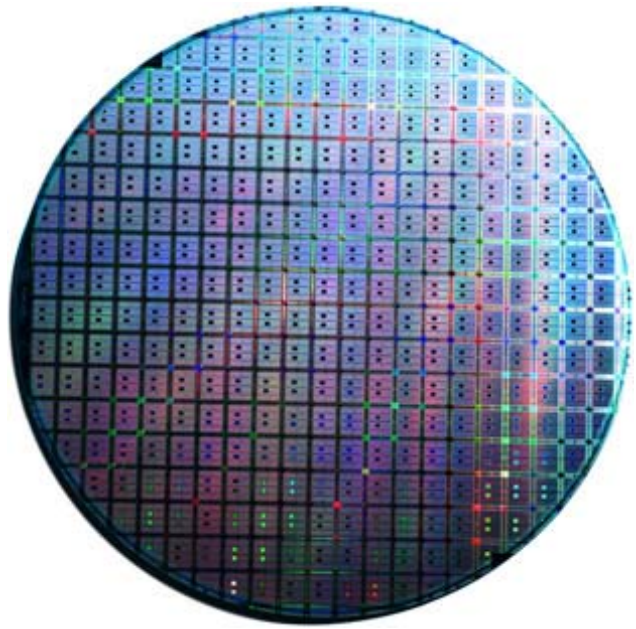
Technology & Process

Technology – Evolution

	EP10K100	EP10K250A	EP20K1500E	EP1S80	EP2S60	*EP2S180*
Introduced	1996	1998	1999	2002	2004	*2005*
Process	0.5 um	0.35 um	0.18 um	0.13 um	90 nm	*90 nm*
Relative Die Size	1	1.09	1.45	1.38	0.55	*1.33*
Transistor Count (Millions)	9	26	110	224	154	*450*
Logic Elements (LEs)	4,992		51,840			*179,400*
RAM Kbits	24	40	432	7,253	2,484	*9,383*
Relative Density	**1**	**3**	**8**	**18**	**31**	***38***
Die Photo						***Feb 2005***

Technology – 0.13um Status

- Now Altera's Mainstream Production Process, Used for:
  - Stratix®, Cyclone™, Stratix GX & HardCopy Stratix Devices
  - Our Highest Revenue Family: Stratix FPGAs
  - Cyclone Volume Ramp Fastest Altera Has Ever Seen
- Over 5M 0.13-um Devices Shipped to Date
- Running Large Volumes at 3 TSMC Fabs
- Most Products Now Running on 300-mm Wafers
  - Better Yields Compared to 200-mm Wafers

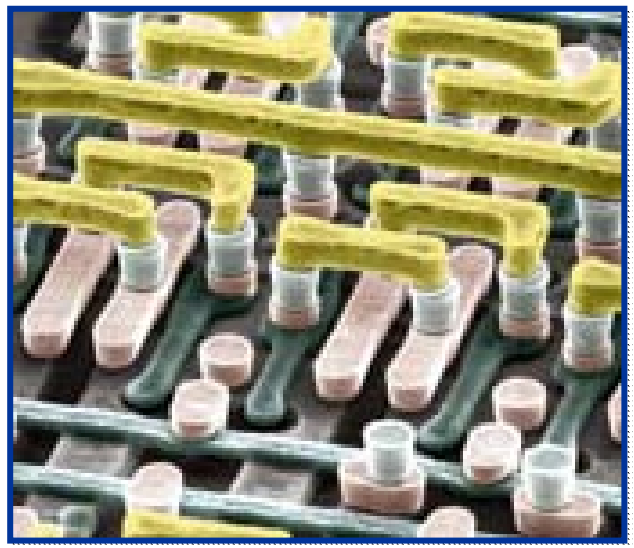


Stratix 300-mm EP1S25

Technology – The Near Term

90 nm

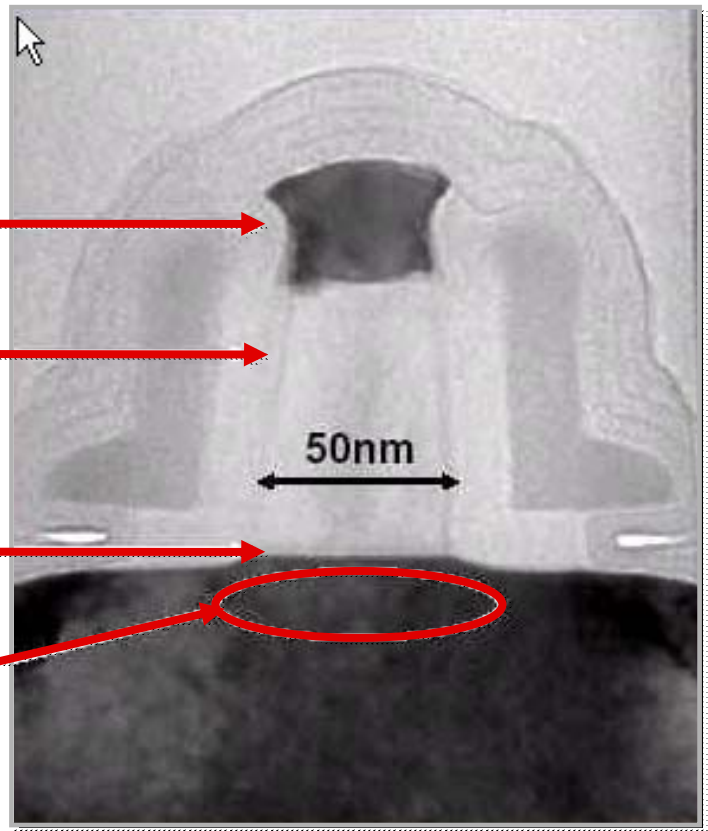
- Stable & Qualified
  - Qualification Completed in July 2003
- Uses Low-k (Black Diamond from Applied Materials), Giving Higher Performance
- Running Entirely on 300-mm Wafers
- Yield Is Higher than Expected
- *Stratix II EP2S60 FPGA Now Shipping—4 More Stratix II Devices in the Fab Today*



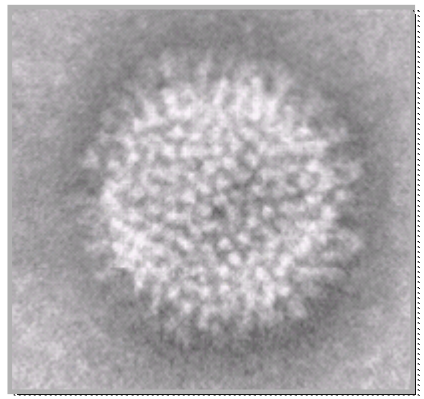
Issues We've Solved Along the Way

- **Power—**Static Consumption Is Higher than Previous Generations
- **Complexity—**Largest Stratix II Device (EP2S180) Will Contain 450M Transistors
- **Layout—**Transistor Layout (even Transistor Orientation) Affects Drive Characteristics Due to Interaction with Silicon Lattice
- **Crosstalk—**Major Design Issue Caused by Parasitic Coupling Between Metal Lines; Low-k Dielectric Helps

Technology – 90-nm Transistors



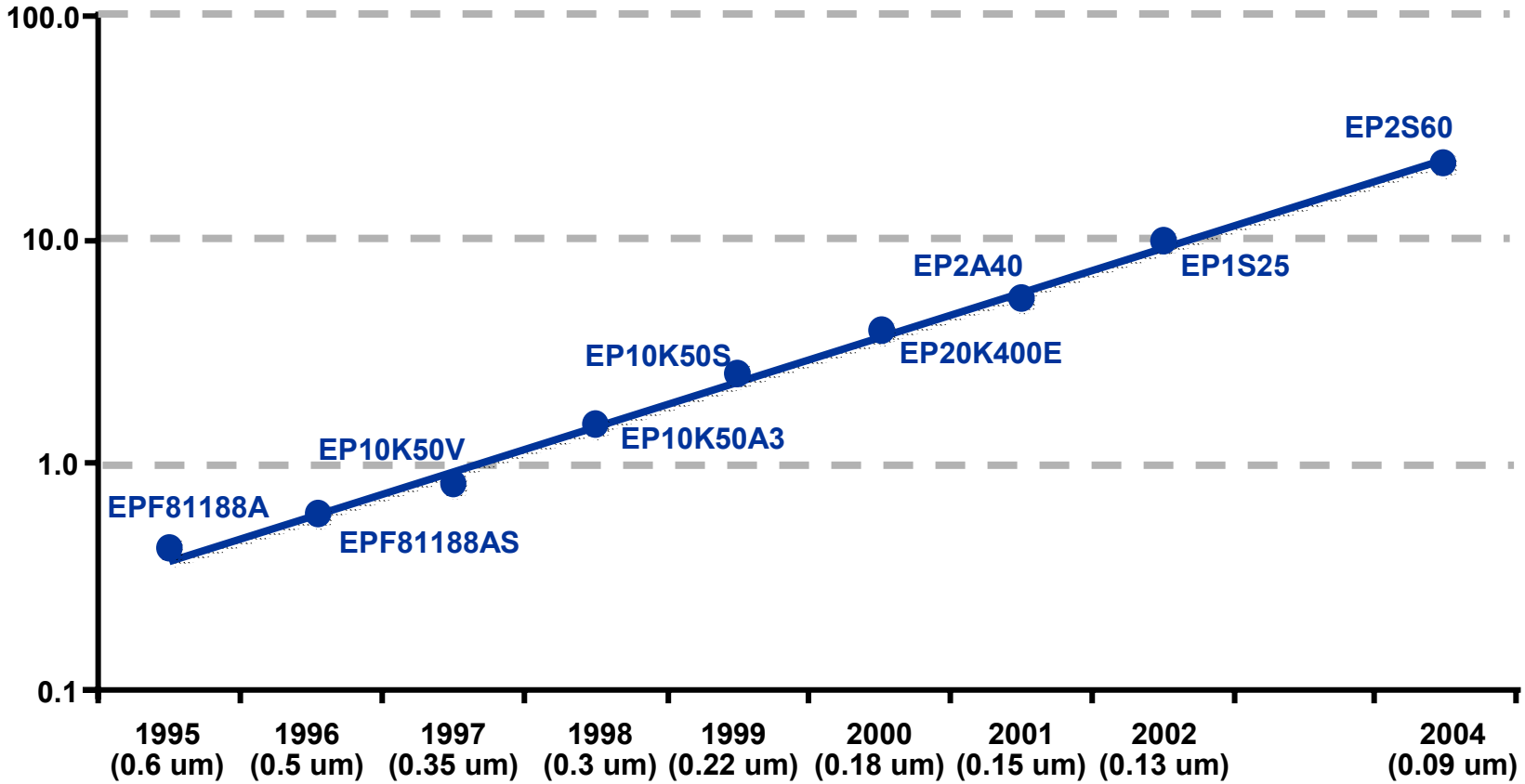
1/2000 Width Human Hair



Flu Virus

Technology – Process Scaling

Number of Transistors (in Billions) per 200-mm Wafer Has Been Doubling Every 19 Months over the Last 8 Years



Technology – The Longer Term

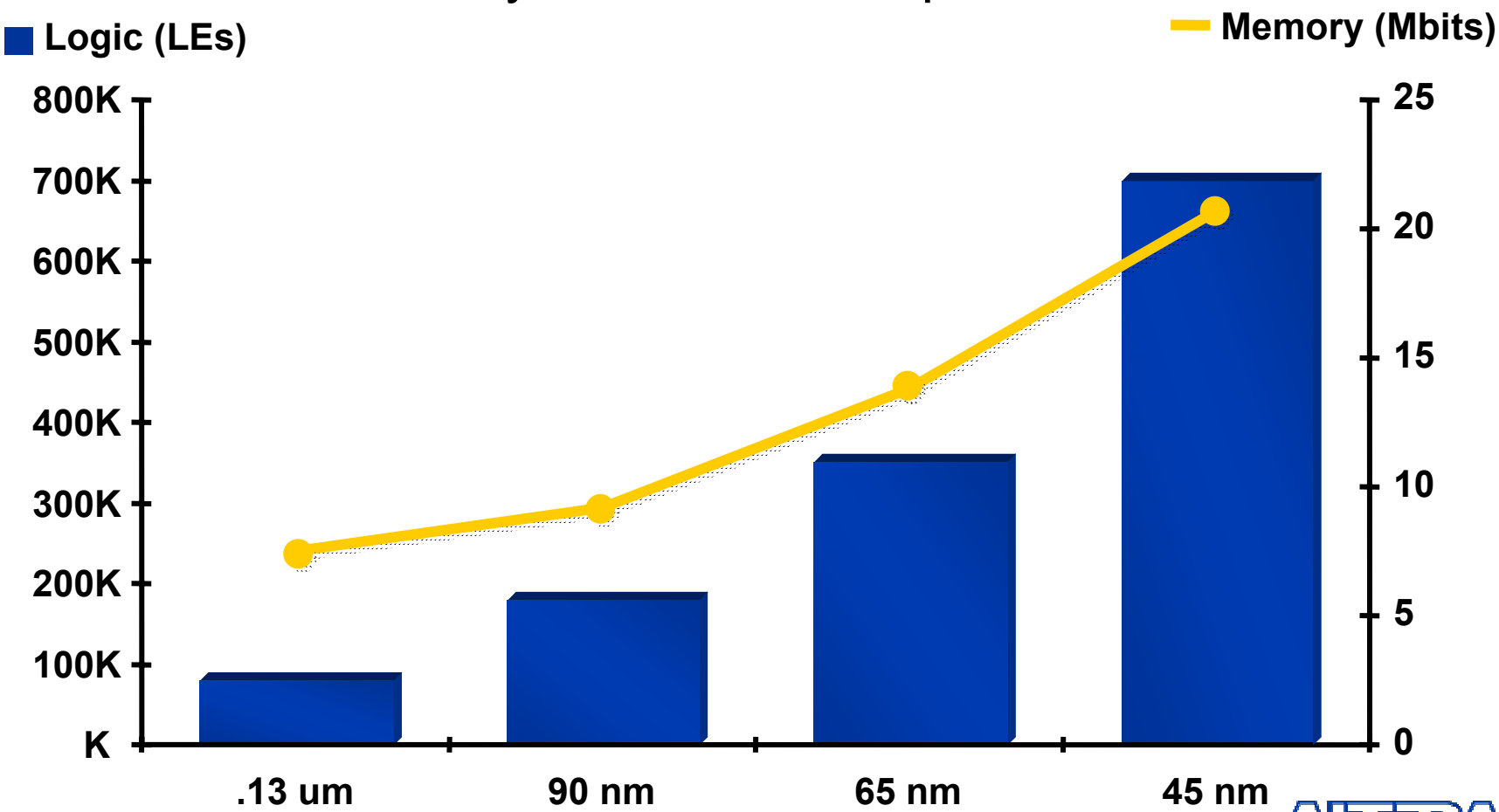
- The Road to 65 nm
  - Started the 65 nm Project One Year Ago
  - First Test Chip to Test Transistor Structures Already Received, Second Chip Running in the Line
  - Timescale: First Product Tape-Out in 2006
  - Major Challenge of this Generation Is Expected to Be Power Management
    - Multiple Approaches Will Be Used to Overcome Power Management Challenge

What Products Can We Create With This Technology?

Product Roadmap & Challenges

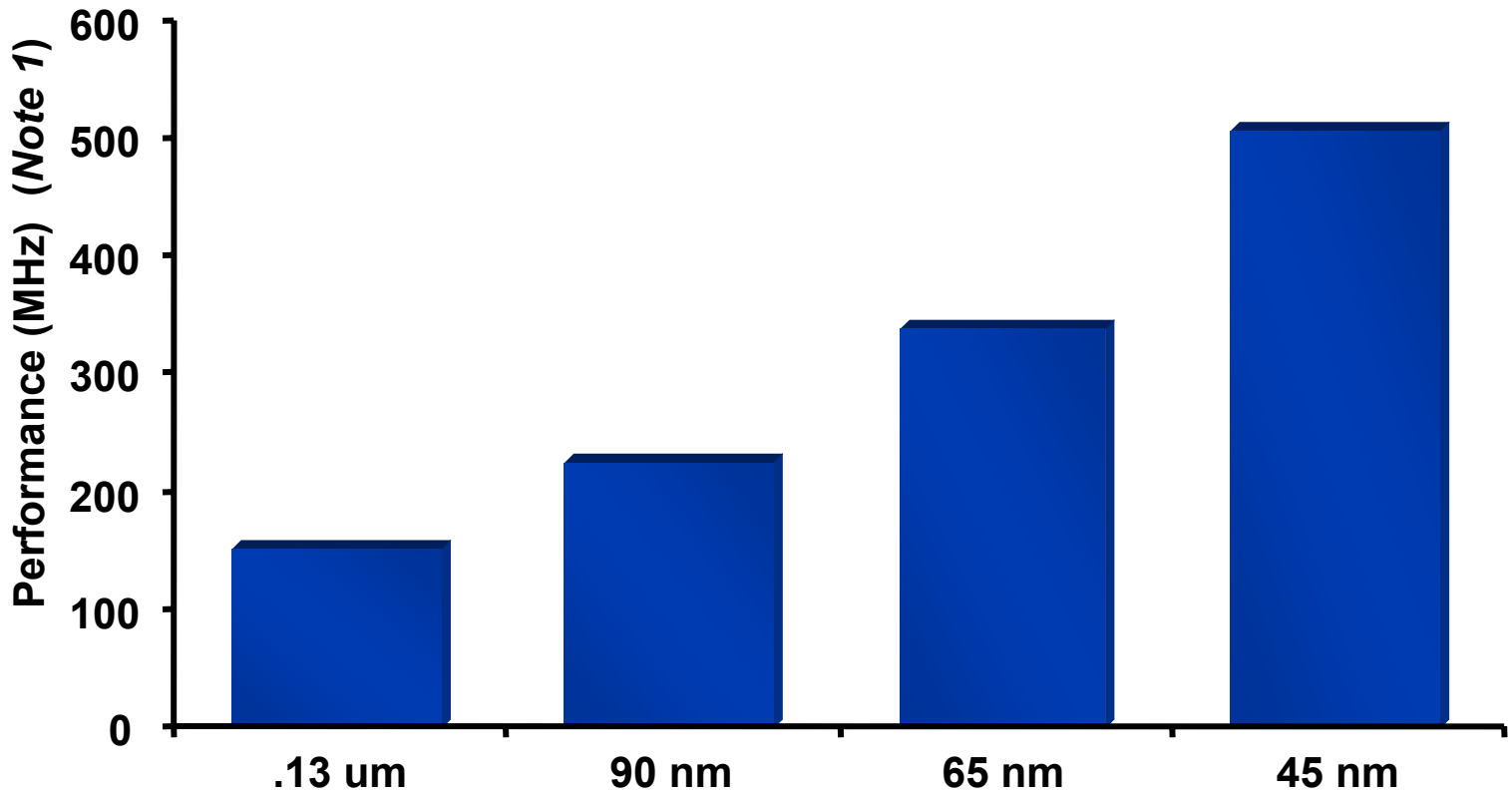
Logic Roadmap

- Logic: 100% Increase per Node
- Memory: 50% Increase per Node



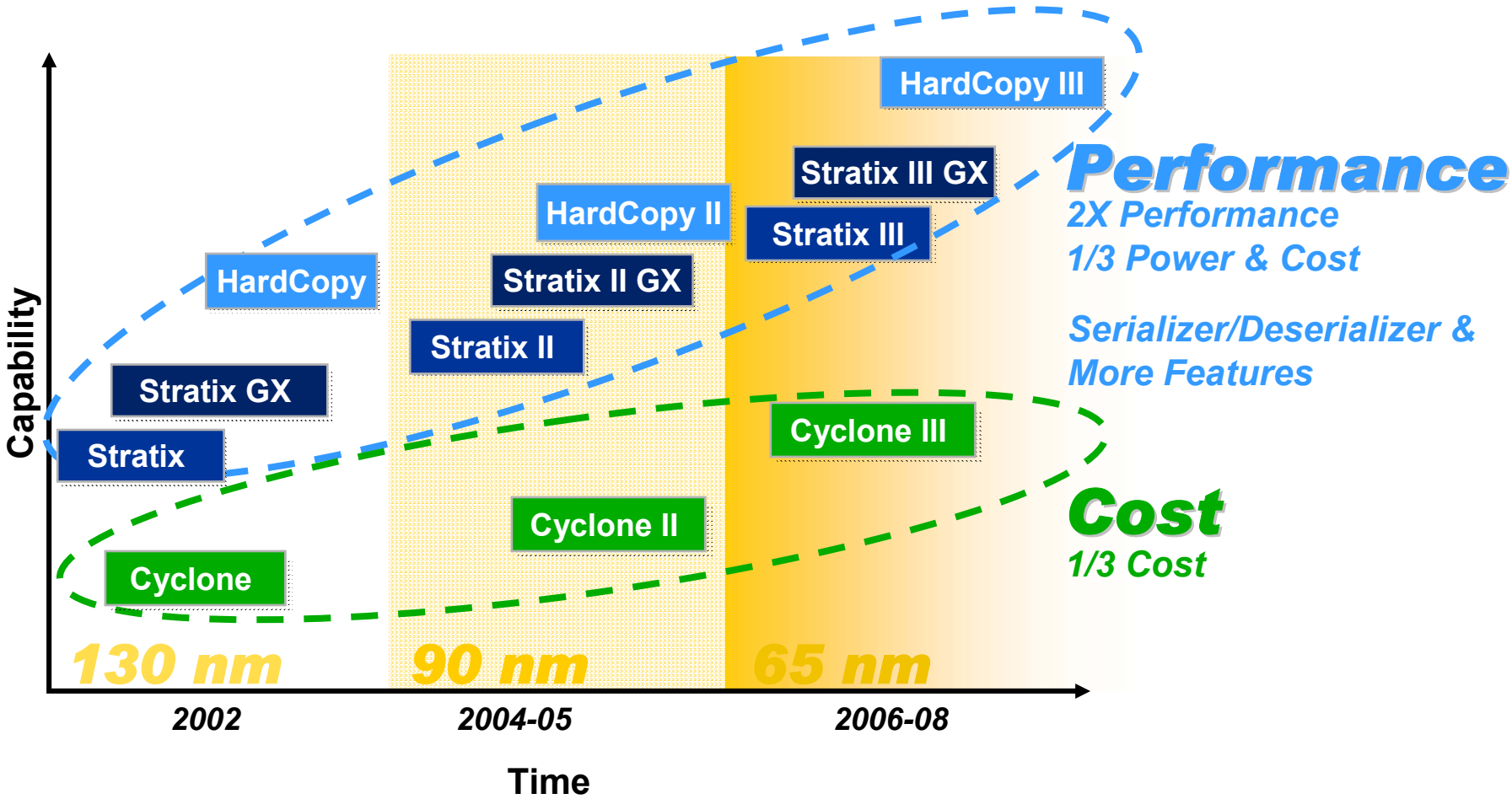
Performance Roadmap

- Technology Supports 50% f_{MAX} Increase per Node
- Actual Performance Implemented Dependent on Customer Demand & Power Requirements



Note 1: Performance Based on Nios® II uP Benchmark

Technology/Product Roadmap



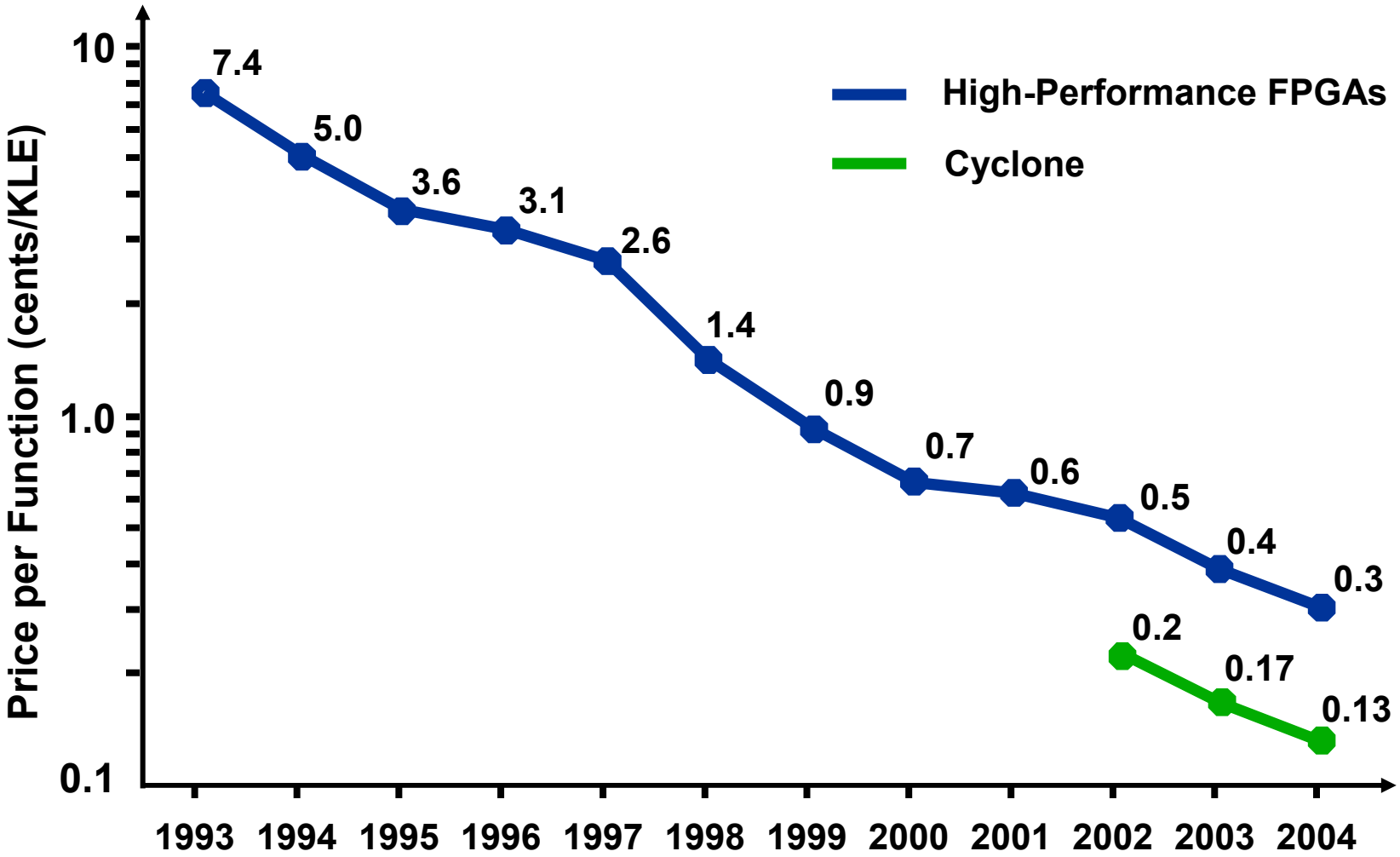
Cyclone Series – Cost & Power

- Cyclone: Fastest FPGA Unit Growth Ever
  - 0 to 4 Million Units in 6 Quarters
- Cyclone II: Lowest-Cost FPGA Series Ever
  - 30% Reduction in Cost per LE per Year
  - 70K LEs for under $100
- Cyclone III FPGAs
  - Will Continue Logic & Cost Gains on Current Ramp
  - Continuing Focus on Total Solution Cost
    - Targeting Less than 6W Power Consumption for Largest Device

Stratix Series – Density & Performance

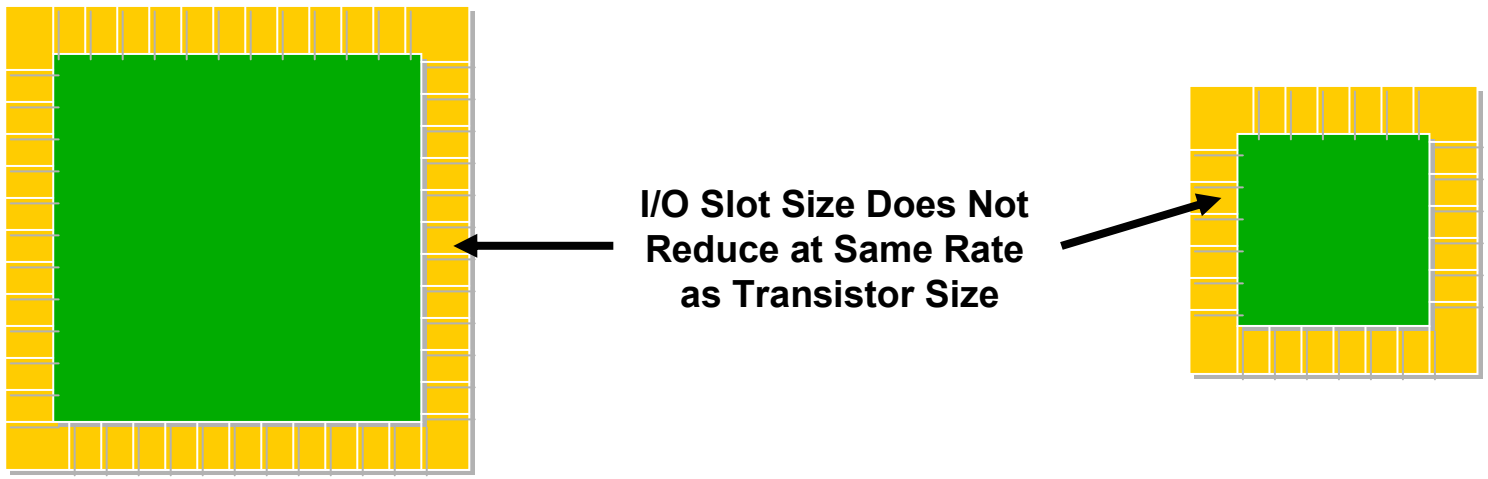
- Performance Increase of 50% per Generation
  - 5X System Performance in 5 Years
- Logic Density
  - Out-Pacing Moore's Law
  - Architectural Innovation—Introduction of Adaptive Logic Module (ALM)
  - Synthesis Efficiency Continuing to Improve
- Stratix III FPGAs
  - Will Continue Performance & Density Gains
  - Additional High-End Features Planned
  - Interconnect Innovation On- & Off-Chip
    - Supports Density Increases, Allows Utilization of Performance

FPGA Products



I/O Evolution

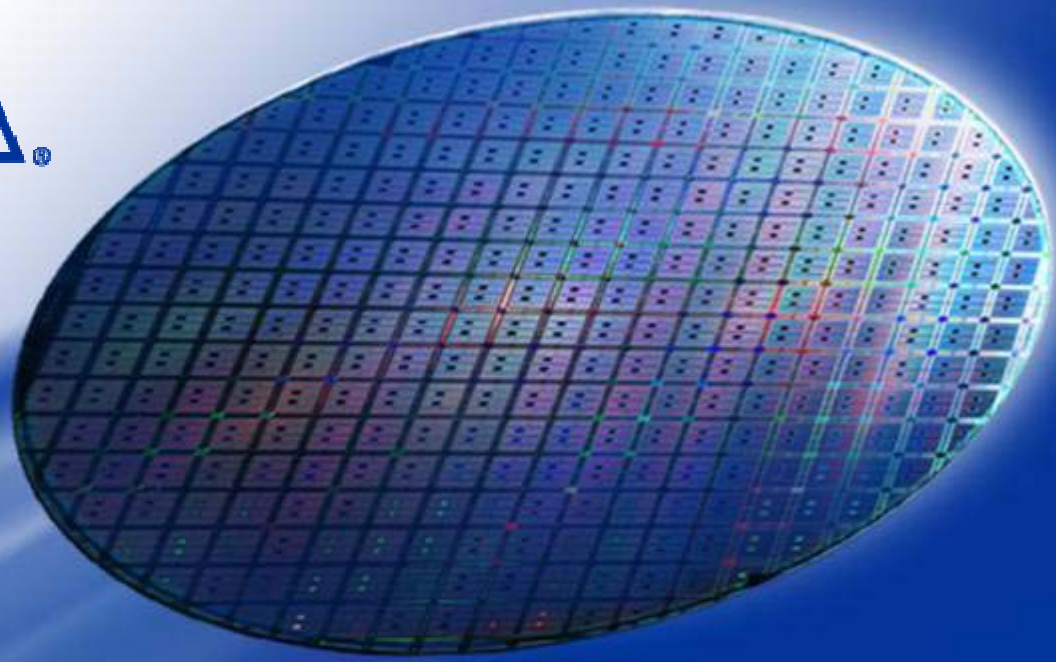
- Beyond 1 GHz, Source-Synchronous I/O Capability Is Not Practical
  - Move to Clock Data Recovery (CDR) for All Speeds Greater than This
- Gate Density Scales Quadratically, While I/O Circuitry Does Not



  - Leads to an Increasing Problem with Pad-Limitation Over Time
  - Result: More HSSI Usage to Minimize I/O Counts
- Today: 3.125-Gbps I/O Capability Only on High-End PLD Families
- Tomorrow: Multi-Gbps I/O Capability on All FPGAs

MAX Series

- MAX Market Share: 45%
  - The Market Likes the Balance of I/O Circuitry, Cost & Features
- MAX II Moves the Goalposts
  - Cost Down 75%
  - Feature Innovation
- MAX III CPLDs
  - Intent: Solve Additional Board Management Issues
  - Adjust Density, Power & Cost According to Market Requirements

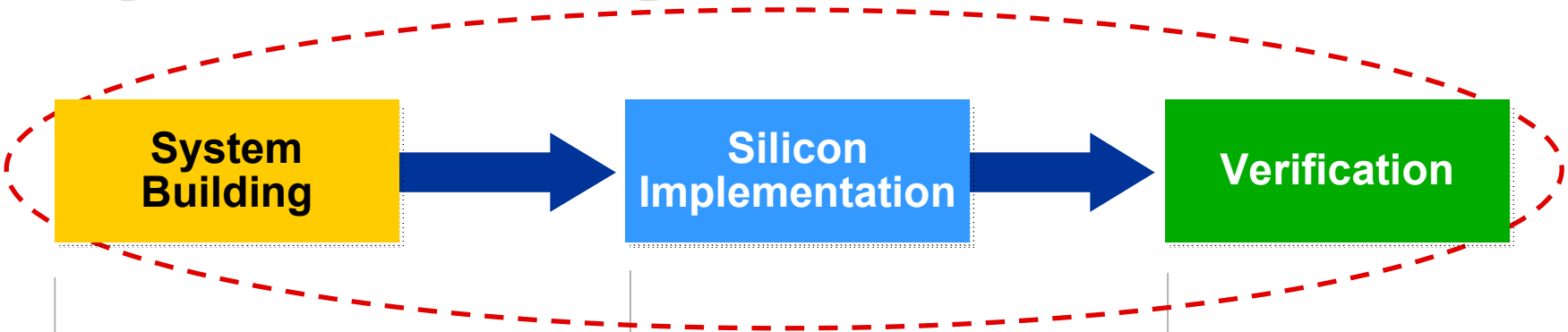


The Design Environment

Altera Software Investment

- Four R&D Teams Worldwide
  - Nearly Half of Altera's Design Engineers Work in Software
- Over 100 Patent Disclosures over Past 2 Years
- Software R&D Is Integral to Silicon R&D Process

System Design

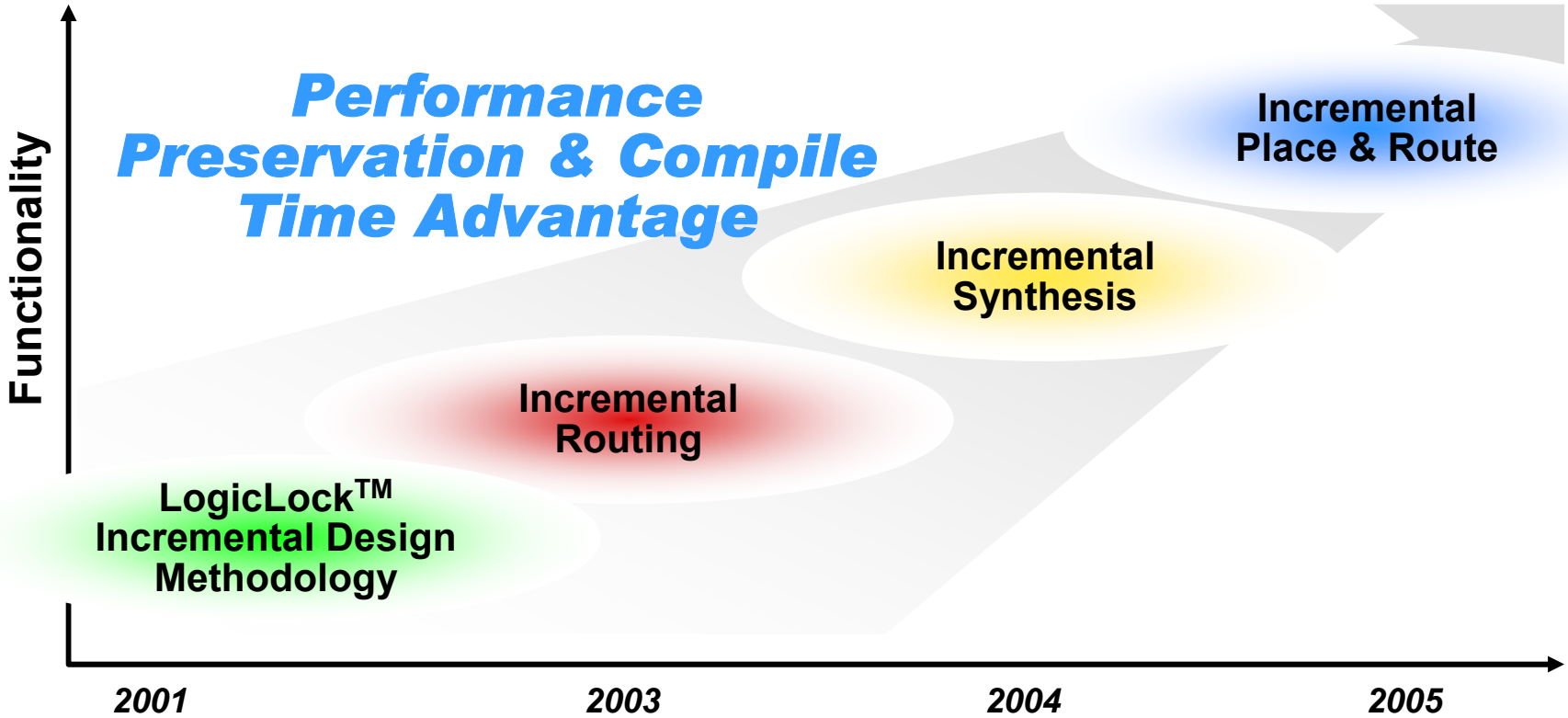


- DSP Builder
- SOPC Builder
- High Level Synthesis
- I/O Assignments & Board Design
  - Creation of Assignments
  - Constraint Passing
  - SSN Modeling & Checking

- Synthesis
  - Architecture-Specific Synthesis
  - Physical Synthesis
- Place & Route
  - QoR
  - Performance Preservation & Compile Times
    - Incremental Design
    - ECO Support
- Power
  - Estimation
  - Design

- System Debug
  - Source Level Debug
  - HW/SW Debug (SW Triggers HW & Vice-Versa)
  - Interactive Stimulus
  - SW Profilers
  - Custom Analyzers (Protocol Analysis, etc.)
- Timing Analysis
- Simulation
- Formal Verification

Incremental Compilation Roadmap



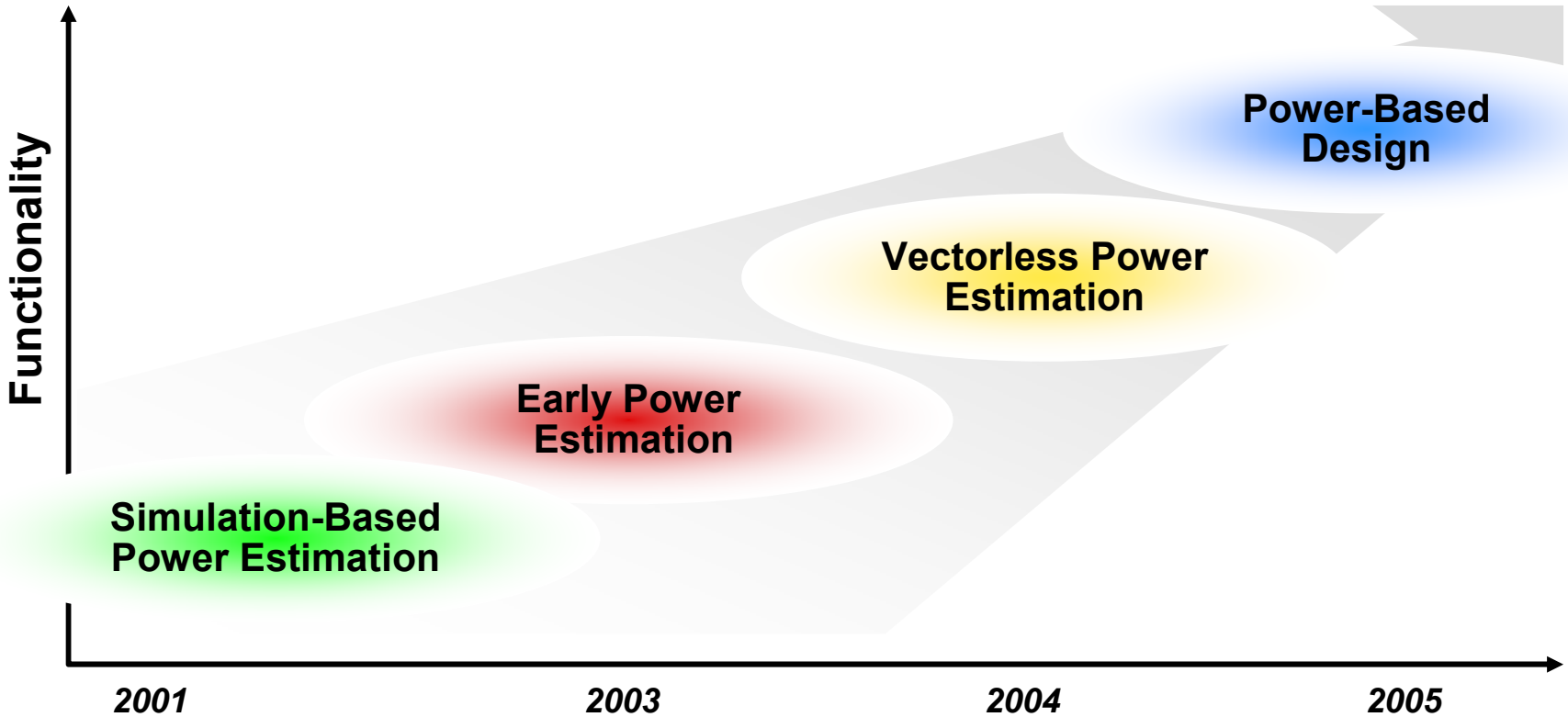
- Block-Based Design
- Performance Preservation

- SignalProbe™ Feature
  - Route Internal Signals to Pins
- SignalTap® Logic Analyzer
  - Routing of Monitor Signals

- Only Re-Synthesize Parts of Design that Change
- Compile Time Improvements

- Complete Incremental Design Flow
  - Top-Down
  - Bottom-Up
  - Team-Based

Quartus II Power Roadmap



- Quartus® II Simulator
- Interface to Third-Party EDA Simulation

- Interface to Power Calculator

- Vectorless-Based Estimation
- User Entry of Activity Rate
- VCD Interface for
  - RTL Estimation
  - Timing Simulation
- HSPICE-Based Power Models

- Optimize for Power
  - Synthesis
  - Place & Route

Nios II Processor: Product Roadmap

Nios II v1.0 Service Pack 1
- Cyclone II Support
- Stratix II Development Kit

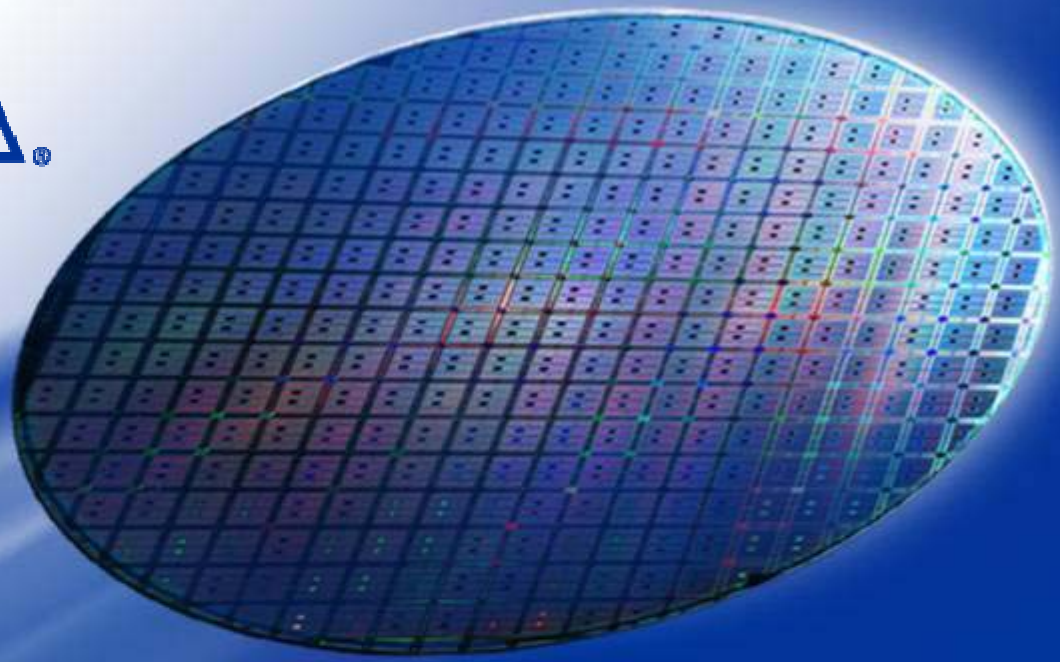
Nios II v1.1
- Linux / Solaris Host Support
- Hardware Multiplier for Cyclone FPGAs
- Nios II Integrated Development Environment (IDE) Enhancements
- Low-Cost Evaluation Kit
- Multi-Clock Domain Support

Nios II v1.1 Service Pack 1

Nios II v2.0
- Memory Management Unit (MMU)
- L2 Cache
- OS Awareness (IDE)
- Mixed Trace Display (IDE)
- Cyclone II Development Kit

30 Years of Trends

	1983	1993	2003	2013
PLD Technology	3 um	0.8 um	0.13 um	32 nm
PLD Maximum Complexity (Macrocells/LEs)	8 Macrocells	1,188 LEs	80,000 LEs	750,000 LEs
Transistor Count	12K	1.5M	230M	1,500M
$20 Buys…	8 Macrocells	128 Macrocells	12K LEs	75K LEs



The System Design Decision

System-Design Options

- ASIC
  - No Longer the Mainstream Option; Up-Front Costs too High
- ASSP
  - Looked Good for Several Years, But Less Attractive Now
    - Economics Issues Same as ASIC
    - No Differentiation from Other Users
- Digital Signal Processors
  - Attractive for Applications Requiring Digital Signal Processing (DSP) Functionality, But Some Issues
    - Power-Hungry & Costly for High Performance
    - Not Highest Performance
    - Increasing Specialization
- Programmable Logic

What Will the Mainstream Choice of the Future Be?

Key Decision Criteria

	PLD	ASIC
Fast Prototyping	✓	✗
Easy Changes Late in the Design	✓	✗
Rapid Evaluation of Changes	✓	✗
Low Design Costs (Low Up-Front Costs)	✓	✗
Low Penalty for Mistakes	✓	✗
Low Production Price	✗	✓
High Performance	✗	✓
Low Power	✗	✓

Consequence of Moore's Law:
FPGA Disadvantages Decrease over time, Advantages Increase
ASIC Disadvantages Increase over Time, Advantages Decrease

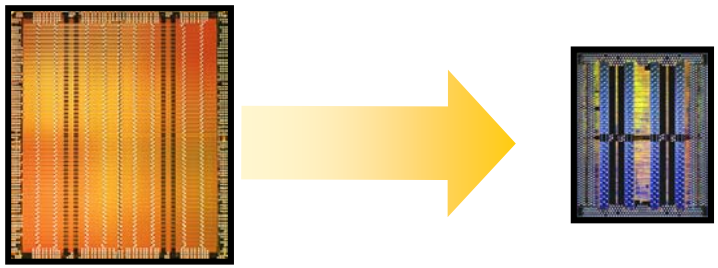
The Best of Both Worlds – Possible?

- Combine Strengths of FPGA…
  - Low Up-Front Costs, Fast Prototyping, Easy Changes, etc.
- …With Strengths of ASIC
  - Low Production Cost, Low Power, High Performance

Yes!
We Call This HardCopy

A Brief History of HardCopy

September 2001



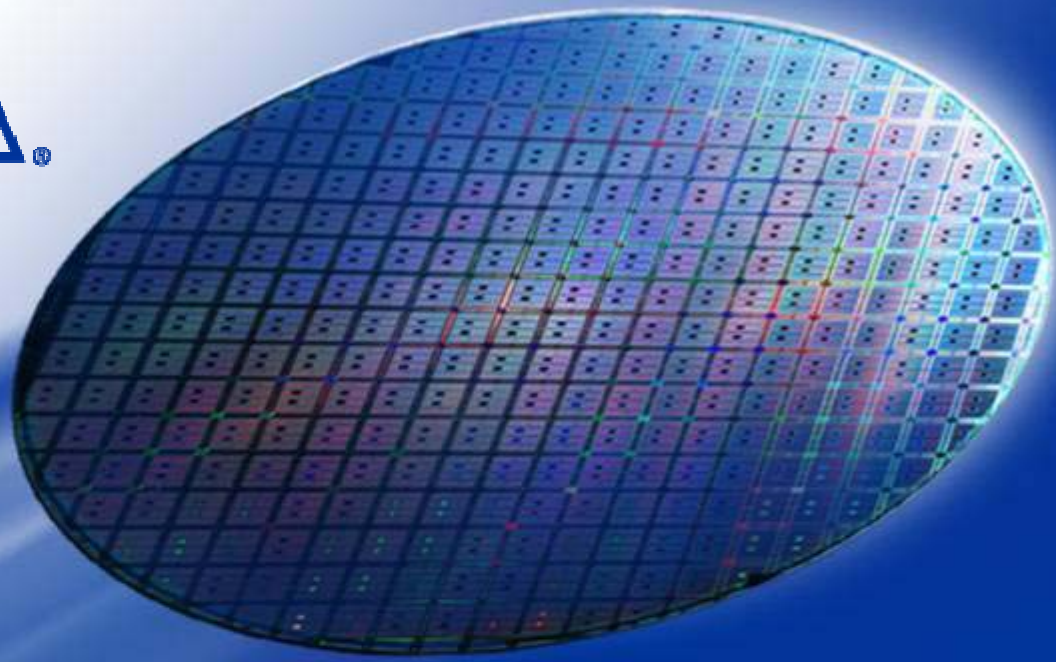
~ 600K Gates @ $100

APEX® 20KE, 0.18µ HardCopy APEX, 0.18µ

December 2003

~ 1.0M Gates @ $100

Stratix, 0.13µ HardCopy Stratix, 0.13µ



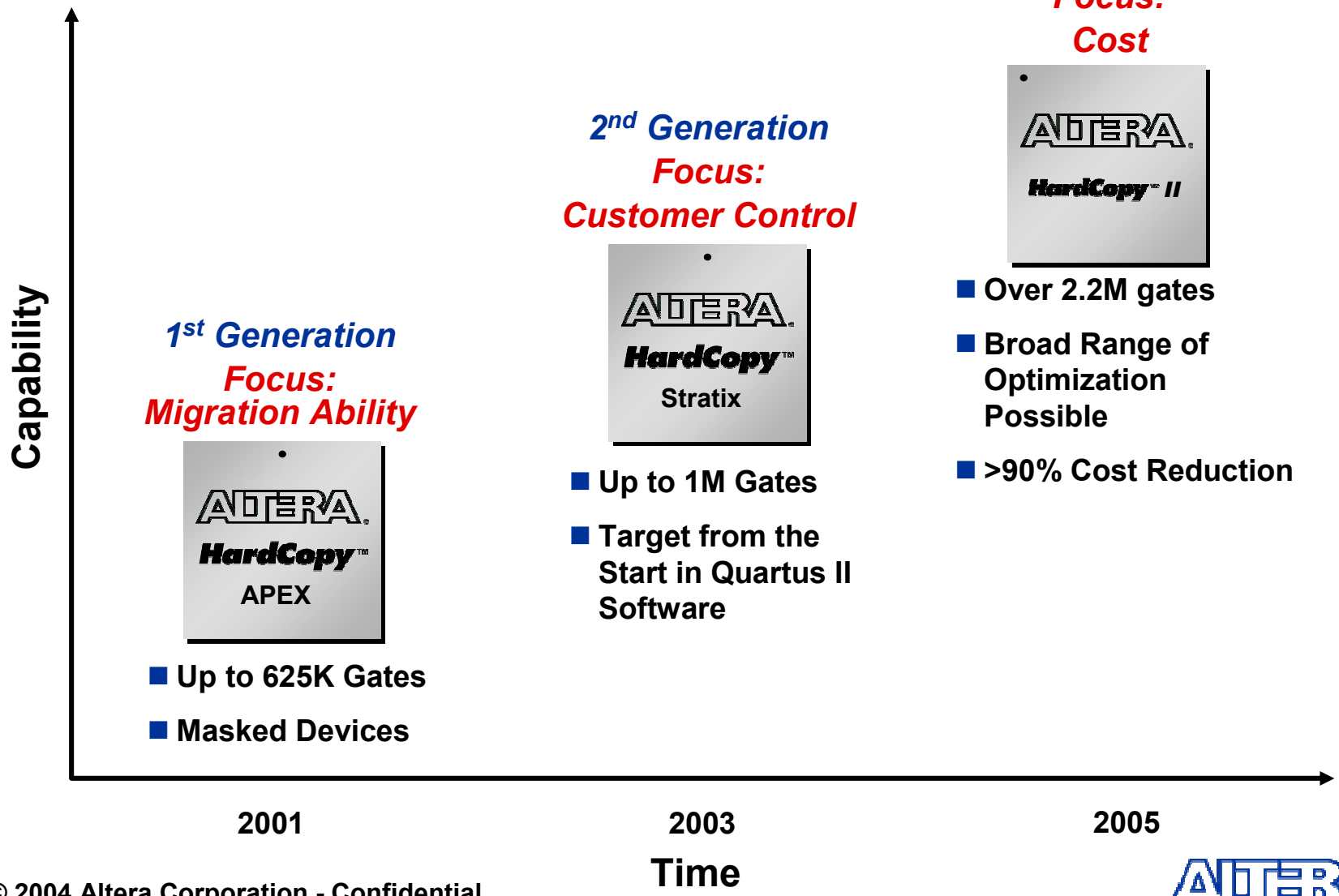
HardCopy II Structured ASICs

HARDCOPY™

HardCopy II Goals

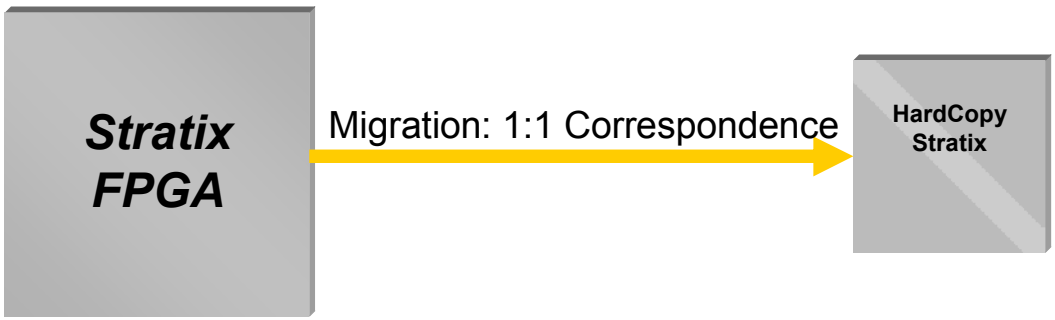
- Keep HardCopy Advantages
  - No Changes to Critical Stratix II Blocks [I/Os, Phase-Locked Loops (PLLs)]
  - In-System Hardware Development with Stratix II FPGAs
  - Flexible Customer Design Flow
  - Altera Conversion Process
- Reach Parity with Structured ASICs
  - Same Cost per Gate
  - High Gate Density
  - High Performance
  - Low Power

HardCopy Evolution



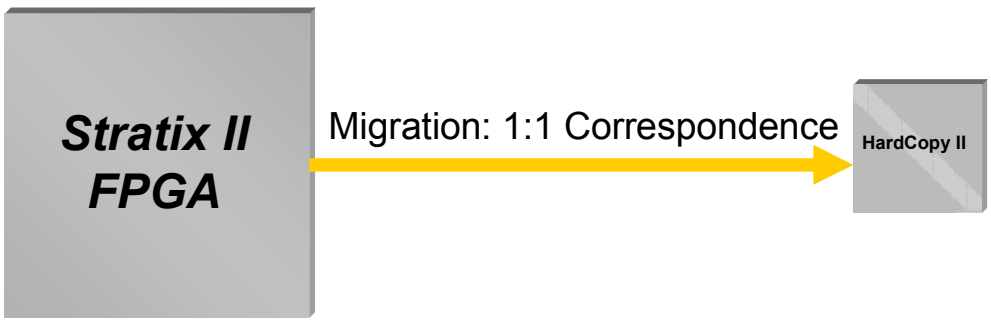
Migration & Prototyping

HardCopy—Stratix Generation



~70% Die-Size Reduction
No PCB Changes Needed
Cost Reduction Constrained by Retention of All Resources

HardCopy II—Stratix II Generation



> 90% Die-Size Reduction Possible
Still No PCB Changes Required
Resource Trade-Off for Better Cost Reduction

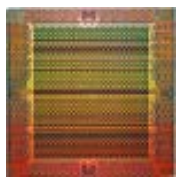
- HardCopy Stratix—1M Gates Possible Only in 1,020-Pin FineLine BGA® Package
- HardCopy II—1M Gates in Packages from 484- to 1,508-Pin FineLine BGA Packages

Stratix II Example – EP2S90

EP2S90

	Logic (LEs)	91K LE Gates
	Memory	4.5Mb
	18x18s	192
	PLLs	6/12
F484*	I/O Pins	~ 341
F780	I/O Pins	~ 540
F1020	I/O Pins	741

* 27x27mm Body



92%

Logic (gates)	1.0M
Memory	0.88M
PLLs	4
I/O Pins	334

HC210-F484

83%

Logic (gates)	1.6M
Memory	3.03Mb
PLLs	6
I/O Pins	494

HC220-F780

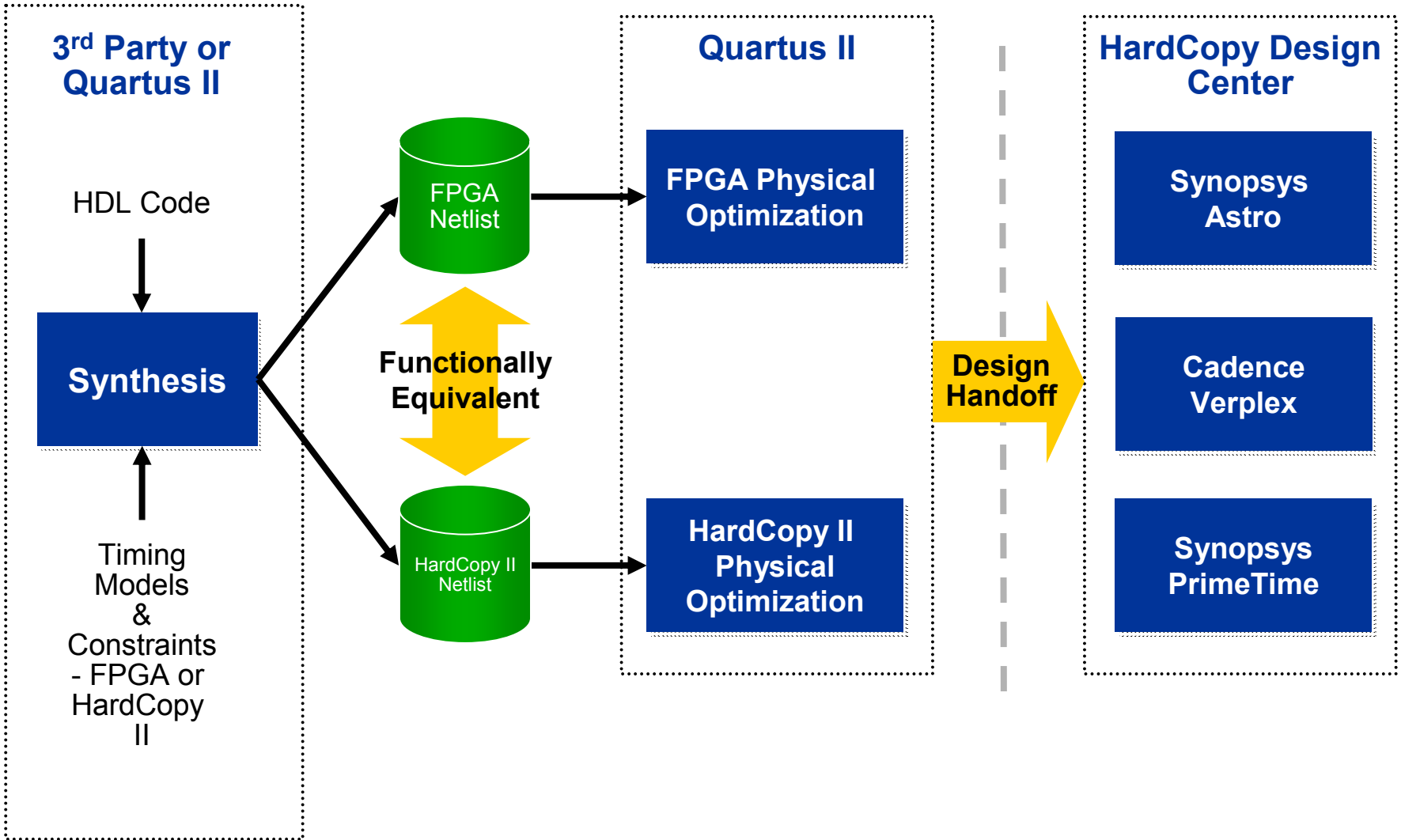
61%

Logic (gates)	2.2M
Memory	6.26M
PLLs	8
I/O Pins	698

HC230-F1020

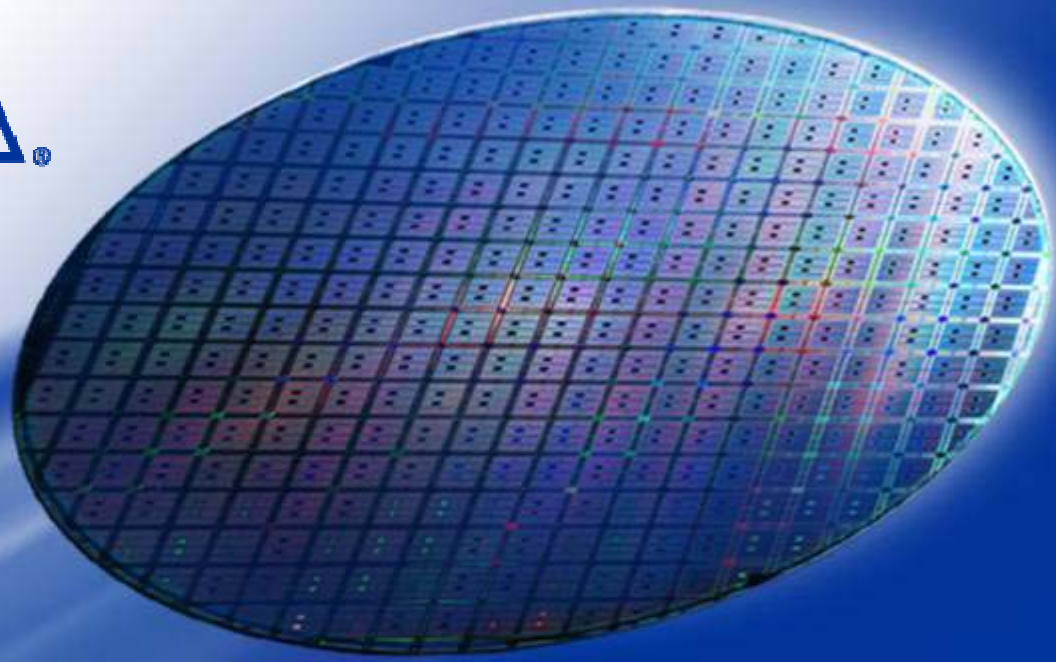
Note: % Represents Die Size Reduction

FPGA & HardCopy II Design Flow



Summary

- Market Changing Due to Semiconductor Economics
  - Process Technology Will Challenge New Chip Decisions
- Programmable Logic Is One of the Few Products Where the Economics Work
  - Expected to Grow at Twice the Rate of the Semiconductor Market
- Some Applications Need Lowest-Cost & Highest Density on Introduction
  - HardCopy II Structured ASICs Allow the Combination of S-ASIC & FPGA Prototyping



Thank You !