

Mentor Graphics Solutions Enable Fast, Efficient Designs for Altera's FPGAs

Fall 2004

**Mentor
Graphics®**

Agenda

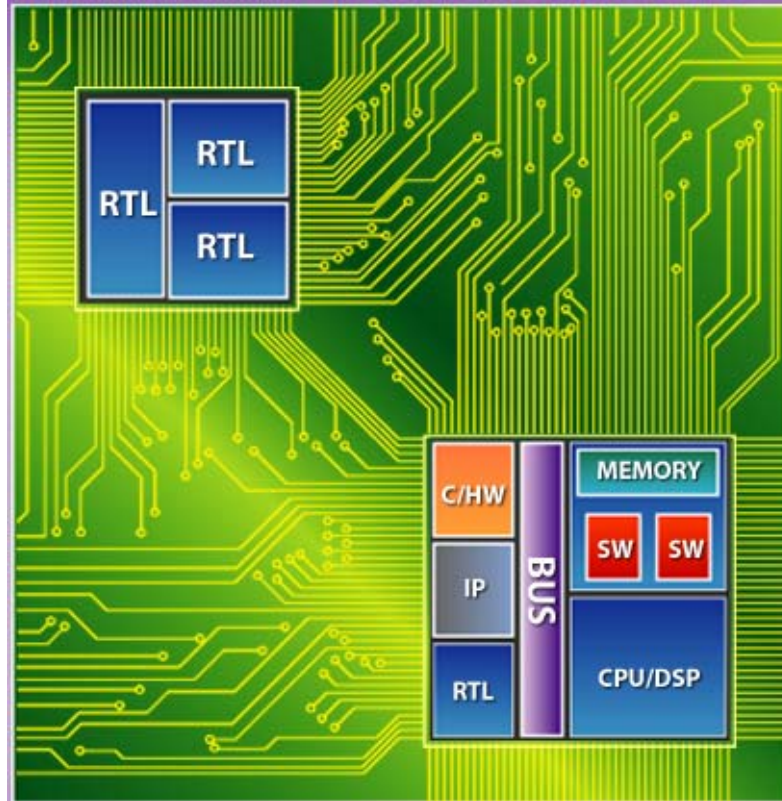
- FPGA design challenges
- Mentor Graphics comprehensive FPGA design solutions
- Unique tools address the full range of complex device- and system-level challenges
 - HDL Designer Series
 - ModelSim
 - Precision Synthesis
 - I/O Designer

Complex FPGA Systems Demand New Design Approaches

Mainstream / Ready-to-use FPGA/PLDs

- Synthesize
- Place & Route
- Simulate/Debug

Low-cost tools
Push-button flow



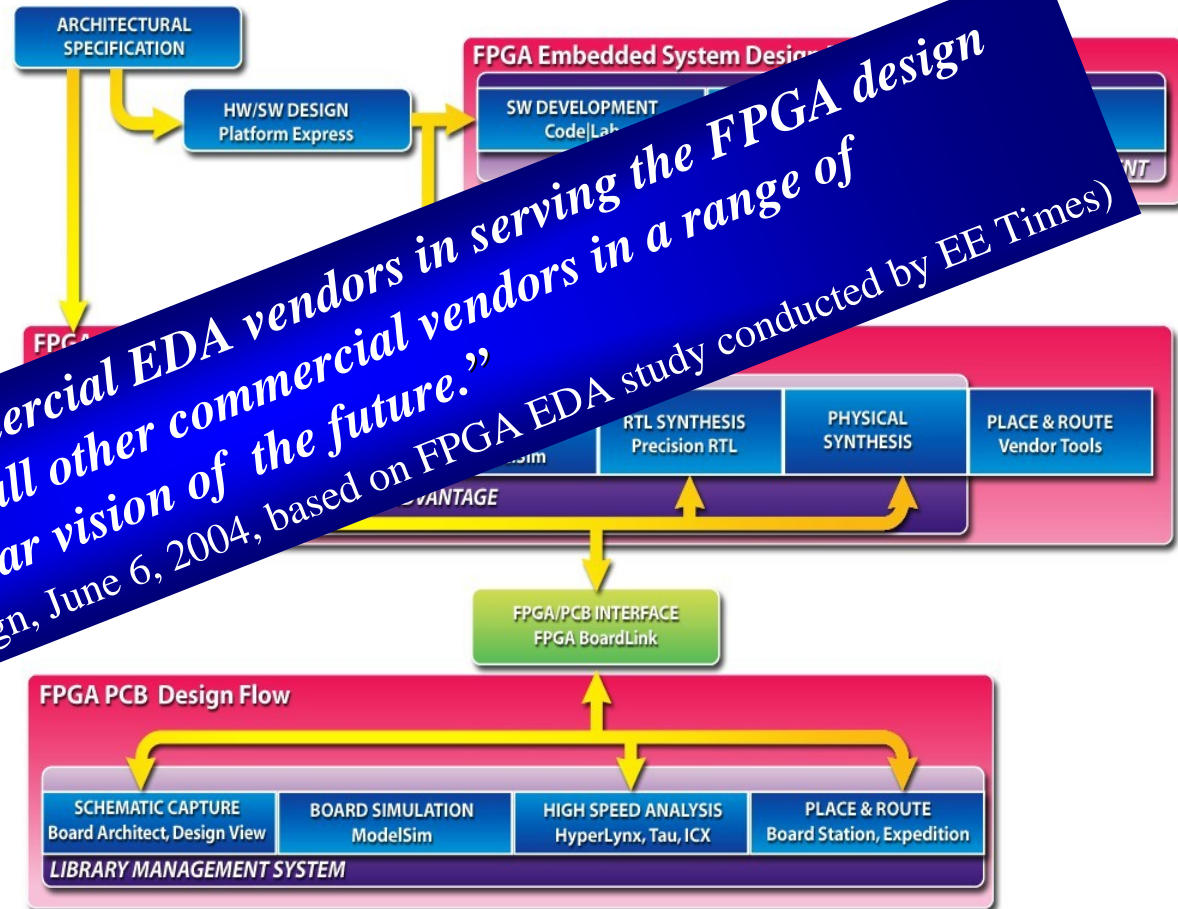
High-end FPGA/FPSoC

- Complex timing
- Physical timing problems
- IP integration
- HW/SW design
- Complex debug
- Prototyping
- SDC constraints
- C-based design
- PCB integration issues
- Team design

Sophisticated tools
ASIC-like flow

Mentor Graphics FPGA Design Flow

- Most comprehensive in the industry
- Incorporates complex FPGA design aspects
 - Embedded systems
 - RTL simulation and synthesis including incremental design



“Mentor Graphics led commercial EDA vendors in serving the FPGA design community. They beat out all other commercial vendors in a range of categories, including a clear vision of the future.”
 (EEDesign, June 6, 2004, based on FPGA EDA study conducted by EE Times)

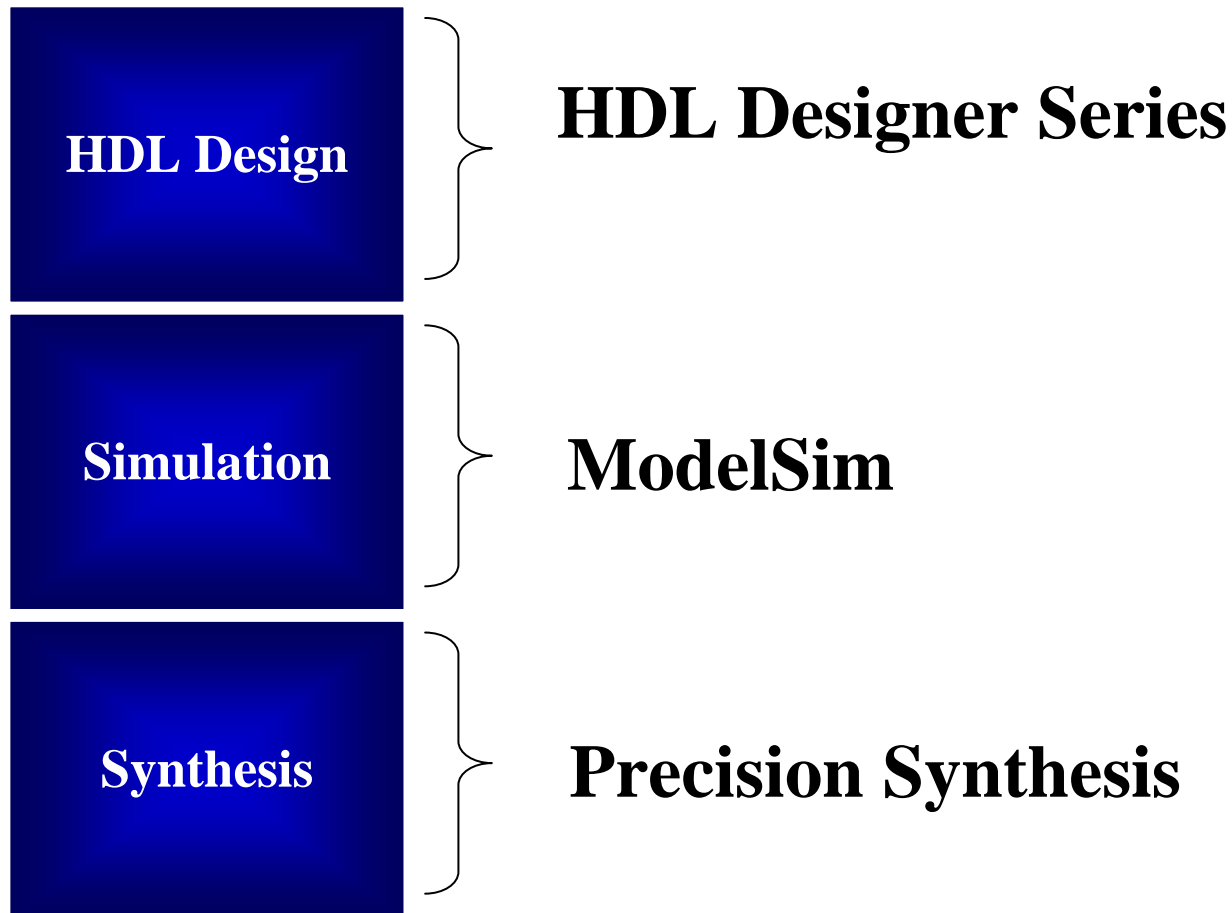
Mentor HDL Flow.psd Rev09.03

Some Mentor Graphics FPGA Design Product Names

- **FPGA Advantage®**
 - Complete FPGA design environment
- **HDL Designer Series™**
 - Design creation, reuse, management, documentation, and design flow control environment
- **ModelSim®**
 - HDL simulation
- **Precision® Synthesis**
 - RTL synthesis
 - Physical synthesis
- **Catapult™ C Synthesis**
 - Algorithmic, untimed C/C++ synthesis for FPGA/ASIC
- **LeonardoSpectrum™**
 - FPGA and ASIC synthesis
- **Seamless™**
 - Hardware/Software co-verification environment
- **XRAY® Debugger**
 - Software debug for embedded processors
- **Inventra™ IP**
 - IP cores for faster, reliable time to market
- **Nucleus™**
 - RTOS family of embedded software
- **HyperLynx®**
 - SI and EMC analysis suite
- **I/O Designer™**
 - Integrated systems design, enabling concurrent FPGA-on-board design

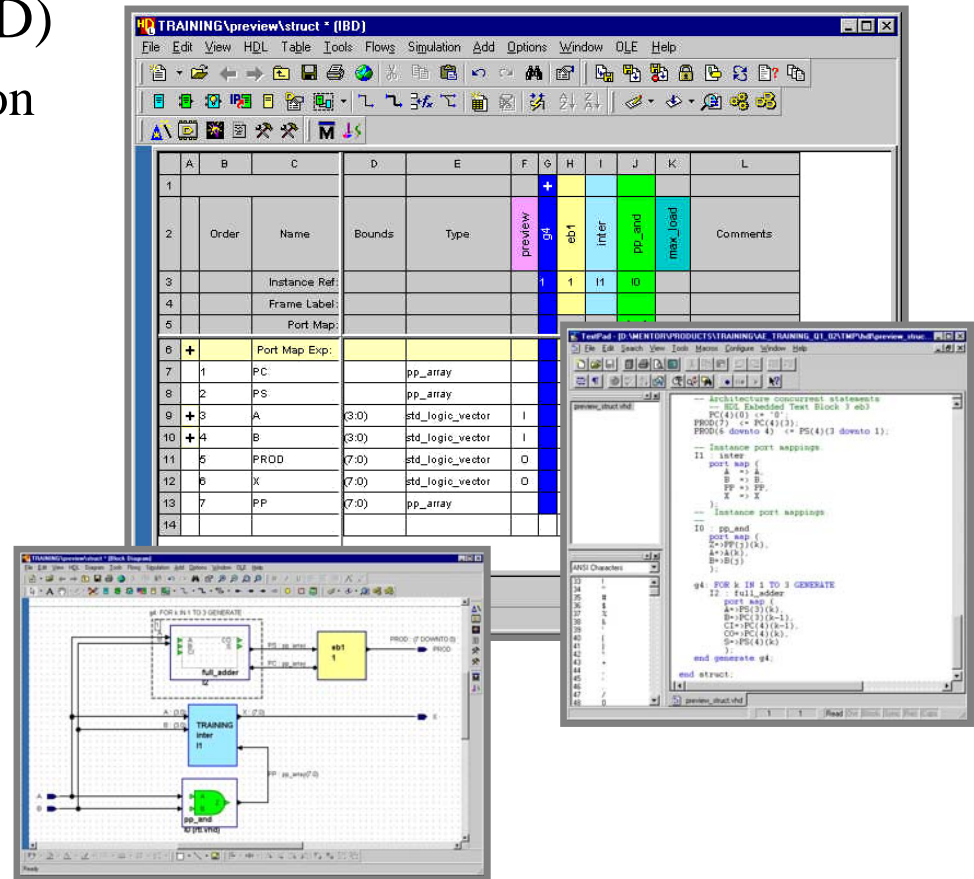
FPGA Advantage

The FPGA Design Flow



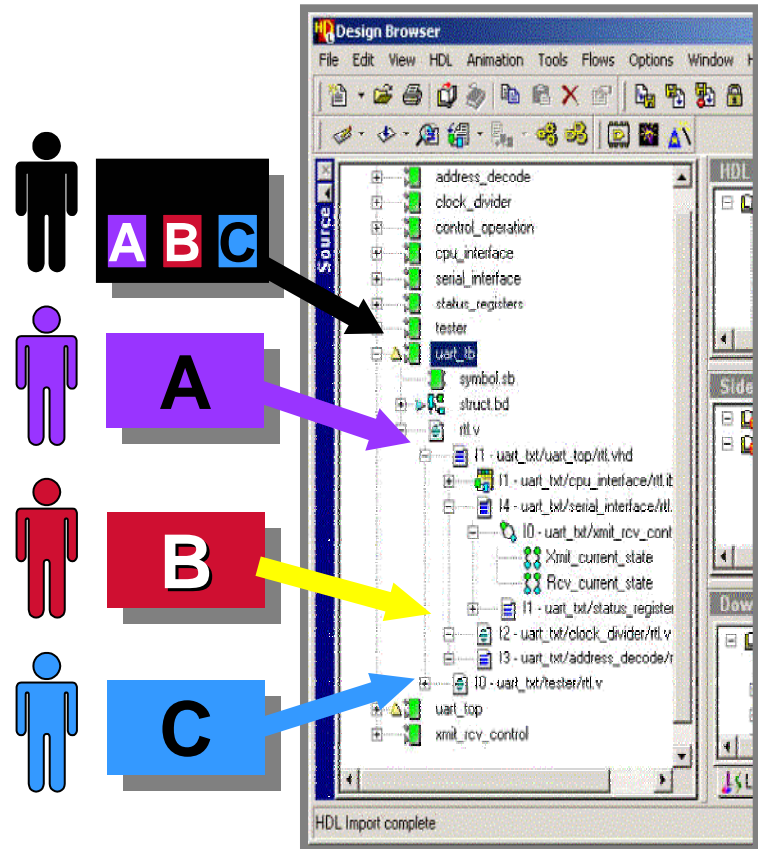
HDL Designer Series: Design Creation

- Interface-based design (IBD)
 - Structural design definition
 - Synthesis properties specified for flow
 - Aids documentation
- Block diagram
- Text entry
- State machine
- Flow chart
- Truth table
- ModuleWare



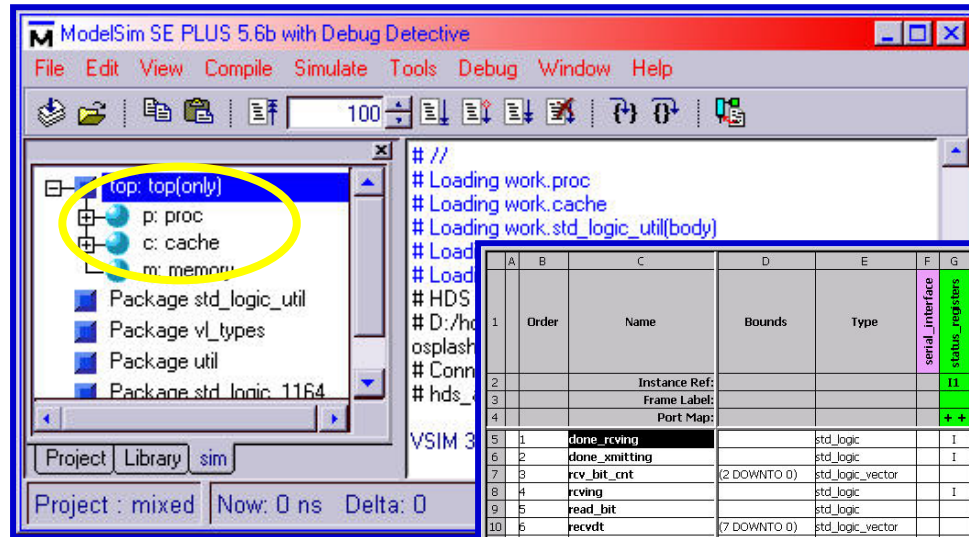
HDL Designer Series: Team Design Environment

- FPGA design teams
 - 1, 5, 10+ engineers
 - Blocks designed separately but in context of entire design
 - Version control



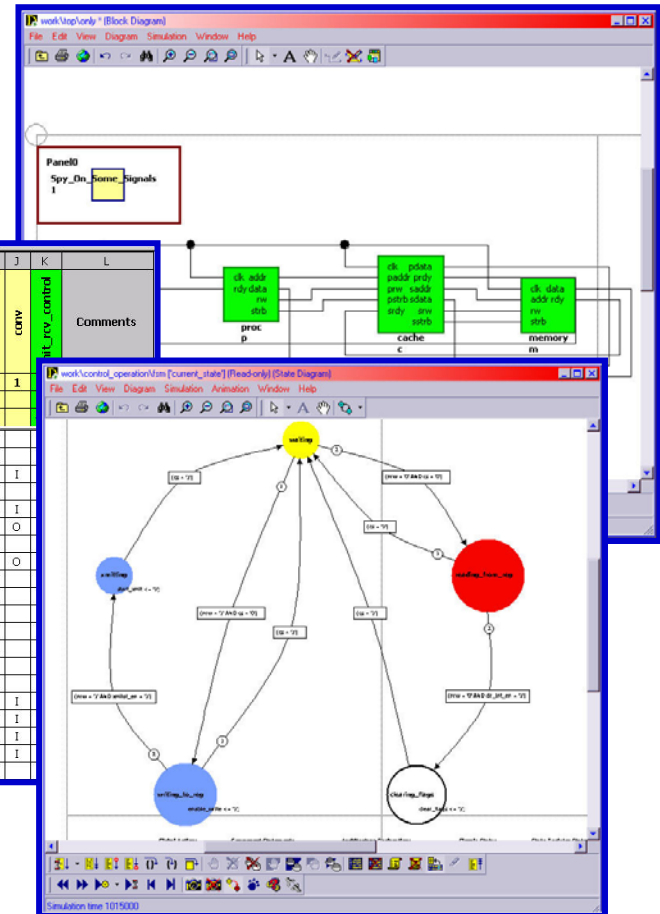
HDL Designer Series: Design Visualization & Documentation

Design structure



Interface-based design

Block diagrams

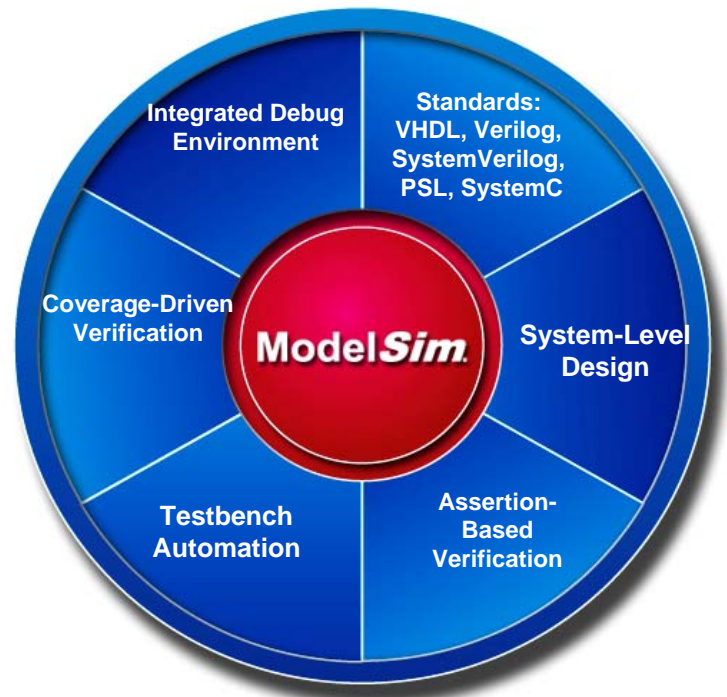


State diagrams

ModelSim 6.0

Verification Environment

- Most widely used simulator in the world
 - **#1 in Mixed-HDL simulation**
- Only unified verification environment supporting all major standards
 - **VHDL, Verilog, SystemVerilog, SystemC and PSL**
- Complete path from simulation to “Scalable Verification”
- Dedicated to high-performance
- Powerful and easy-to-use
- Award-winning Technical Support
- Best price/feature/performance



ModelSim 6.0

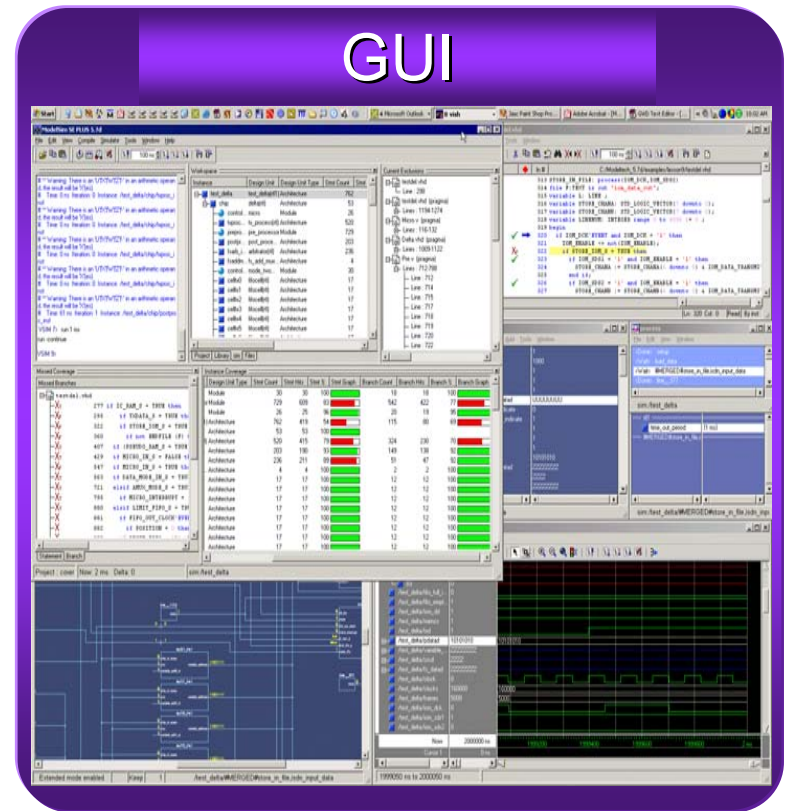
Verification Highlights

- Add Verilog PSL to existing VHDL support
- Functional coverage
 - **Based on PSL**
- SystemC enhancements
- More performance
- More SystemVerilog
 - Nearly all design constructs
 - DPI
- Highly intelligent GUI
- Shipping now (August 2004)

ModelSim 6.0

Modernized GUI

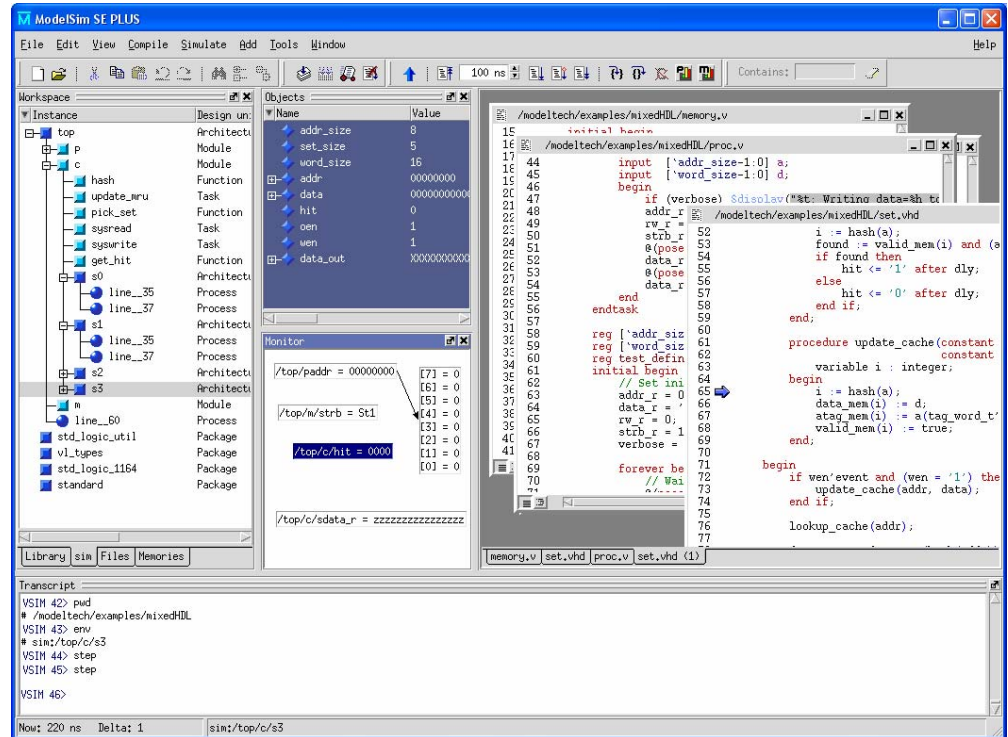
- Support for new methodologies
 - Assertion browser supports control and debugging with ABV
 - Functional coverage browser provides loading, control and reporting of functional coverage directives
- ModelSim is recognized as having best native GUI in the industry...
 - Best interactive debugger
 - All-in-one
 - Language Independent
 - Tcl/tk expandability



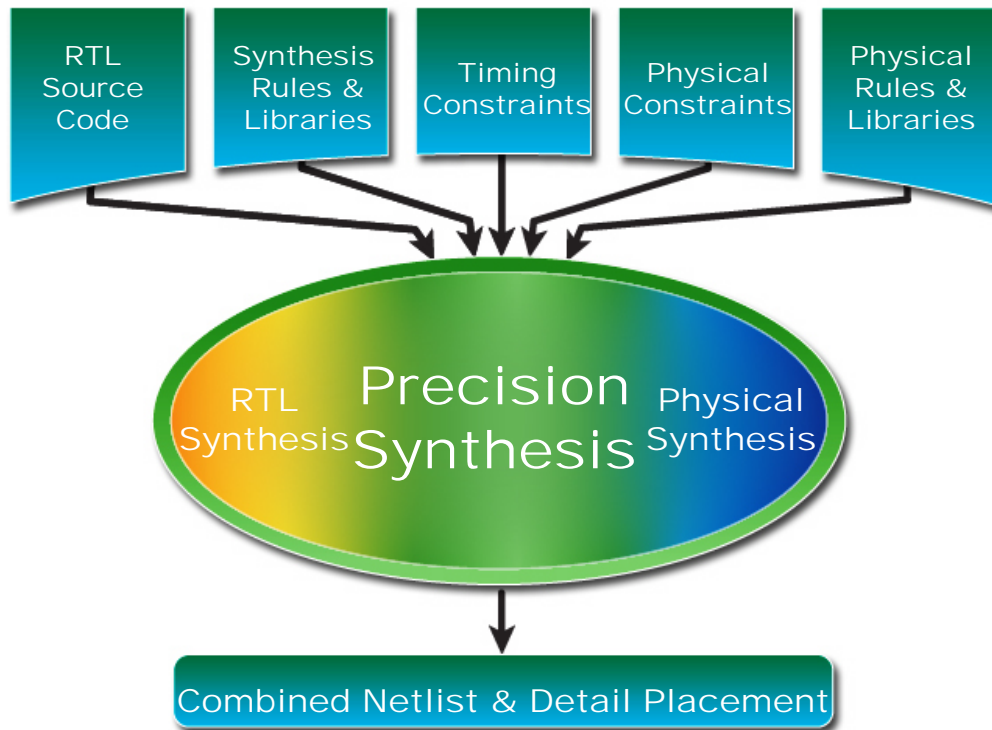
ModelSim 6.0

Improved User Interface

- New window layout
- Reorganized display of data
- Uses fewer windows
- Improved window manager
- More efficient use of screen real estate



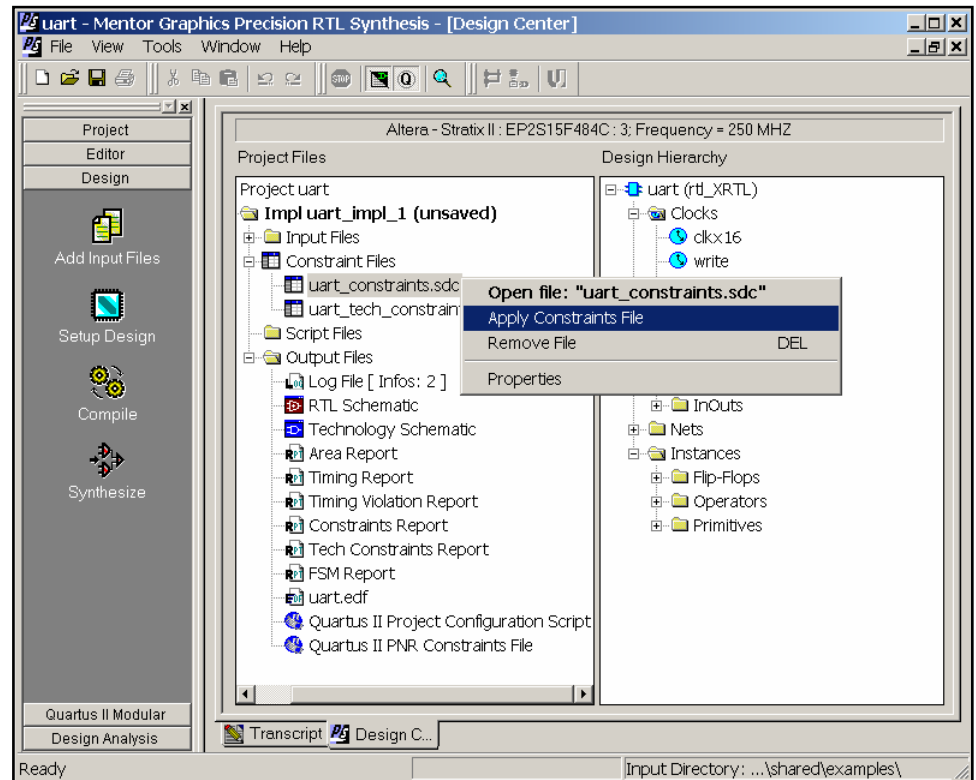
Precision Synthesis: Integrated Logical & Physical Synthesis



- Productivity enhancing synthesis tool suite
 - RTL + Physical
- Addresses design challenges of advanced, complex devices
 - Predictable design schedules
 - Reduced number of design iterations
 - Achieves timing closure

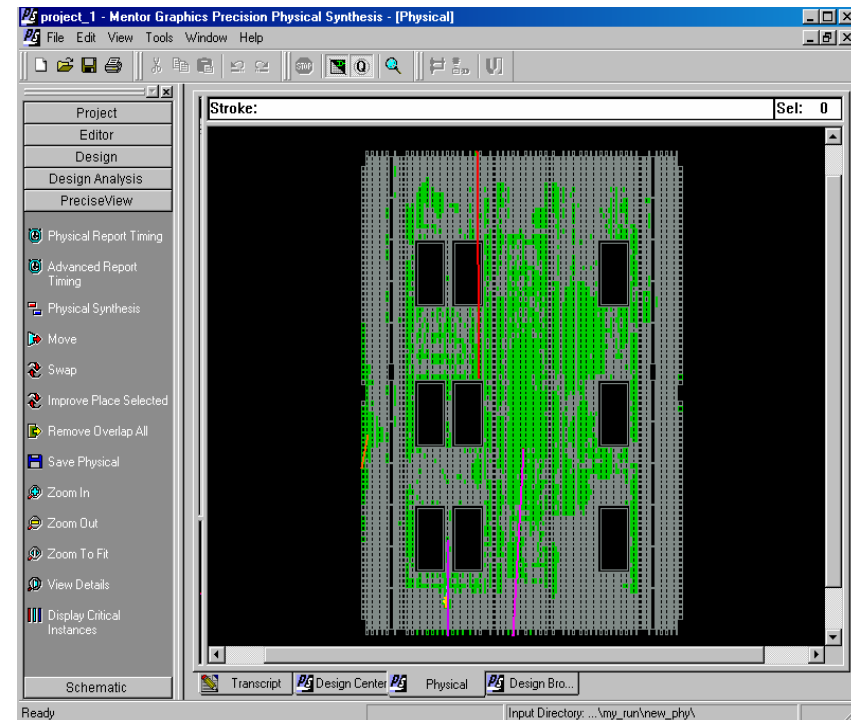
Precision RTL Synthesis

- Ease of use and competitive quality of results (QoR)
 - Incremental timing analysis allows rapid constraint debug iterations
 - Eliminates the need to re-run synthesis, or even a full static timing analysis again
 - Fewer design iterations
 - Precision RTL finds and incrementally fixes timing closure issues, early
 - Easy migration from ASICs
 - Standard SDC constraint file format



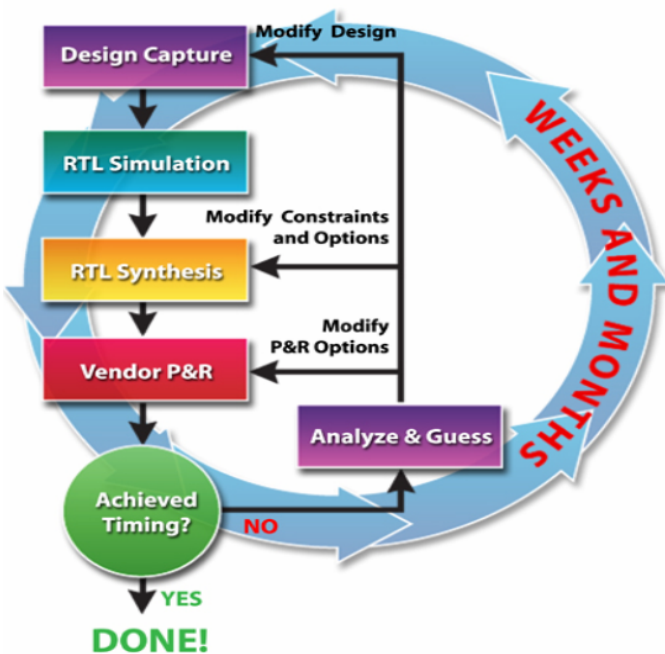
Precision Physical Synthesis

- The market leader that integrates RTL and Physical domain knowledge
 - Reduces design iterations by linking physical data with logic synthesis
 - Improves timing convergence by enhancing design analysis with ease of use
 - Intelligent and easy-to-use timing analysis
 - Cross-probe between RTL code, schematic, physical and timing views
 - Improves performance by interactively optimizing the placed design
- Supports Altera devices beginning with May 2004 release
 - Stratix, Stratix GX and Cyclone

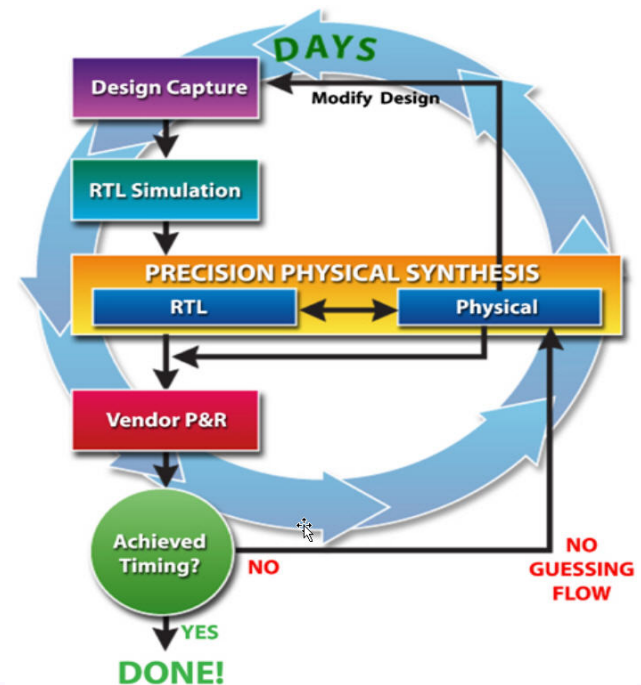


Why Precision Physical Synthesis?

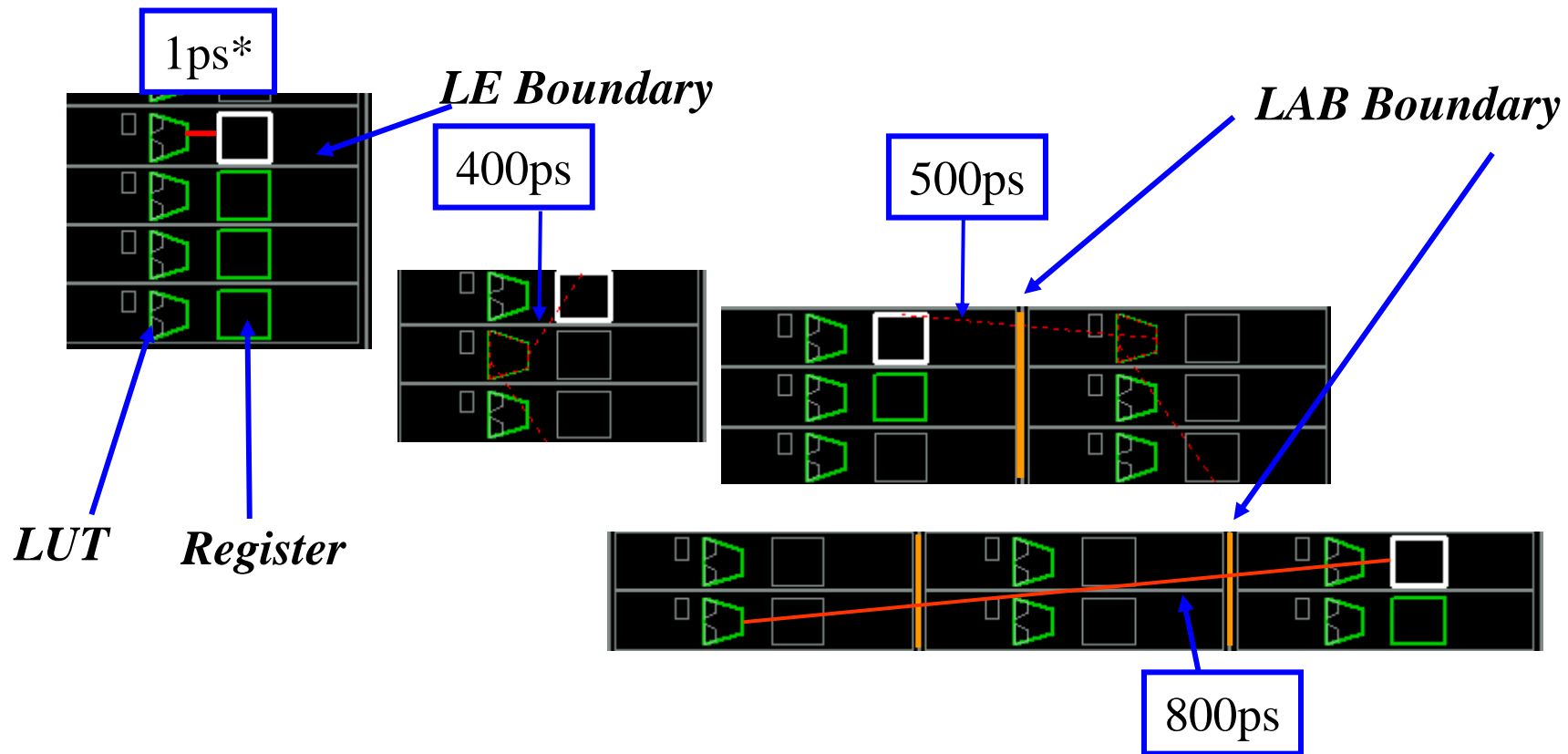
- Traditional approach to timing convergence
 - Iterative methods
 - Writing/re-writing RTL code
 - Modifying constraints/attributes
 - Multiple synthesis runs
 - Multiple P&R runs
 - Floorplanning



- With Precision Physical
 - Faster time to performance
 - Uses exact knowledge of placement / physical delays
 - Fast, incremental, deterministic
 - Placement optimization based on physical delays
 - Available resources guide optimization



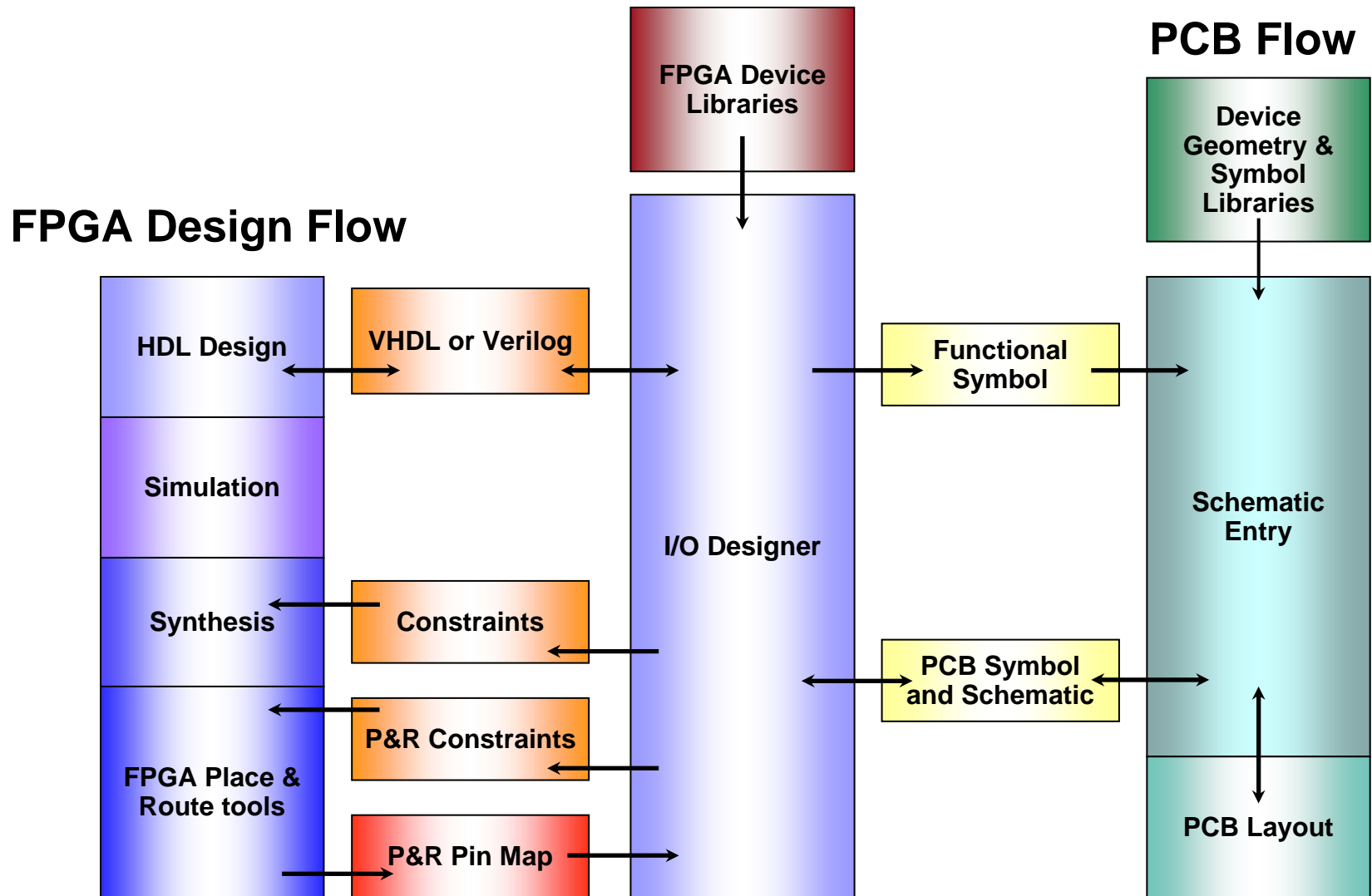
Traditional Floorplanning Fails



Delay is not a regular function of distance at a detailed placement level

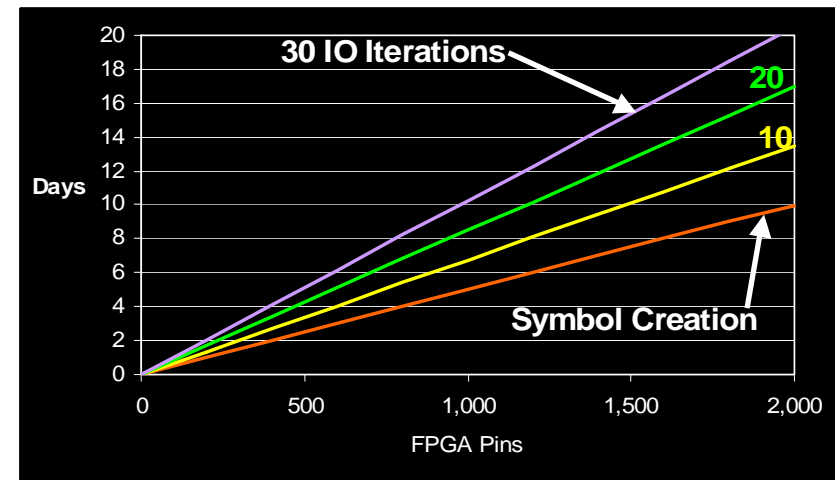
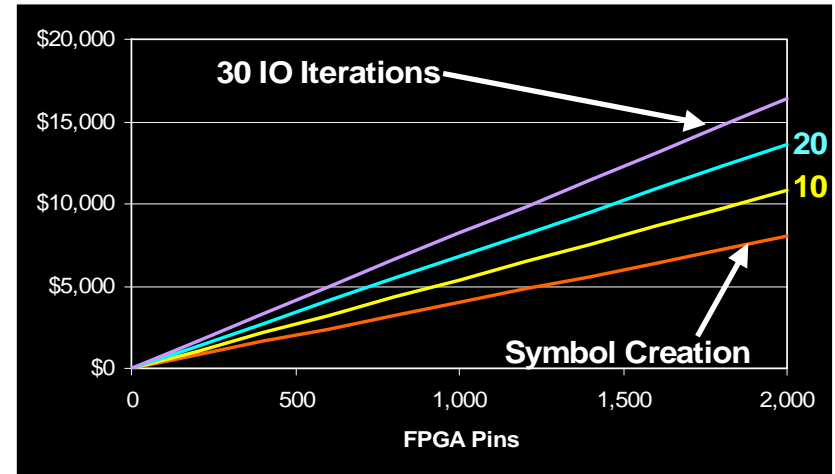
**Stratix-specific delay values*

I/O Designer: Concurrent FPGA-PCB Design



I/O Designer: Productivity

- Automatic FPGA – PCB symbol integration
 - Eliminates symbol creation and maintenance costs
 - Eliminates man-weeks of effort
 - Eliminates manual data entry issues
 - Promotes correct by construction

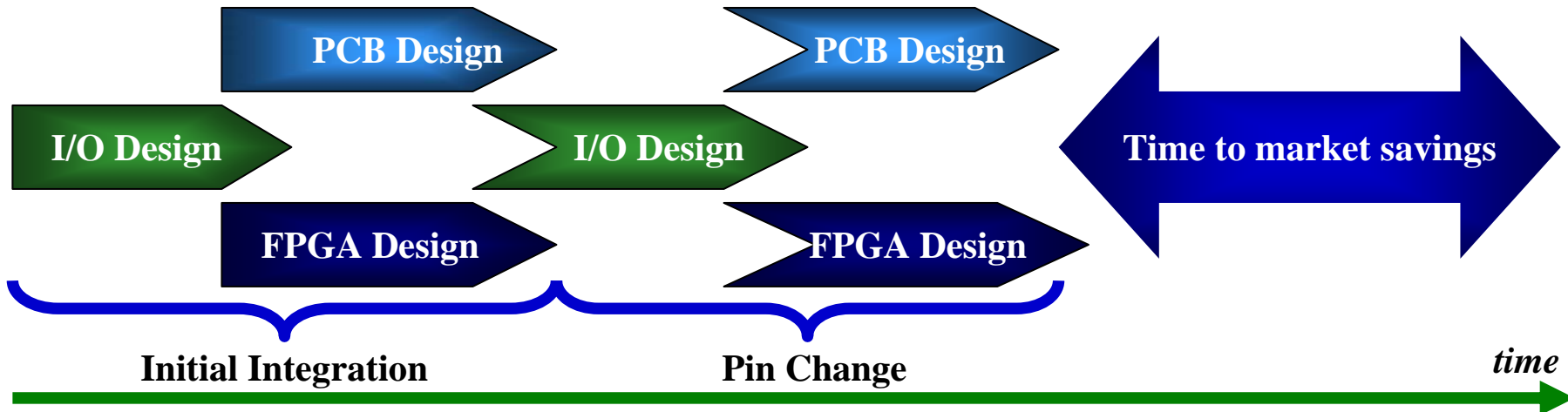


I/O Designer: Serial versus Concurrent

Traditional Flow:

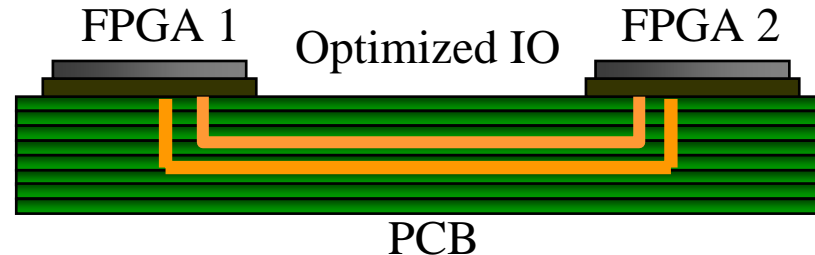
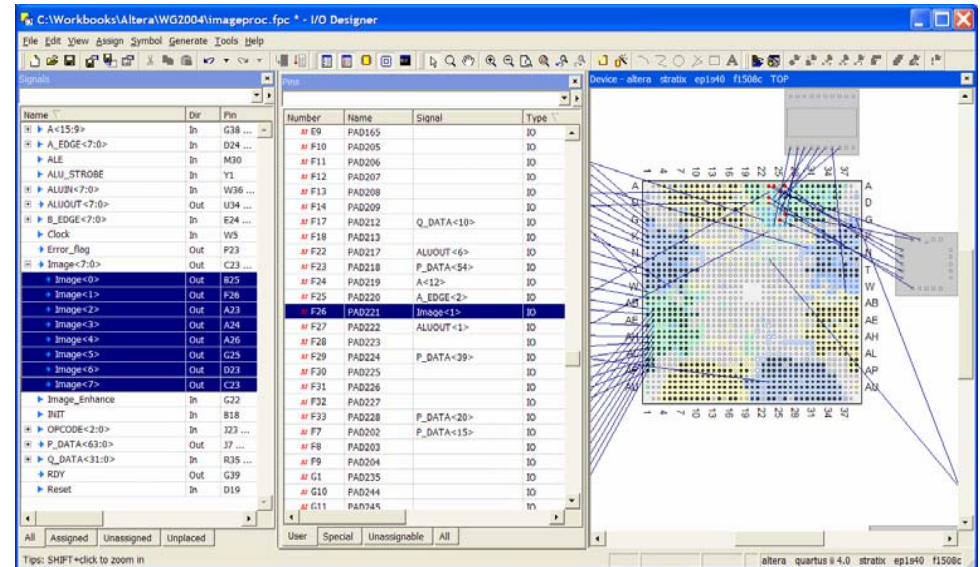


I/O Designer Flow:



I/O Designer: PCB Manufacturing Optimizations

- Multi-component, view-driven I/O design and optimization
 - Minimize crossovers
 - Unravel busses
 - Assign compatible I/O standards across multiple FPGAs
 - PCB design leads FPGA
 - Drives FPGA design flow
 - FPGA leads PCB
 - PCB floorplanning drives PCB design flow



Design Project Saving > 1 Month per complex FPGA on a PCB

Summary

- Mentor Graphics has all the tools you need to handle your next advanced Altera FPGA design
 - HDL Designer
 - ModelSim
 - Precision Synthesis
 - I/O Designer
- Industry leading tools
- Unique functionality
- Significant productivity gains

To Learn More

- Go to <http://www.mentor.com>
- Visit the Mentor Graphics Booth

The background is a vibrant blue with a complex pattern of white lines and dots, resembling a circuit board or a digital network. The lines are of varying thickness and form both straight and curved paths. Small white dots are scattered throughout, some acting as nodes in the network. The overall effect is a sense of high-tech connectivity and digital architecture.

Mentor Graphics®

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