FPGA

Design Once with Design Compiler® FPGA

The Best Solution for ASIC Prototyping

Synopsys Inc.

Your Design Partner

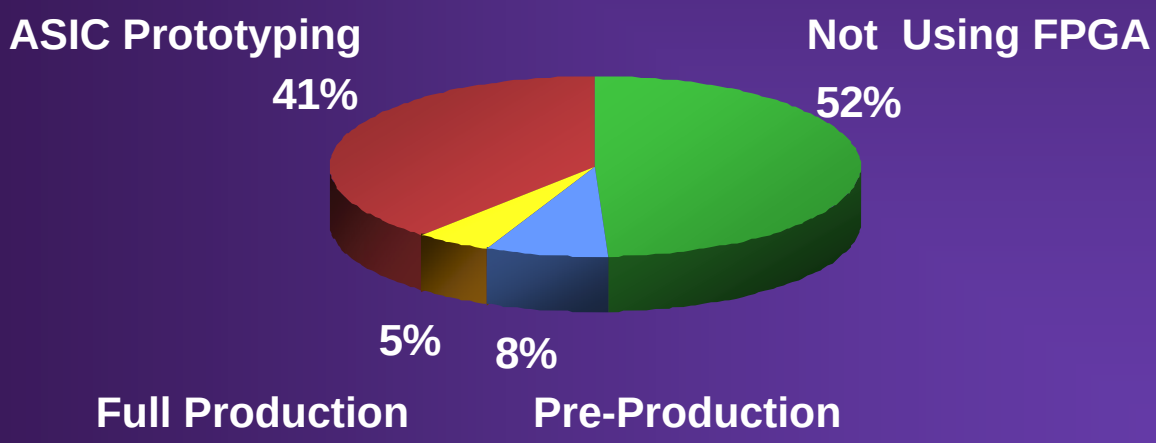
SYNOPSYS®

Agenda

- Prototyping Challenges
- Design Compiler® FPGA Overview
- Flexibility in Design Using DC FPGA and Altera Devices

41% of our ASIC customers are prototyping their ASIC designs in FPGA

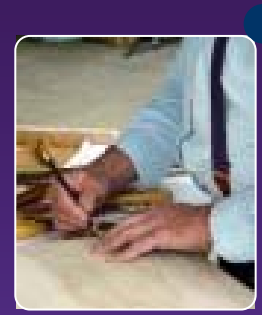
Synopsys 2004
Implementation Seminar Survey



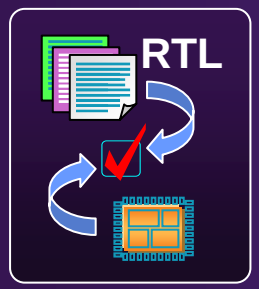
Customer's use of FPGA's – Multiple Responses Allowed

Compelling Needs are Fueling Prototyping Market

Earlier integration



Earlier software development



Faster verification

Avoid costly ASIC re-spins

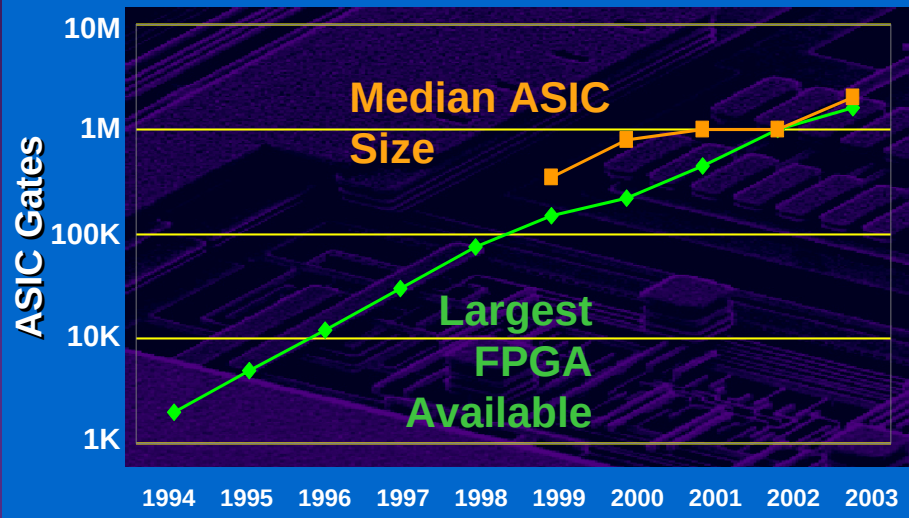
ASIC Design Data

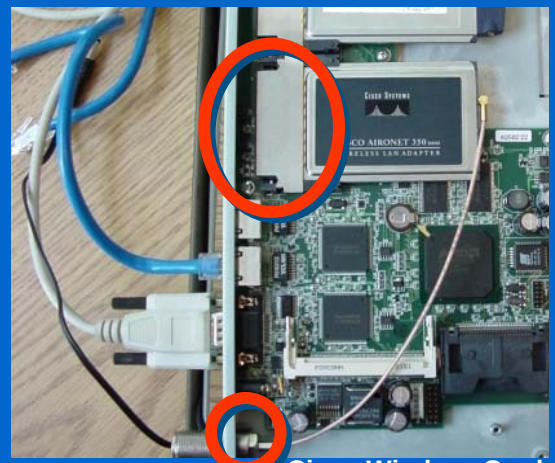
FPGA Synthesis

FPGA Prototyping Platform

ASIC Prototyping Poses Complexity Challenges

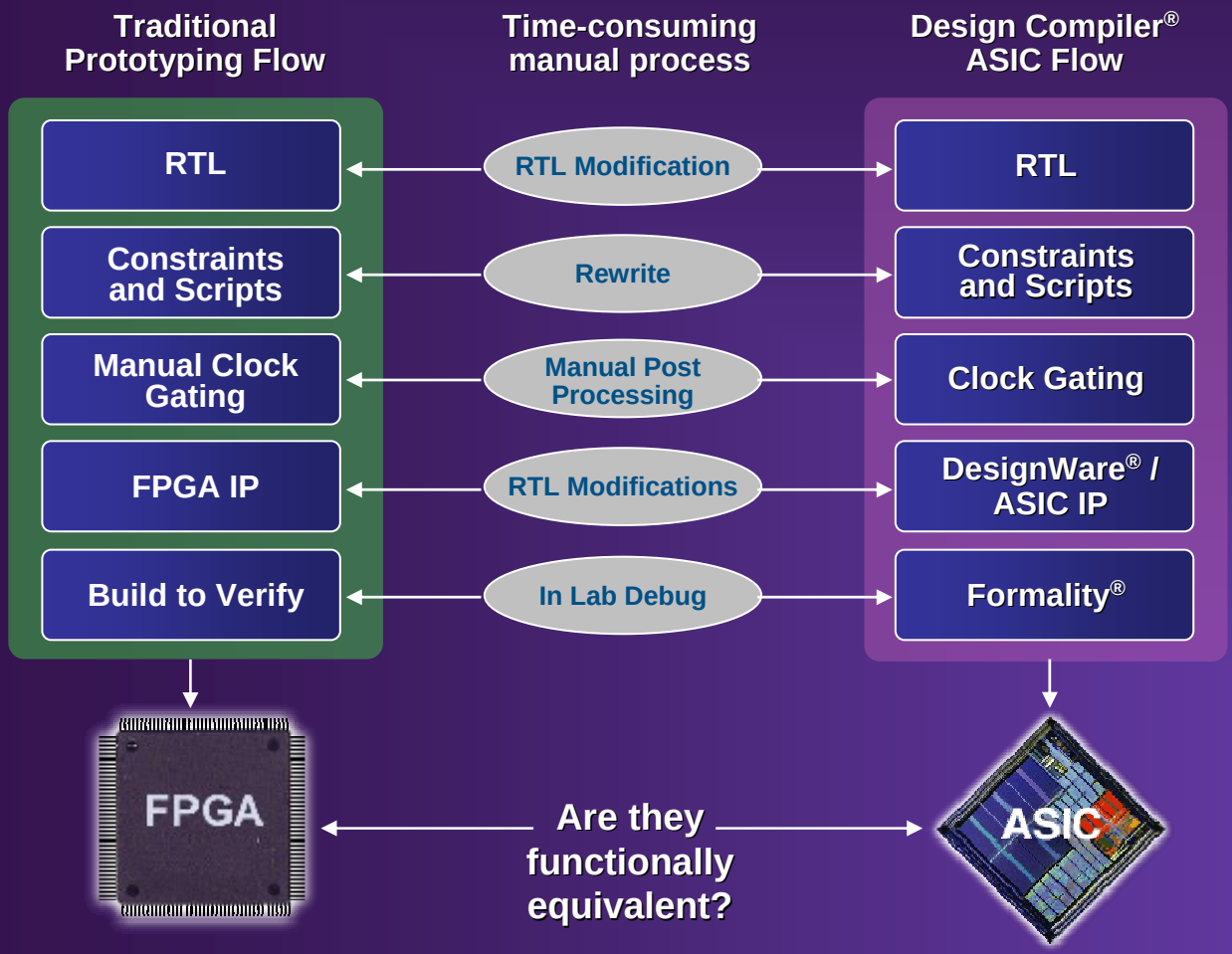
- **FPGAs are approaching ASIC-like complexity**
  - Require ASIC-strength solution
- **Timing Quality of Results is critical**
  - Many prototypes (such as, wireless) need to run at top speed
  - Real World Interfaces do not slow down for prototypes





Cisco Wireless Card

Two Flows = Two Implementations



- Different source, tools, IP and flows
- Time consuming, error prone, manual modifications
- Is design integrity guaranteed?

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Agenda

- Prototyping Challenges
- **Design Compiler® FPGA Overview**
- Flexibility in Design Using DC FPGA and Altera Devices

Design Compiler FPGA

Evolutionary

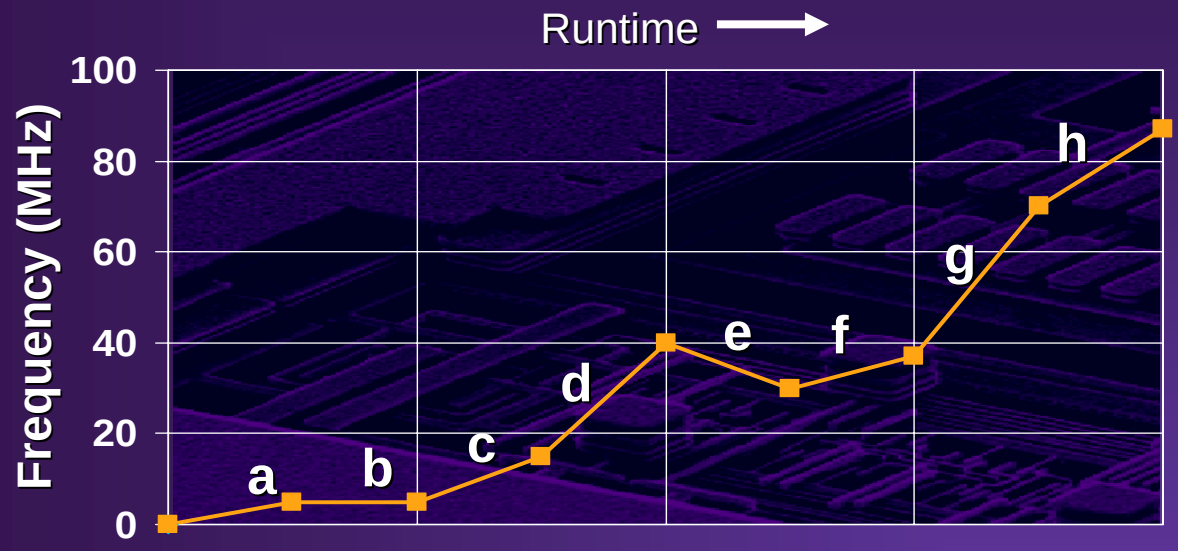
Revolutionary

- Industry standard ASIC-strength solution
- Best timing
- Fastest path to prototype

Industry Standard ASIC-Strength Solution
Built on Design Compiler® Technology

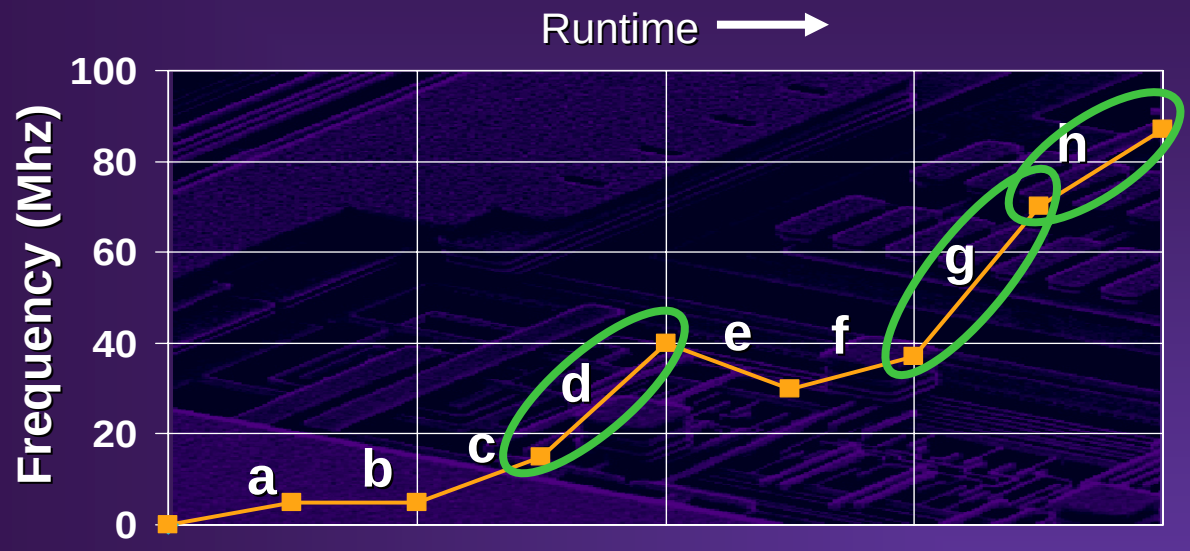
- **ASIC Reliability**
  - Proven through over 125,000 ASIC tapeouts
- **Advanced**
  - Algorithms that deal with the most challenging designs
- **Controllability**
  - Ability to customize the synthesis process to meet your design goals
- **Formal verification support**
  - ASIC strength platforms

Drawback of Traditional "Inflexible" Synthesis Process



Traditional Synthesis Process *"Inflexible"*

Adaptive Optimization™ Technology Delivers the Best Timing



Traditional Synthesis Process *"Inflexible"*

Select best synthesis algorithms

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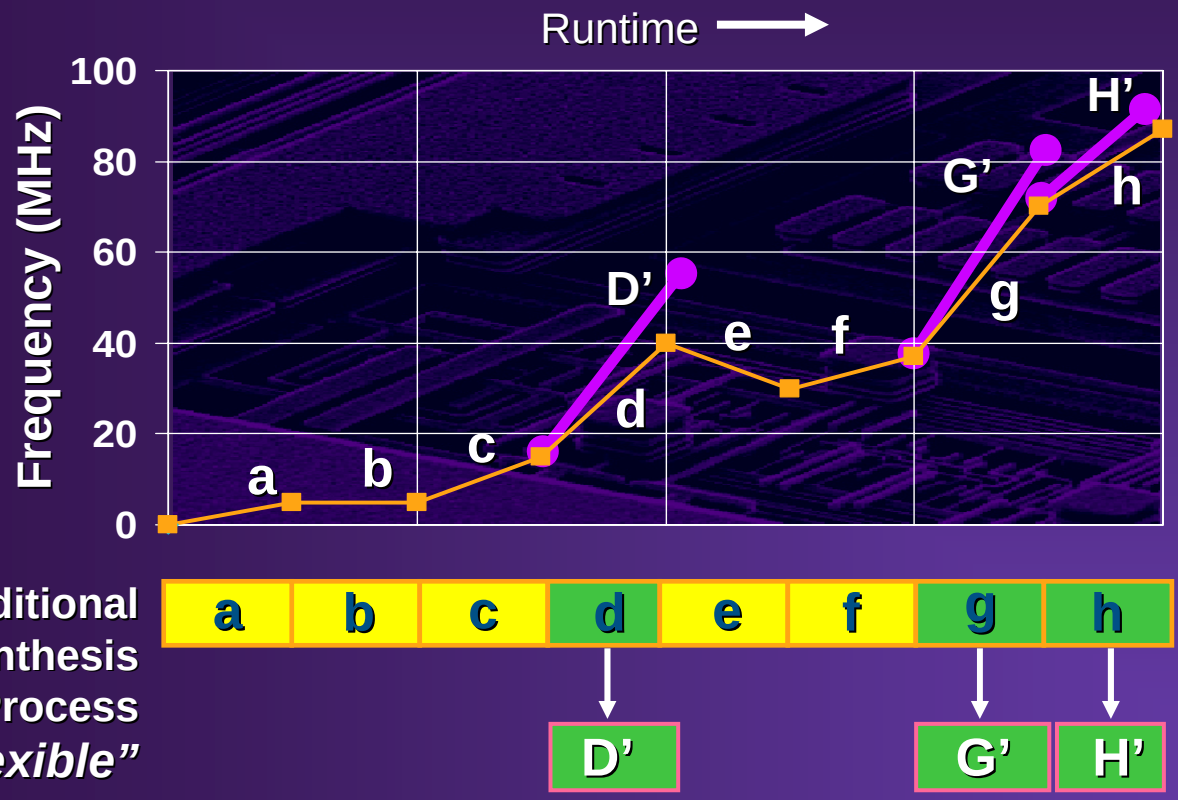
Adaptive Optimization™ Technology Delivers the Best Timing



Select best synthesis algorithms

Dynamically tune algorithms

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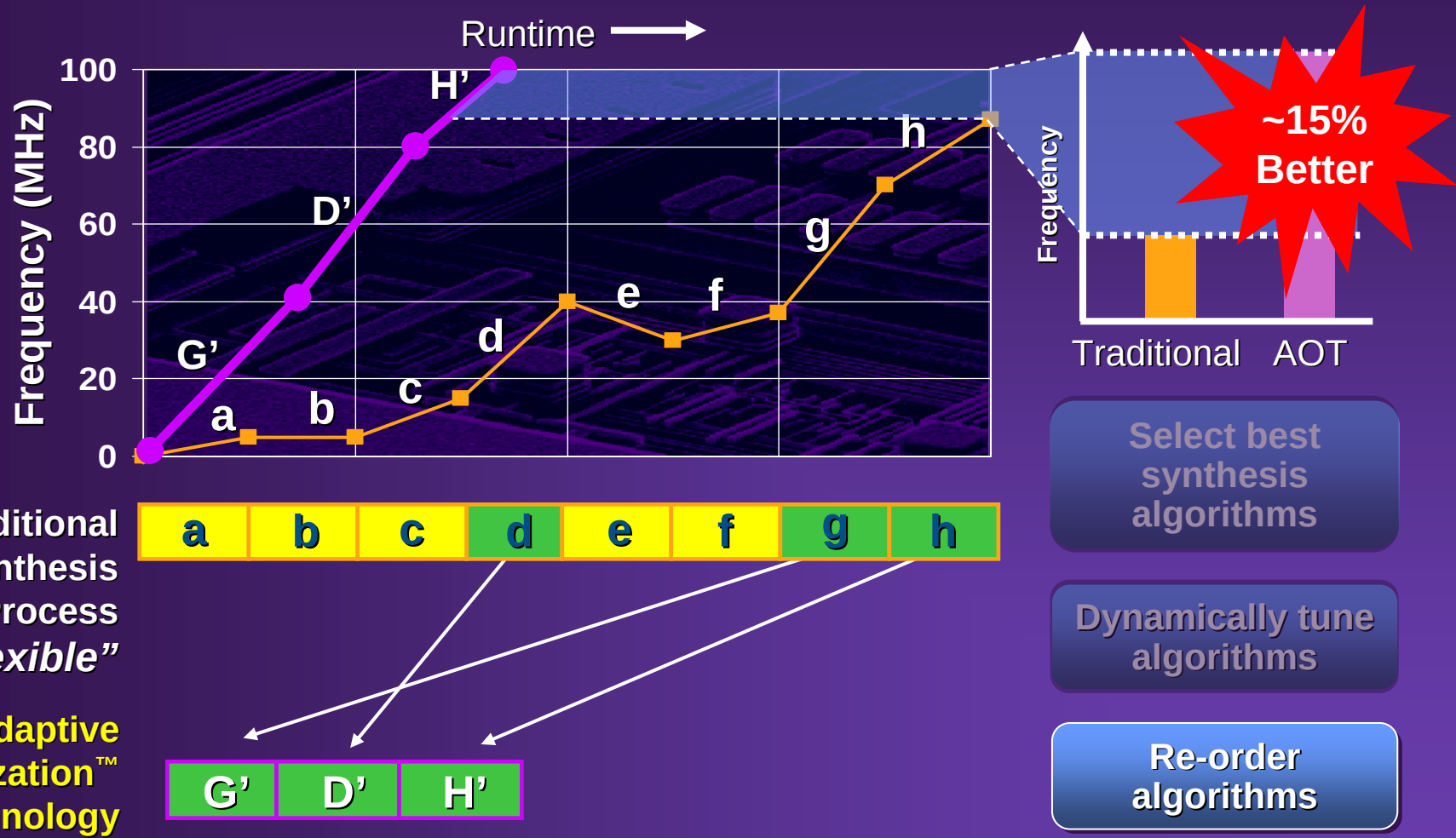
Adaptive Optimization Technology Delivers the Best Timing



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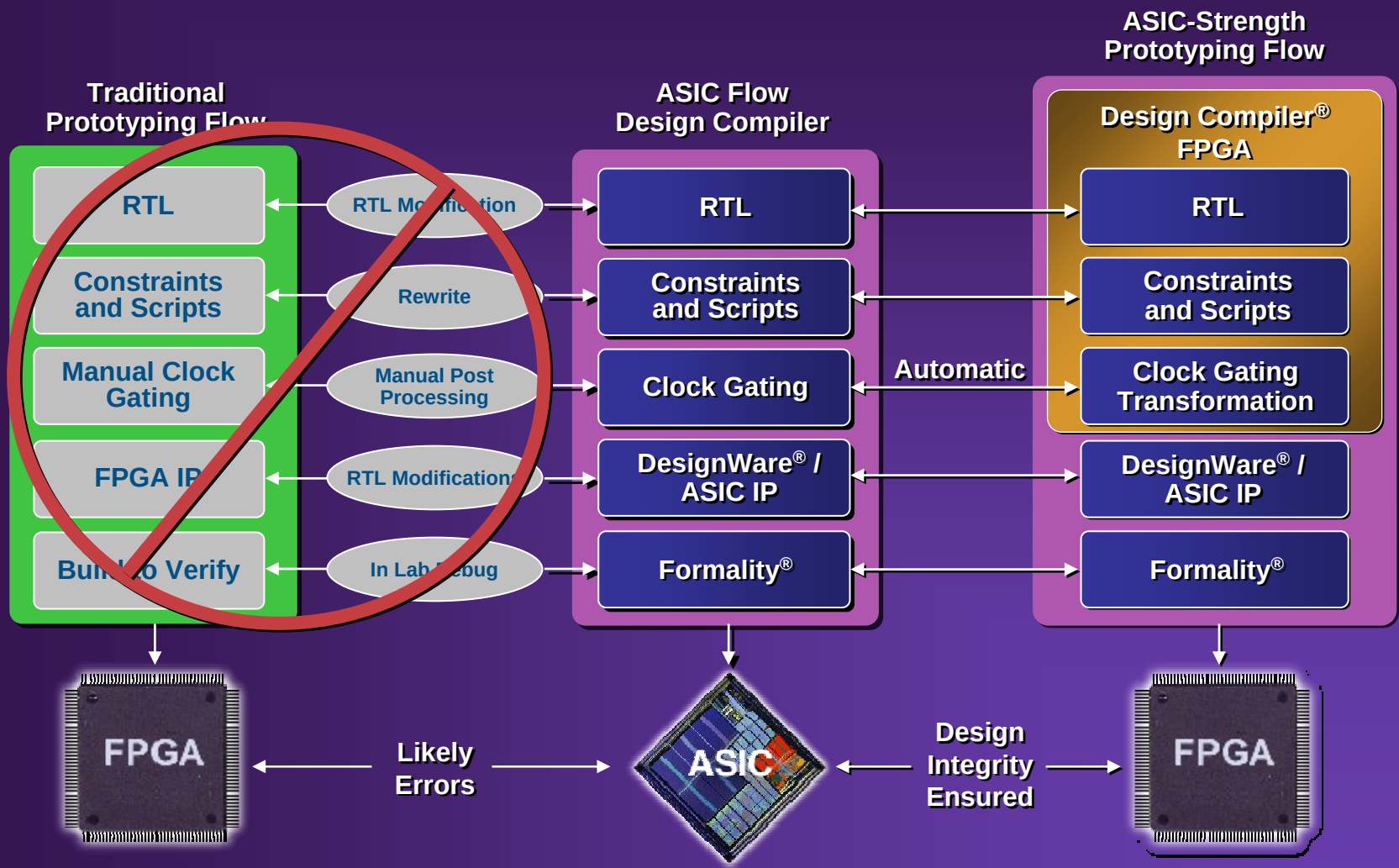
Design Once With Design Compiler® FPGA



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ASIC-Strength Flow at Alereon

"The [DC FPGA] methodology and flow were exactly the same as Design Compiler so we were able to use the same scripts, constraints and RTL from the ASIC design."

- Dave Ohmann, IC Design Engineer

Best Timing at AMD

"…A significant speed increase over what we were able to achieve with other FPGA synthesis tools."

- Dirk Haentzschel, Sr. Design Engineer

Fastest Path to Prototype at Matrix Semiconductor

"Design Compiler FPGA was the only FPGA synthesis solution that had an integrated ASIC/FPGA flow, providing the easiest path to prototype our technology."

-James Tringali, ASIC Design Manager

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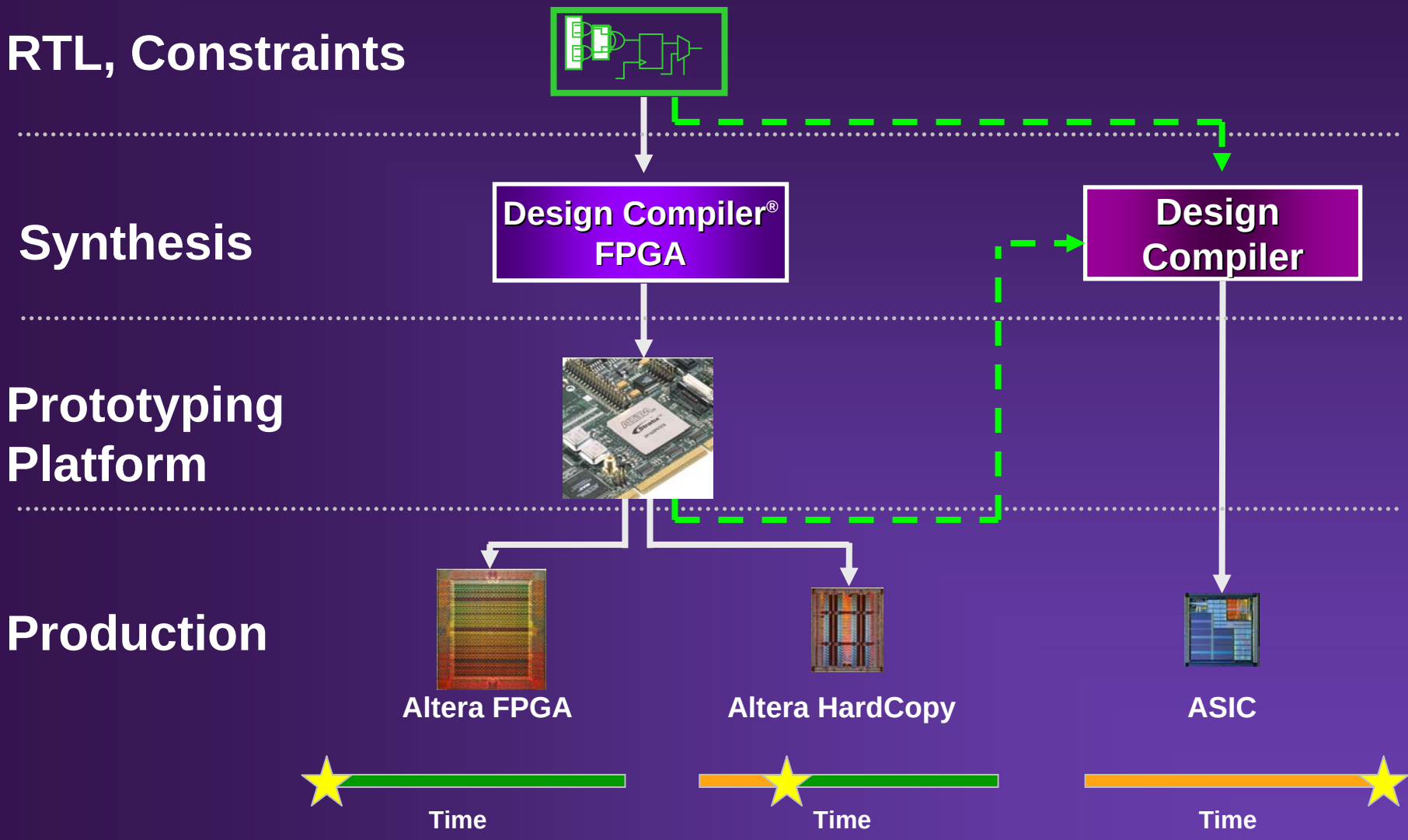
Design Once Implementation Flow



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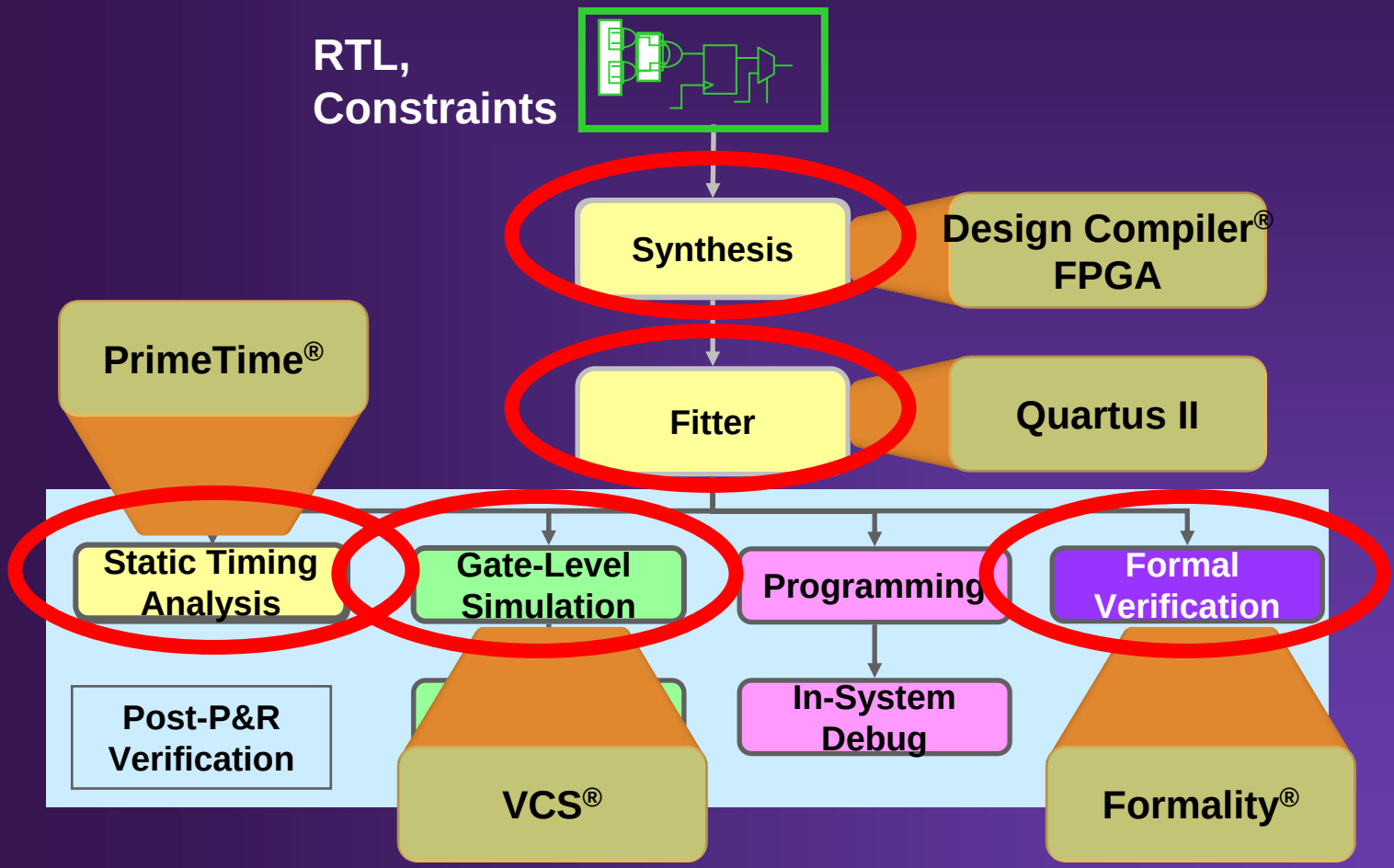
ASIC Strength Flow for Flexibility



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Design Compiler® FPGA
Supported Devices and Platforms

- Stratix™
- Stratix™ GX
- Cyclone™
- HardCopy™
- Stratix™ II (Available 2004.12)
- Cyclone™ II (Available 2005.03)

DC FPGA is available today on:
Solaris (32 and 64 bit) and Linux

DC FPGA is Having Significant Success

Over 80 Customers

Fastest Path to Prototype
DC FPGA Partners

Auspy	Automated Partitioning
AccelChip	DSP Algorithms in Silicon
Temento systems	Embedded Instrumentation
eVe	Hardware Assisted Verification
tensilica	Configurable Cores
Aptix	Reconfigurable Prototyping Platforms

Summary

Design Compiler® FPGA

- **Industry standard ASIC-strength solution**
  - Flexibility and Stability of DC
  - Advanced Algorithms
- **Best timing**
  - Adaptive Optimization™ Technology
- **Fastest path to prototype**
  - Ensuring Design Integrity between Prototype and ASIC
- **Flexibility to target Altera FPGA or HardCopy Devices**

Design Once!