Using the RTL Viewer in the Quartus II Software

MJL

H.M Kim

Agenda

What is the RTL Viewer and Why Use It?

Feature Overview & User Interface Details

Technology Map Viewer

Enhancements & References

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What Is the RTL Viewer?

- A Graphical Representation of the Register Transfer Level (RTL) Design

- A Viewer that Allows You to Analyze How Design Was Interpreted by the Quartus II Software

- Introduced Due to Popular Demand

- Similar to Viewer in EDA Synthesis Tools (Synplicity, Mentor Graphics) and ASIC Debug Tools (Debussy)

User Interface

RTL Viewer Toolbar

Hierarchy List

Schematic View

Why Use the RTL Viewer?

- View Your Initial Synthesis Results to Determine Whether You Have Implemented Desired Logic

- Do a Visual Check of Your Design Before Performing a Simulation

- Trace Through Initial Synthesis Netlist to Analyze Source of Problems Found During Verification

- Locate the Source Of a Particular Signal When Debugging Design

- Locate Nodes of Interest in VQM/EDIF Netlist When Making Assignments to Optimize Design

What Can Be Viewed?

- **Quartus II Results After Analysis & Elaboration**
  - Before Quartus II Synthesis Optimizations, Before Any Netlist Optimizations, Before Fitter

- **Source V, VHD, TDF, BDF, GDF**
  - View Blocks such as AND Gates, MUX's, Adders, and Registers

- **Third-party VQM, EDIF**
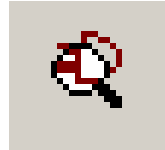 - View ATOMs in Netlist such as Logic Cells

Agenda

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Launching RTL Viewer

- **Analyze & Elaborate Design**
  - Or Any Compilation Flow that Includes Elaboration
- **Choose RTL Viewer (Tools menu)**

- **First Time You Open RTL Viewer After Analysis & Elaboration or Compilation, RTL Preprocessor Starts Automatically**
  - Once Only Per Analysis & Elaboration/Compilation

Highlighting/Selecting in Schematic View

■ Enable **Selection Tool** from RTL Viewer Toolbar

■ Click to Select (Use Shift for Multiple Items)

– Highlight Node or Port

– Highlight All Connected Nets for Wire or Bus

■ Selecting Item in Schematic View Also Expands Hierarchy List to Show Selected Item

Zooming in Schematic View

- Enable **Zoom Tool** from RTL Viewer Toolbar

- Click to Zoom In, Left-Click to Zoom Out
- Keyboard Shortcuts: Ctrl+Space to Zoom In, Ctrl+Shift+Space to Zoom Out
- Toggle Between Zoom Tool and Selection Tool Using the Icons
  - You Can't Select Nodes If the Zoom Tool Is Enabled!

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Traversing Design Hierarchy

■ Navigate in Hierarchy List, or Use Schematic View to Traverse Hierarchy

■ With **Selection Tool**, Mouse Cursor Changes Over Areas of Schematic to Indicate You Can:

– Double-Click to Go Down in Hierarchy or Right-Click and Select **Hierarchy Down**

● Opens Lower-Level Schematic

– Double-Click to Go Up in Hierarchy or Right-Click and Select or **Hierarchy Up**

● Returns to Higher-Level Schematic
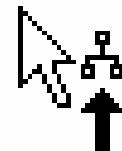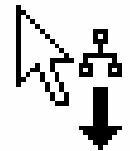
Page Partitioning

- For Large Designs, Netlist Partitioned Into Multiple Pages in Schematic View

- Control How Much of Design on Each Page Under **Display Settings** on **RTL Viewer** Tab of **Options** Dialog Box (**Tools** Menu)
  - **Nodes Per Page** Specifies Number of Nodes Per Partitioned Page, Default = 50, Range = 1 to 1000
  - **Ports Per Page** Specifies Number of Ports (or Pins) Per Page, Default = 1000, Range = 1 to 2000

Page Partitioning

- **Title Bar for RTL Viewer Window Indicates Page <*Current Page Number*> of <*Total Number Of Pages*> for Current Display**
  - Shown on Title Bar for Quartus II Software When RTL Viewer Window Is Maximized
- Example:
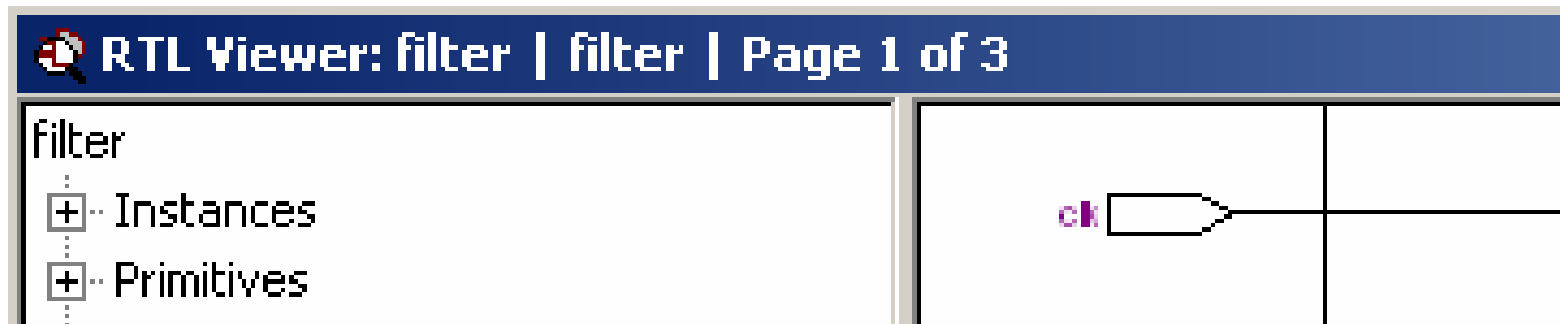
Moving Between Pages

- Move to Another Schematic Page with **Previous Page**/**Next Page** (**View** Menu or RTL Viewer Toolbar)

- Go to Particular Page of Schematic with **Go To** (**Edit** Menu, or Right-Click In Schematic and Choose **Go To,** then Select Page Number)

- Go Back to Previous Page View with **Back**, Return to that Page with **Forward** (**View** Menu or RTL Viewer Toolbar)
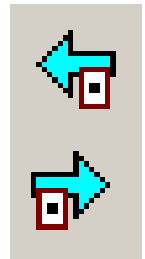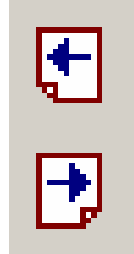
Following Nets Between Pages

- **Input and Output Connectors Used to Represent Nodes that Connect Between Pages**
- **Right-Click for Menu to Trace Net in Hierarchy**
  - Select Desired Net to Highlight It In Red First
  - **Related** Commands Open Pages with Other Nets Fed by/Feeding Same Source/Destination
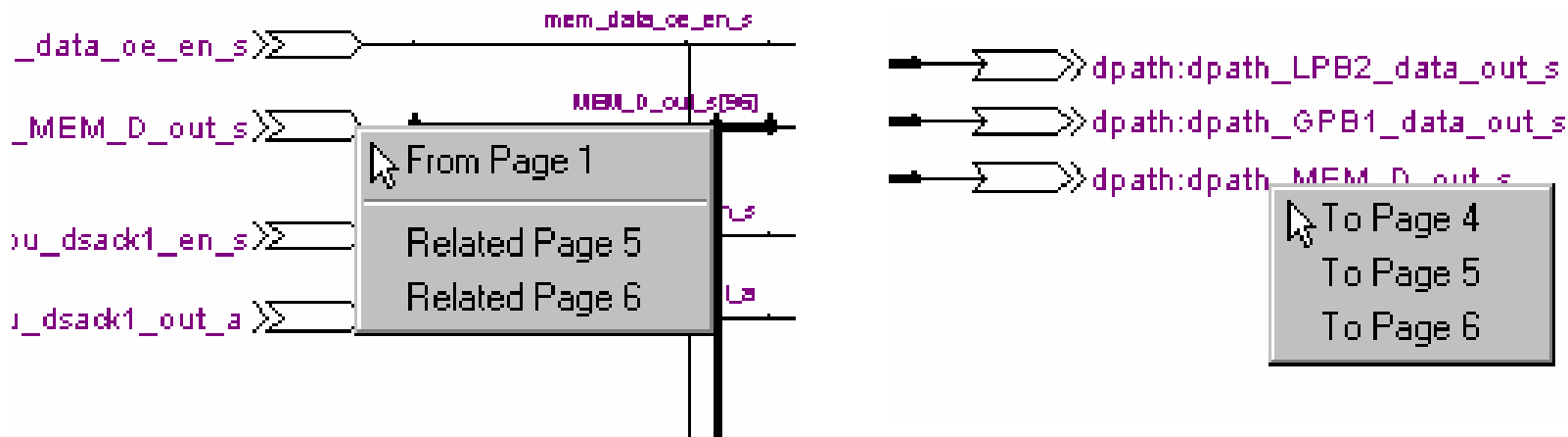
Go To Net Driver

- To Locate Source Of a Net, Select The Net, Right-click and Choose **Go To Net Driver**
  - Opens Correct Page Of Schematic (If Needed), Adjusts Focus of Page So You Can See Net Source
- Applies Only to Nodes In the Same Netlist Hierarchy

Filtering

- Filter Out Nodes and Nets to View Only Logic Path(s) Related to Particular Node(s)
- Select Nodes or Ports You Want to See, Choose **Filter**, Choose Appropriate Command
- Applies Only to Nodes In Same Netlist Hierarchy
- If You Click Item In Hierarchy List, Schematic View Displays Unfiltered View of Appropriate Hierarchy Level
    - Can Not Use Hierarchy List to Select Items or Navigate In a Filtered Netlist

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Filter Options

- **Sources, Destinations, Sources & Destinations**
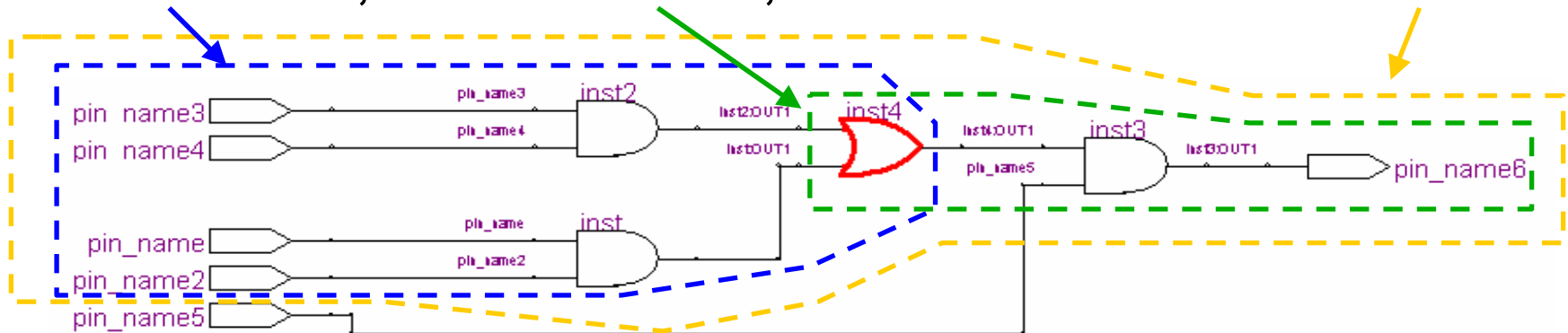
- **Between Selected Nodes**
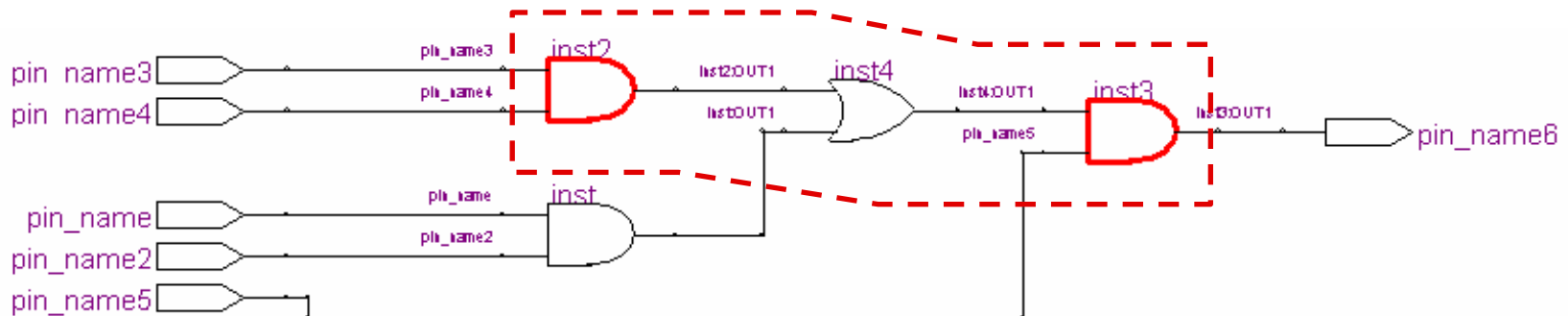
Filtering Stops Tracing Through Netlist When It Reaches…

- A Port of Current Hierarchy

- A Specified Number of Levels/Schematic Elements (10 by Default)

  – Specify **Number Of Filtering Levels**, Range 1 to 100, Under **Filtering Settings** in **Options** Dialog Box (Tools Menu), **RTL Viewer** Tab

- A Register In the Current Hierarchy Level (Optional, On By Default)

  – Turn **Stop Filtering at Register** Option On or Off Under **Filtering Settings** in **Options** Dialog Box (Tools Menu), **RTL Viewer** Tab

Probing to Source Design File

- Right-Click Node In Schematic and Choose **Locate In Design File**

- Opens Source Design File In Another Window
  - Return to RTL Viewer by Closing Window

- Highlights Definition of Node In Text Editor or Block Design File Editor

Find

- Select **Find** (View Menu), Click **Find** Icon In RTL Viewer Toolbar, or Right-Click In Schematic View and Choose **Find**

- **Find** Dialog Box Is Standard Search Used Throughout Quartus II

- For **Search** Direction, **Up** Searches from Current Hierarchy to Upper (Parent) Hierarchies, **Down** Searches From Current Hierarchy to Lower (Children) Hierarchies

Agenda

What is the RTL Viewer and Why Use It?

Feature Overview & User Interface Details

Technology Map Viewer

Enhancements & References

Technology Map Viewer

- New in Quartus II 4.1!
- Shows Netlist After Mapping Design to Atoms in Target Device Technology (LCELLs etc)
- Run from Tools Menu
- Most Features (Navigating, Filtering, Zooming, etc.) Same as RTL Viewer

Tools   Window   Help

Run EDA Simulation Tool
Run EDA Timing Analysis Tool
Launch Software Debugger   Ctrl+Shift+D

Compiler Tool
Simulator Tool
Timing Analyzer Tool

Resource Optimization Advisor
Timing Optimization Advisor

Chip Editor
RTL Viewer
Technology Map Viewer

SignalTap II Logic Analyzer
In-System Memory Content Editor
Programmer

MegaWizard Plug-In Manager...
SOPC Builder...
Tcl Scripts...

Customize...
Options...
License Setup...

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Technology Map Viewer

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Instances In Technology Map Viewer

■ **Shows Atoms in a Hierarchy, but Not User's Port Names for Hierarchy Blocks**

  – Port Name Information Is Not Maintained Throughout Synthesis

  – Optimizations Change Atom Names When Merging Logic etc.

  – Ports Appear with Default Names IN1, OUT1 etc.

taps:inst
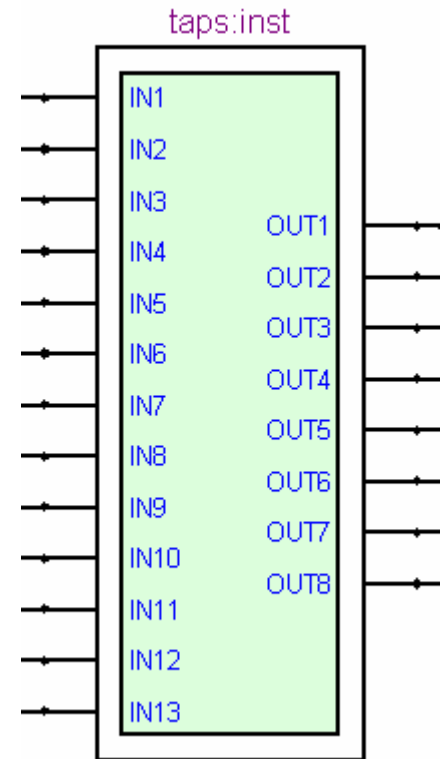
Locate Timing Path

- Locate Path Listed in Timing Analyzer Report

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Locate Timing Path

■ Delays Annotated from Timing Analyzer Report

<Node Name> (<Interconnect (IC) Delay>, <Cell delay>)

filter~27 (0.402 ns, 0.075 ns)

Technology Map Viewer: filtref | Timing | Page 1 of 1

filtref
- Instances
- Primitives
- Pins
- Nets

Timing | Page 1 of 1

Total delay: 7.580 ns

filter~30 (0.000 ns, 0.000 ns)

CLK
DATAB
SYNCH_DATA   COMBOUT
DATAD   REGOUT
ACLR
SLOAD

LCELL (0300)

filter~27 (0.402 ns, 0.075 ns)

CLK
SYNCH_DATA
DATAD   COMBOUT
                    REGOUT
ACLR
SLOAD

LCELL (FFF0)

xn_2[1]~reg0 (0.690 ns, 0.366 ns)

CLK
DATAA
DATAB
SYNCH_DATA   COMBOUT
DATAD   REGOUT
ACLR
SLOAD
ENA

LCELL (D9C8)

xn_3[1]~reg0 (0.325 ns, 0.075 ns)

CLK
DATAA
DATAB
SYNCH_DATA   COMBOUT
DATAD
ACLR
SLOAD
ENA

LCELL (F588)

Total delay: 7.580 ns

LCELL (D9C8)

<Primitive Type> (<LUT Mask>)

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RTL Viewer Optimizations

Quartus II 4.0
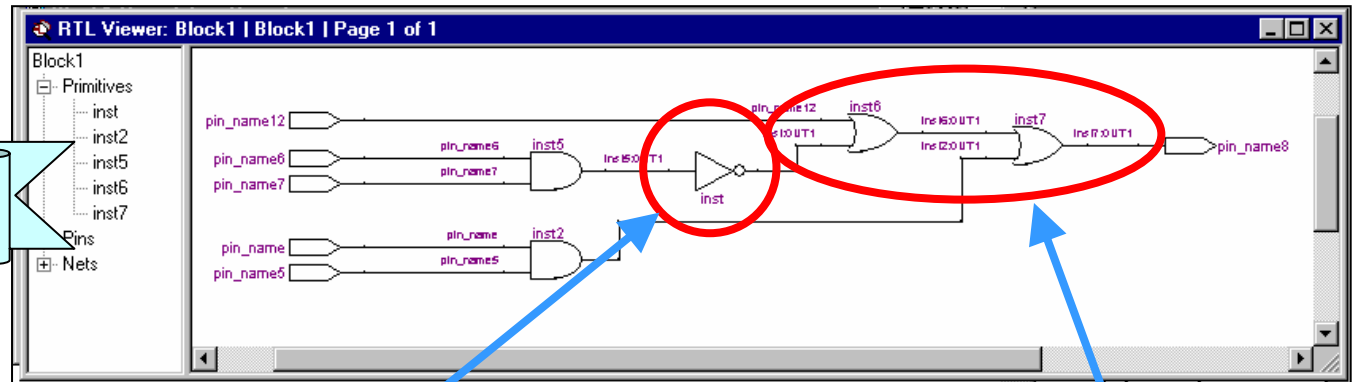
Not Gate → Inversion

Combinational Logic Merging

Quartus II 4.1
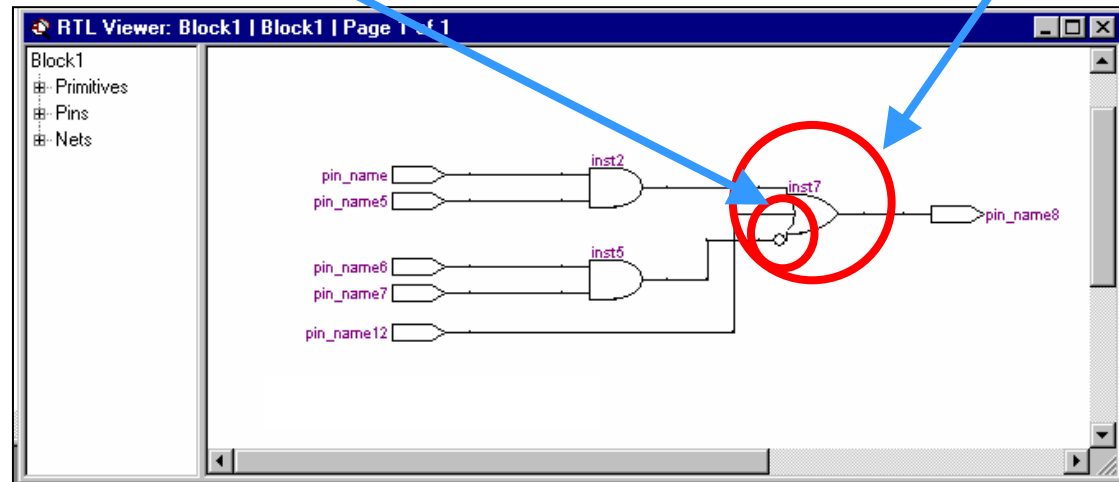
RTL Viewer Operator Symbols

- ■ Quartus II 4.0: All Operators Are Box Shaped
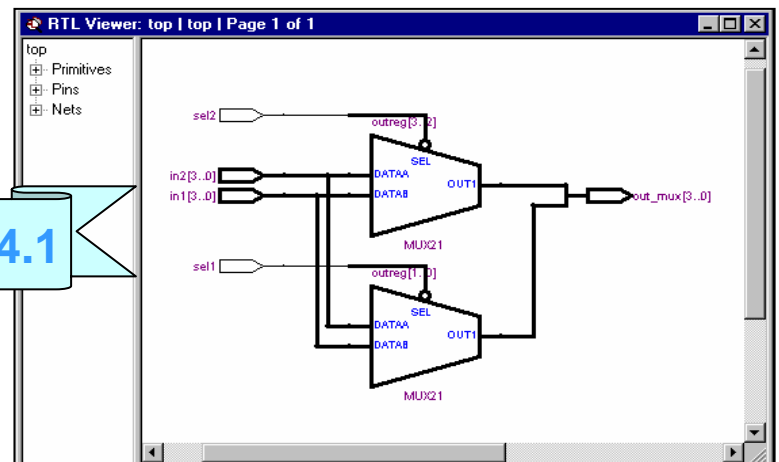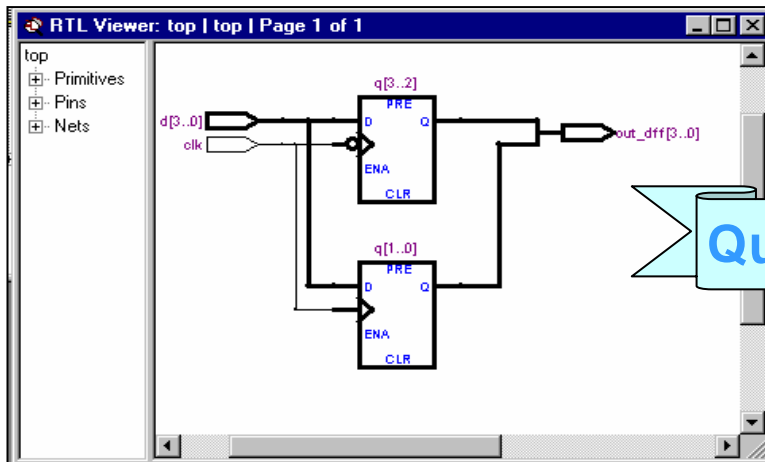- ■ Quartus II 4.1: Operators Are Shaped Differently from Other Primitives

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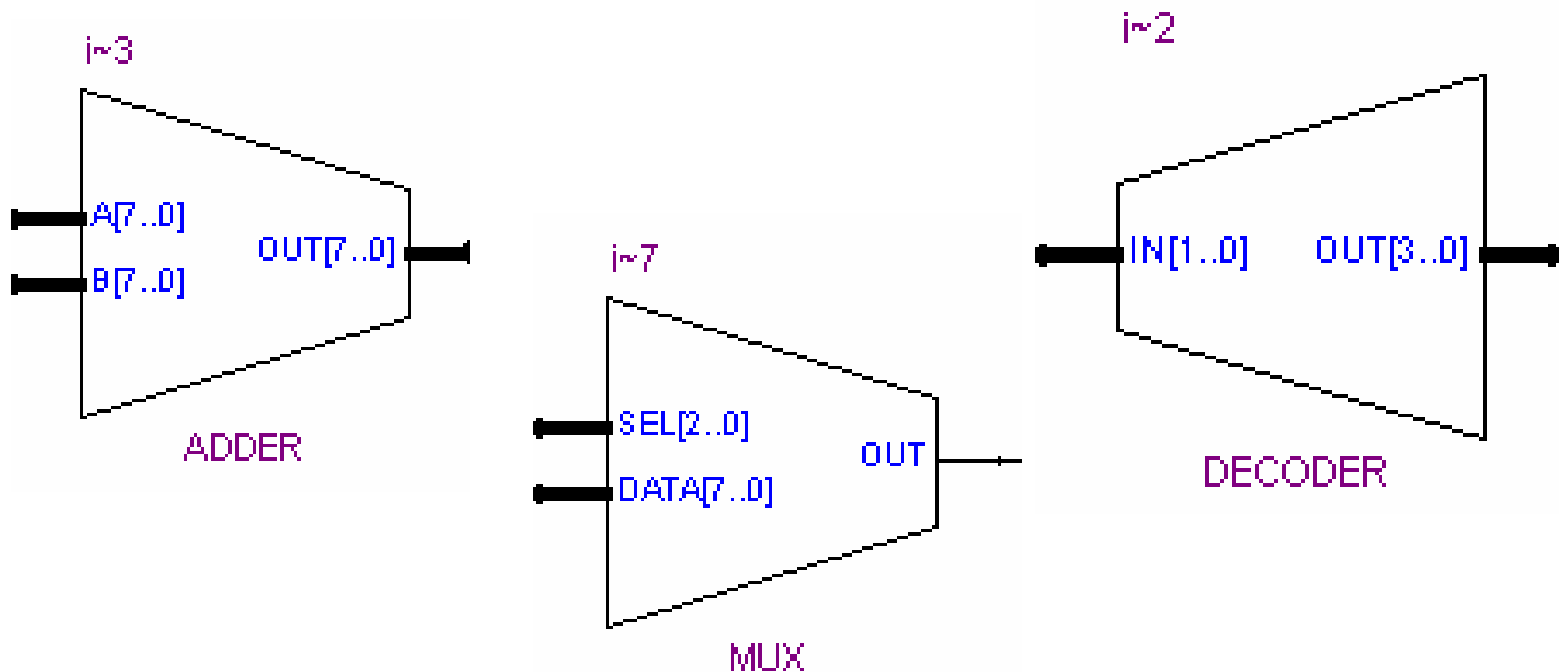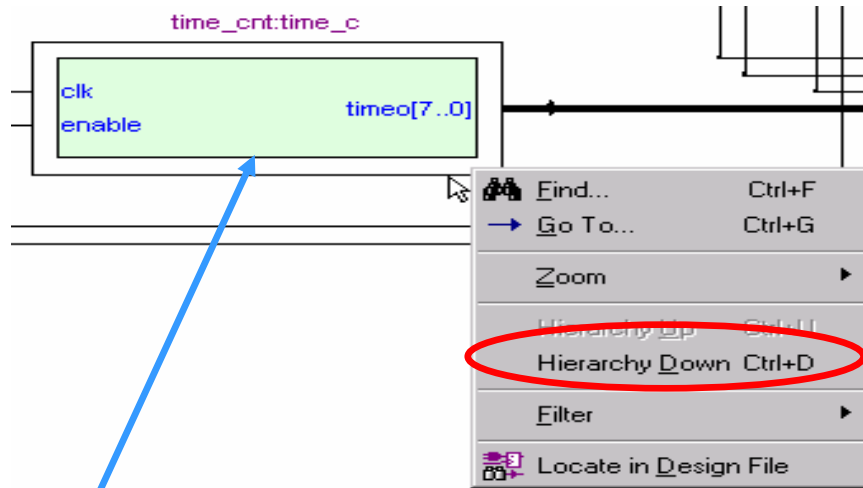
RTL Viewer Bus Grouping
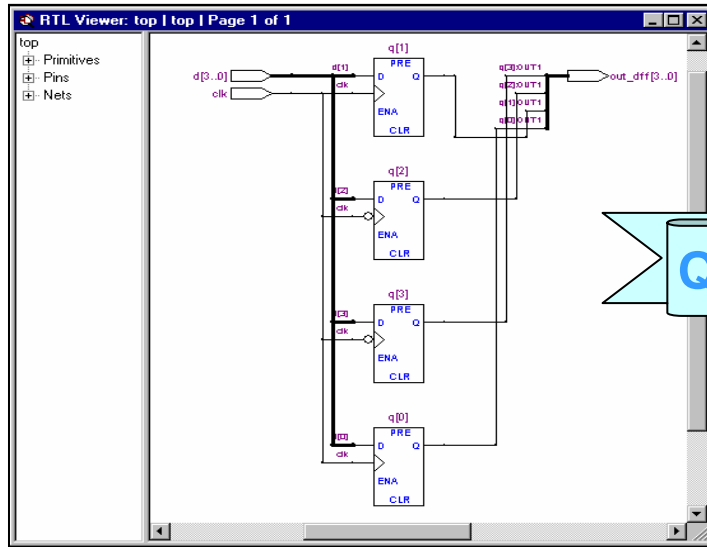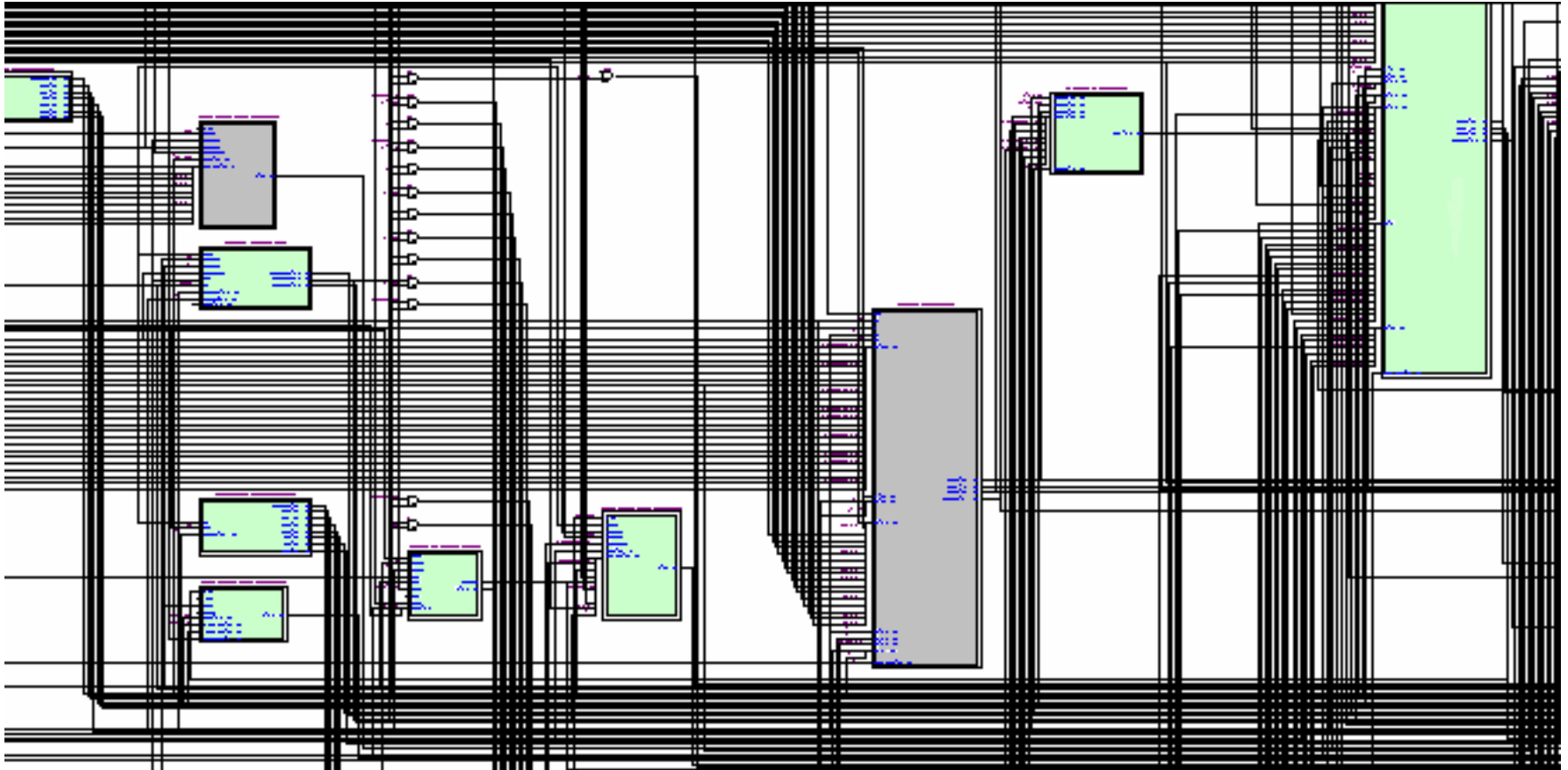

Quartus II 4.0
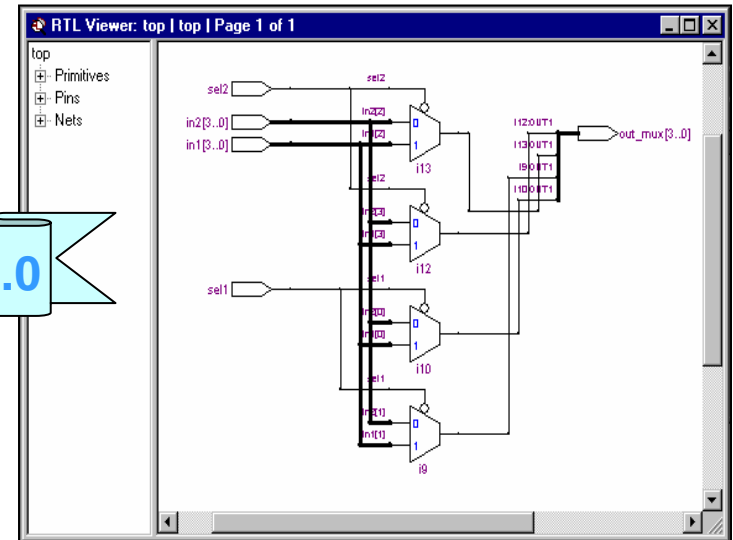
Quartus II 4.1

Instance Coloring

Instance Can Be Analyzed in RTL Viewer
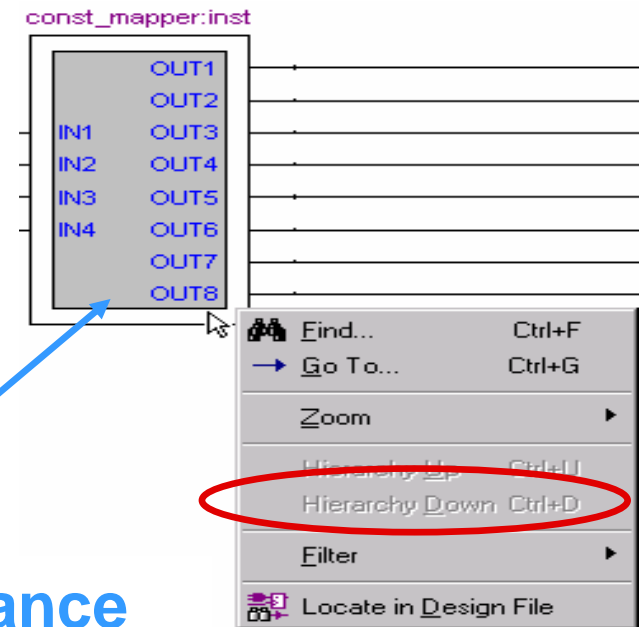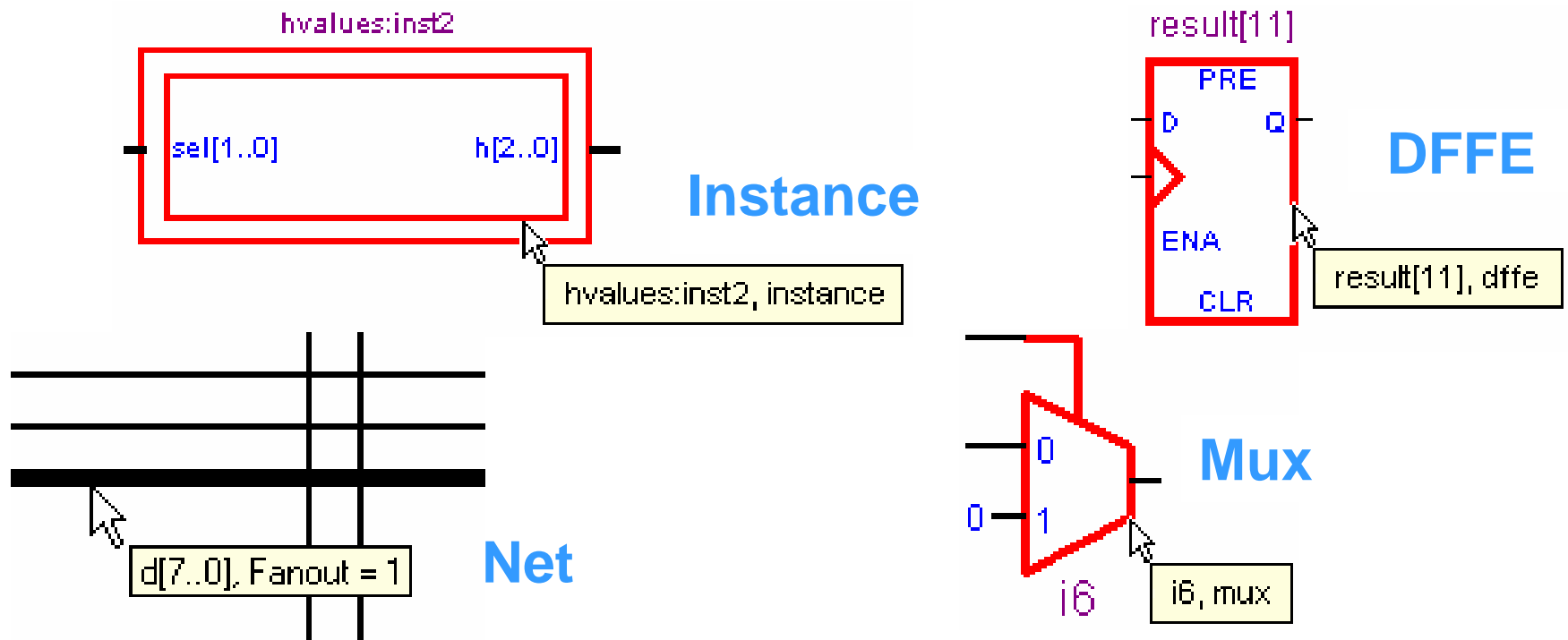
Encrypted Instance Can NOT Be Analyzed in RTL Viewer

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Instance Coloring

■ Easy to See Instances at Lower Zoom Levels

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Tooltips

- Provide Information About Nodes & Nets
- Options for Display Time Under Tools -> Options

Instance

DFFE

Net

Mux

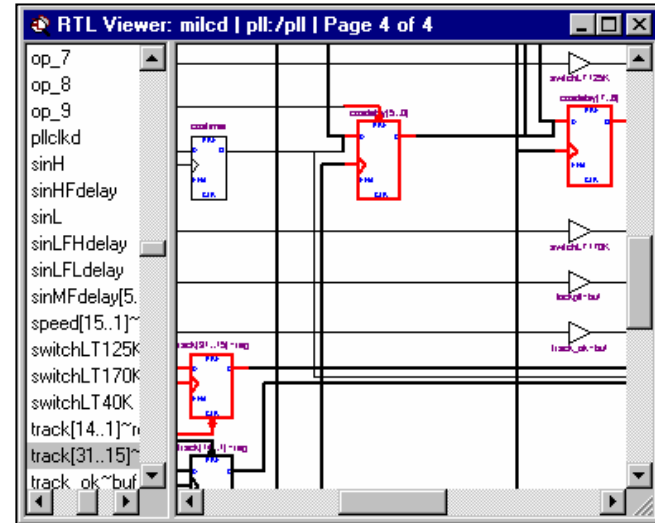- Any Suggestions for Information to Add?

Box Selection & Zooming
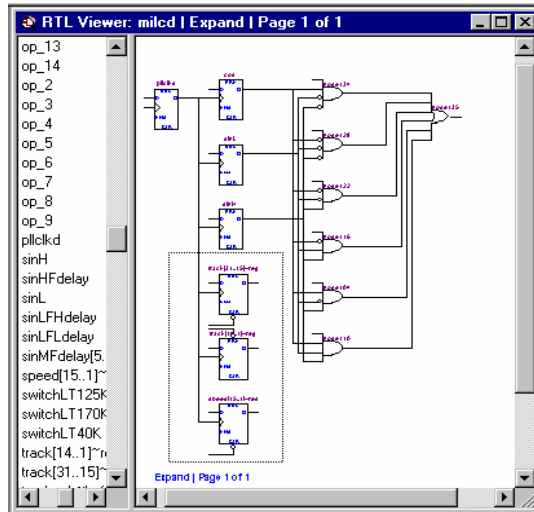
Box Selection

Box Zooming

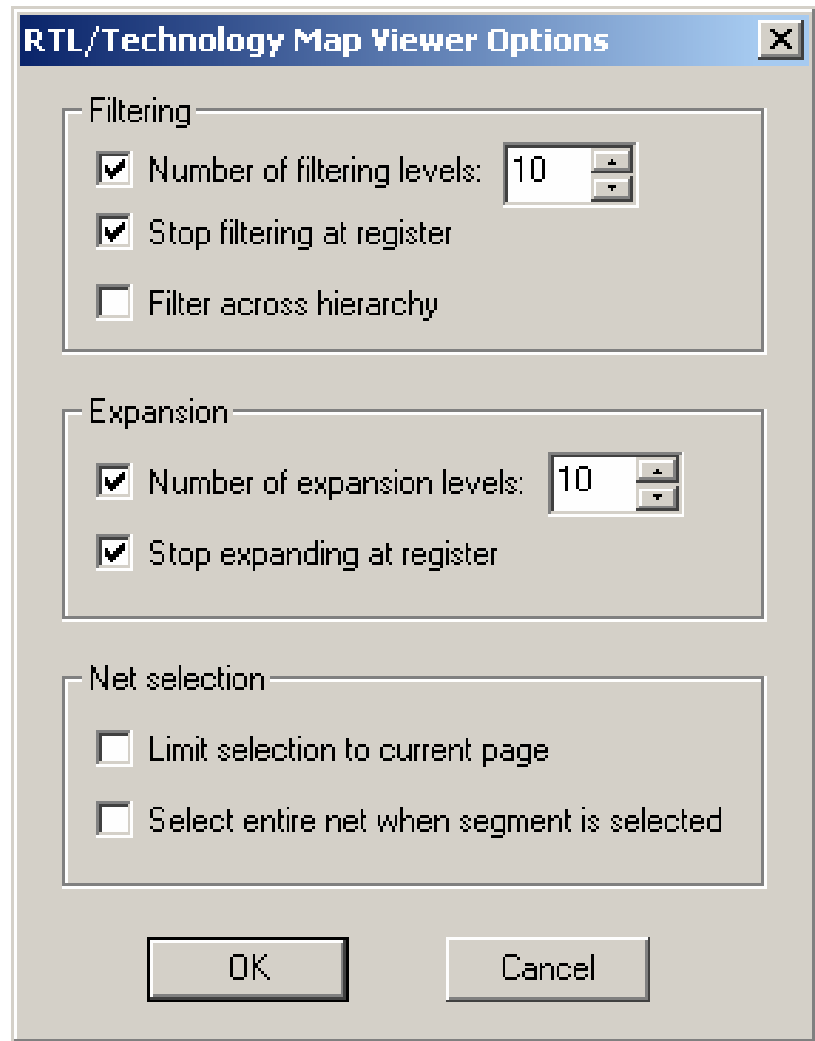© 2004 Altera Corporation
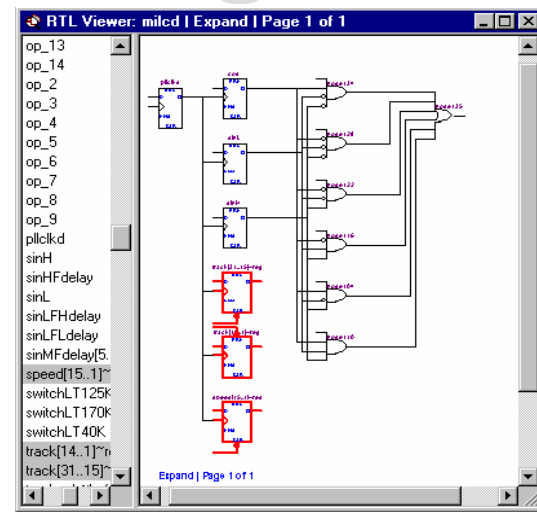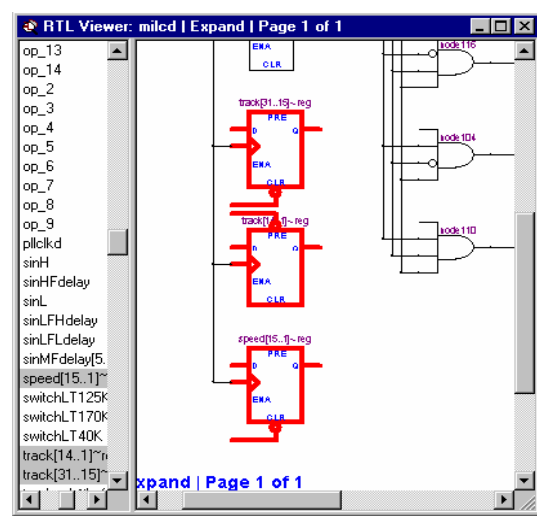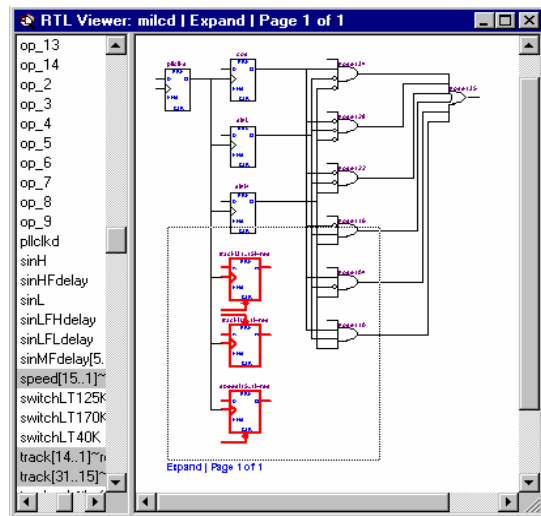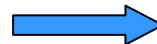
Zoom - Fit Selection in Window
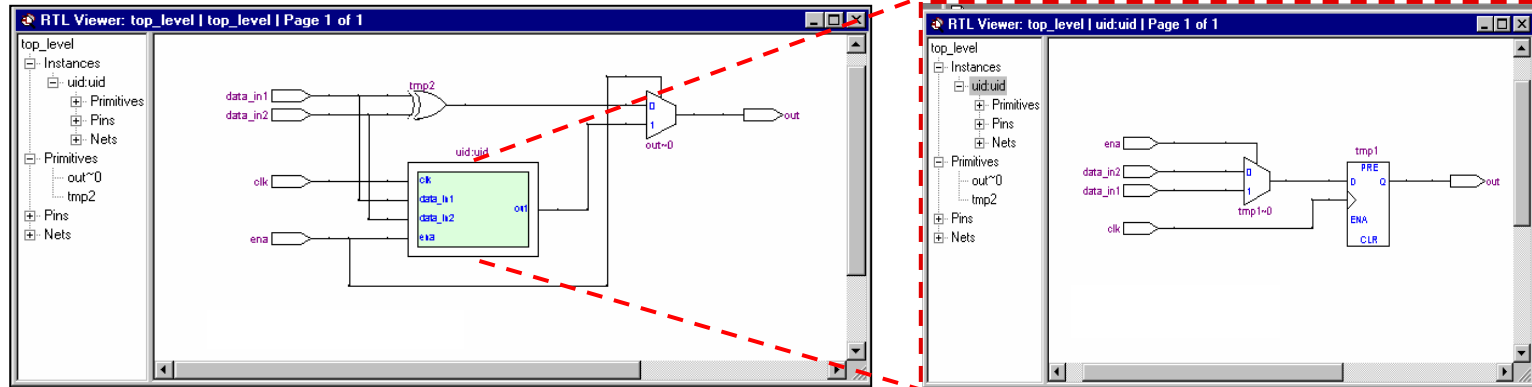
© 2004 Altera Corporation
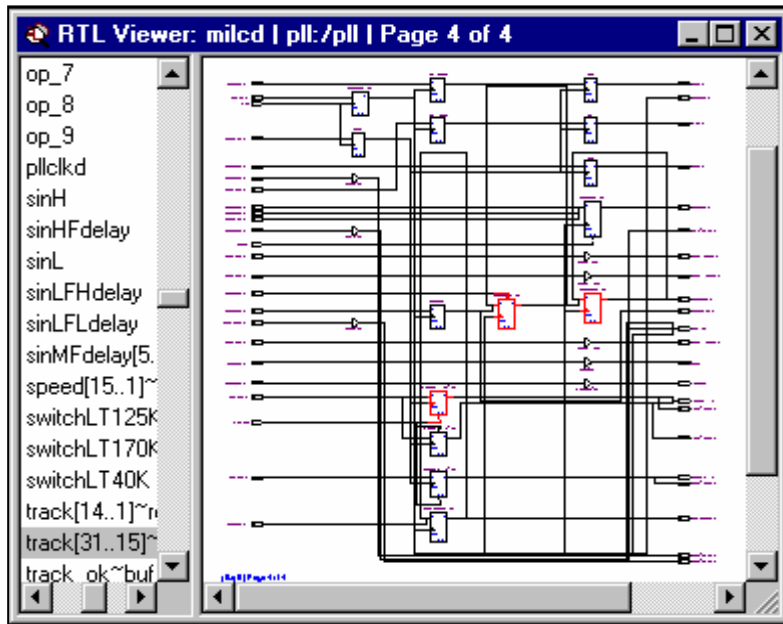
Viewer Options Dialog Box

- **New in 4.1 (May Be Subject to Change)**
- **Accessed from Right-Click in the Viewer**
  - No Need to Go to Tools > Options for Common Options
- **Filtering Options Have Moved Here from Options Menu**

RTL/Technology Map Viewer Options ✕

Filtering
- ☑ Number of filtering levels: [10] ⬍
- ☑ Stop filtering at register
- ☐ Filter across hierarchy

Expansion
- ☑ Number of expansion levels: [10] ⬍
- ☑ Stop expanding at register

Net selection
- ☐ Limit selection to current page
- ☐ Select entire net when segment is selected

[OK]　[Cancel]

Filter Across Hierarchy

Filter Across Hierarchy Turned Off (& Quartus II 4.0)

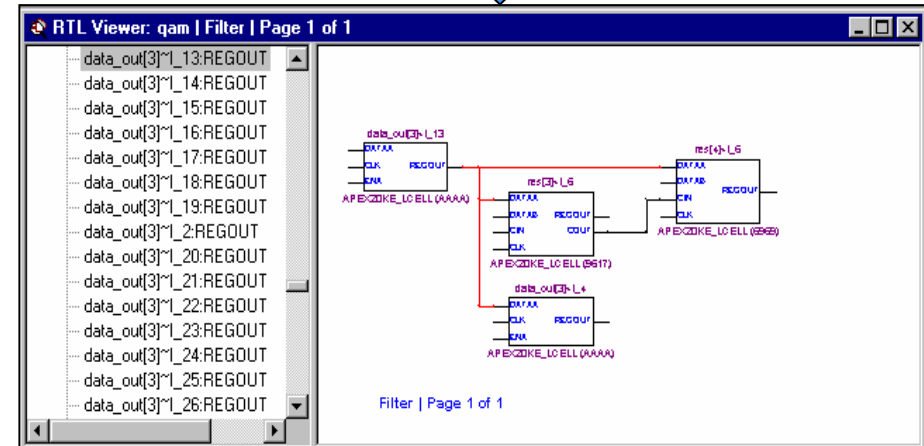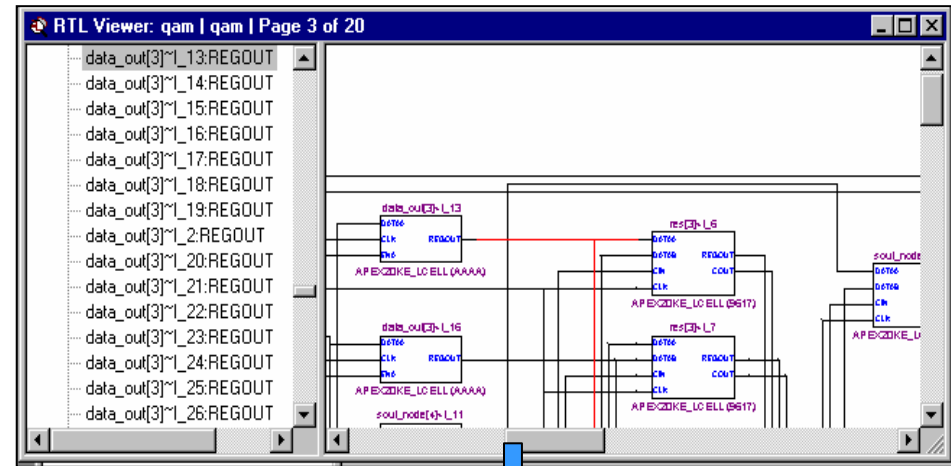**Quartus II 4.1 with Filter Across Hierarchy Turned On**

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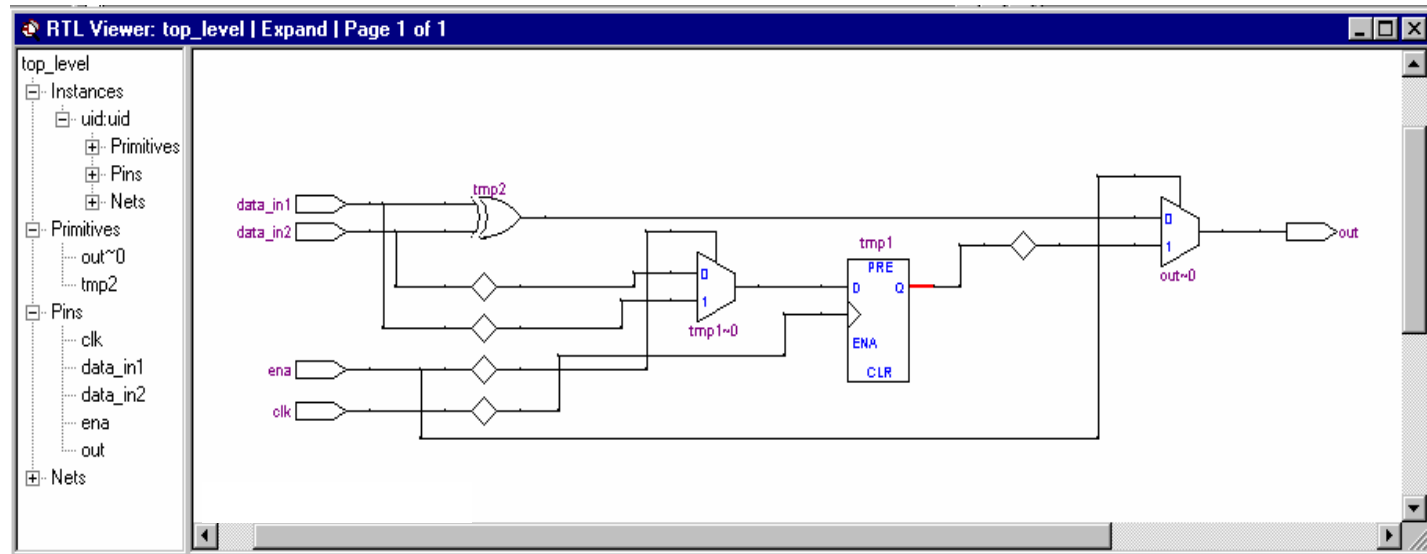
Filter on Selected Nodes & Nets
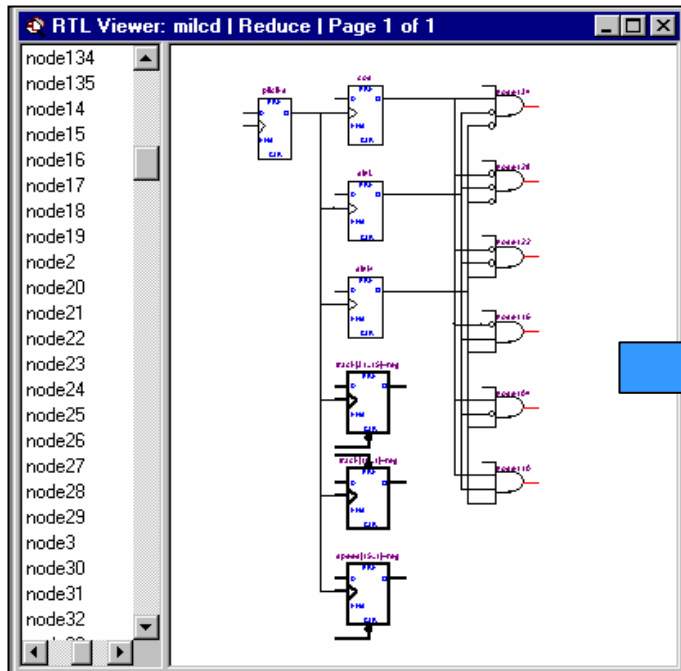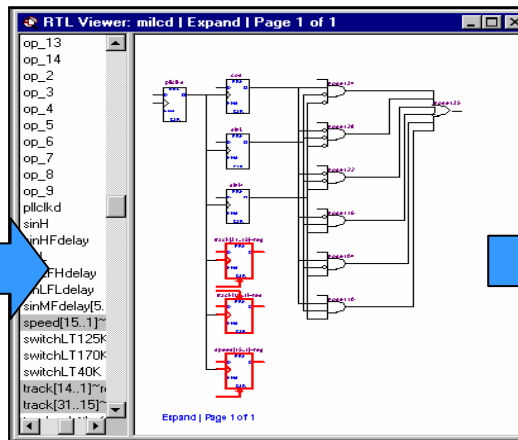
Selected Nodes
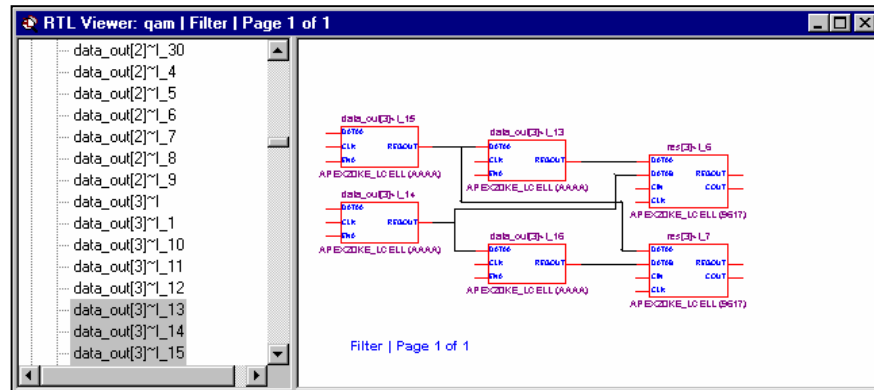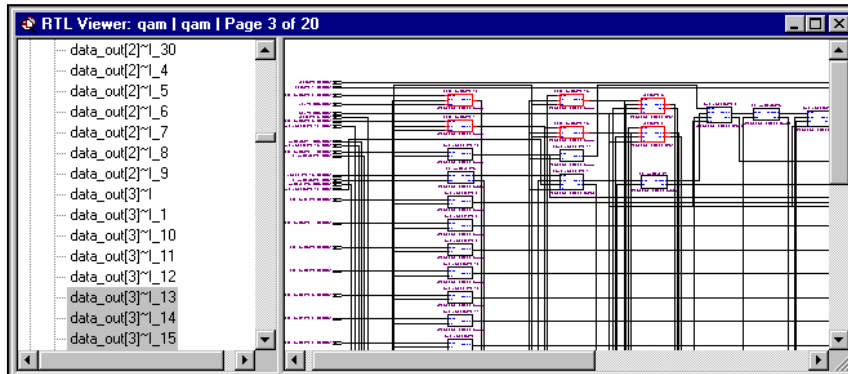
Selected Net
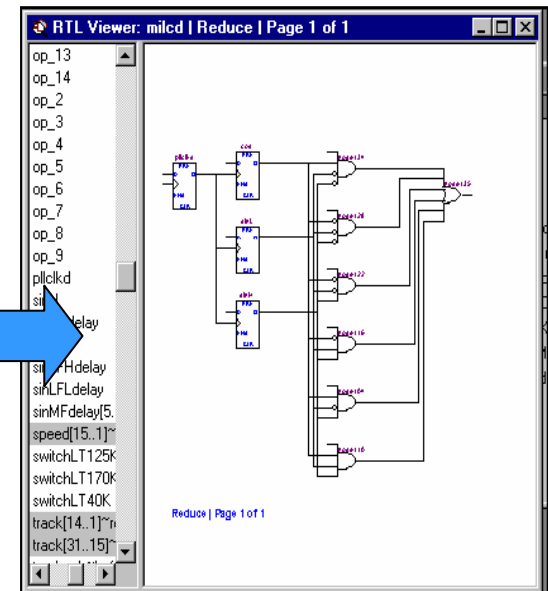
Expand & Reduce Filtered Netlist

■ Add or Remove Logic from Filtered Netlist View
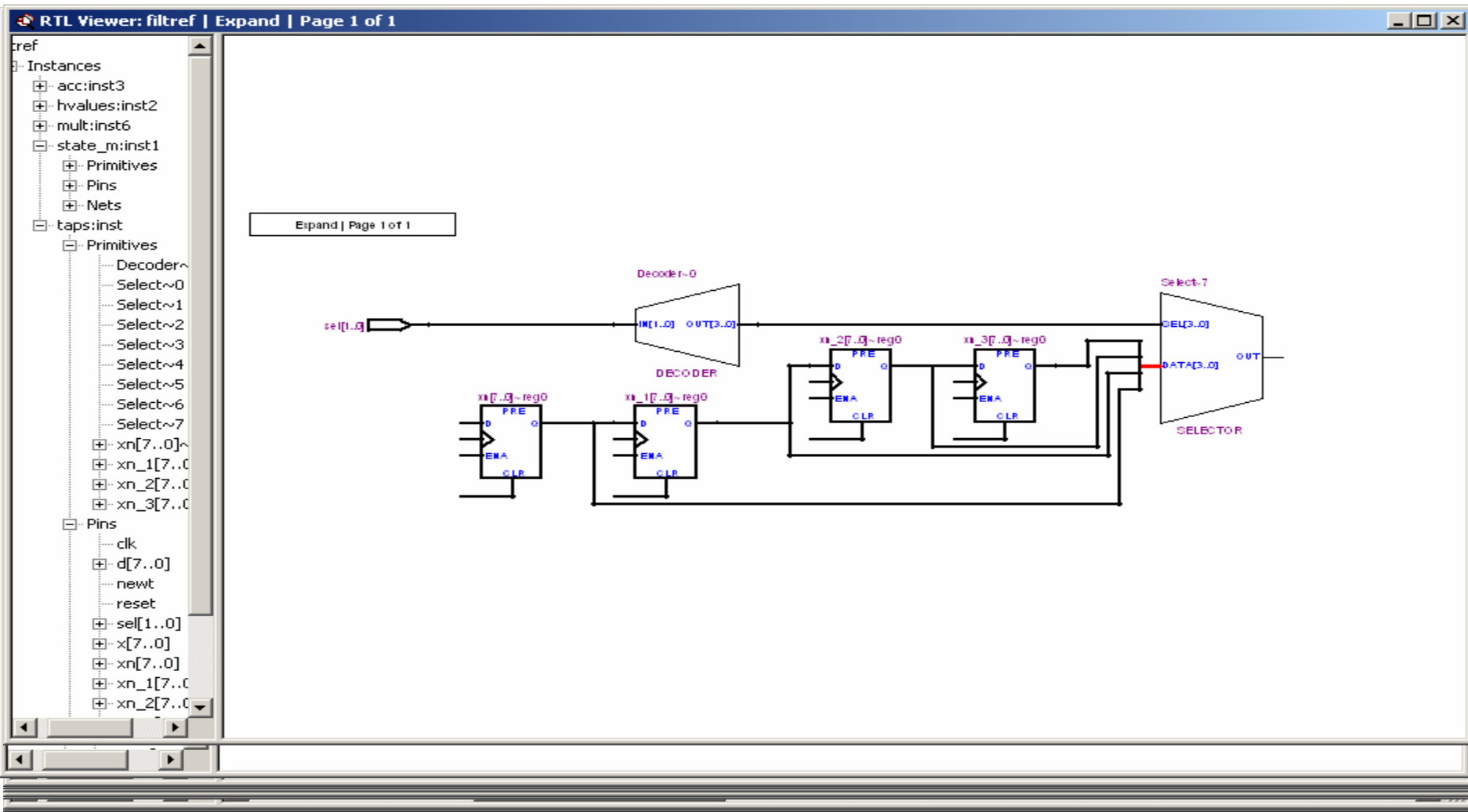

Select AND Gate Port & Choose Expand to add Logic

Select three DFFs & Choose Reduce to Remove Logic

Final Schematic

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Expand & Reduce Filtered Netlist

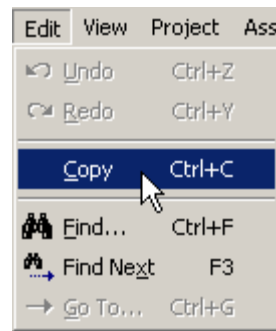© 2004 Altera Corporation

Export & Copy Schematic Image

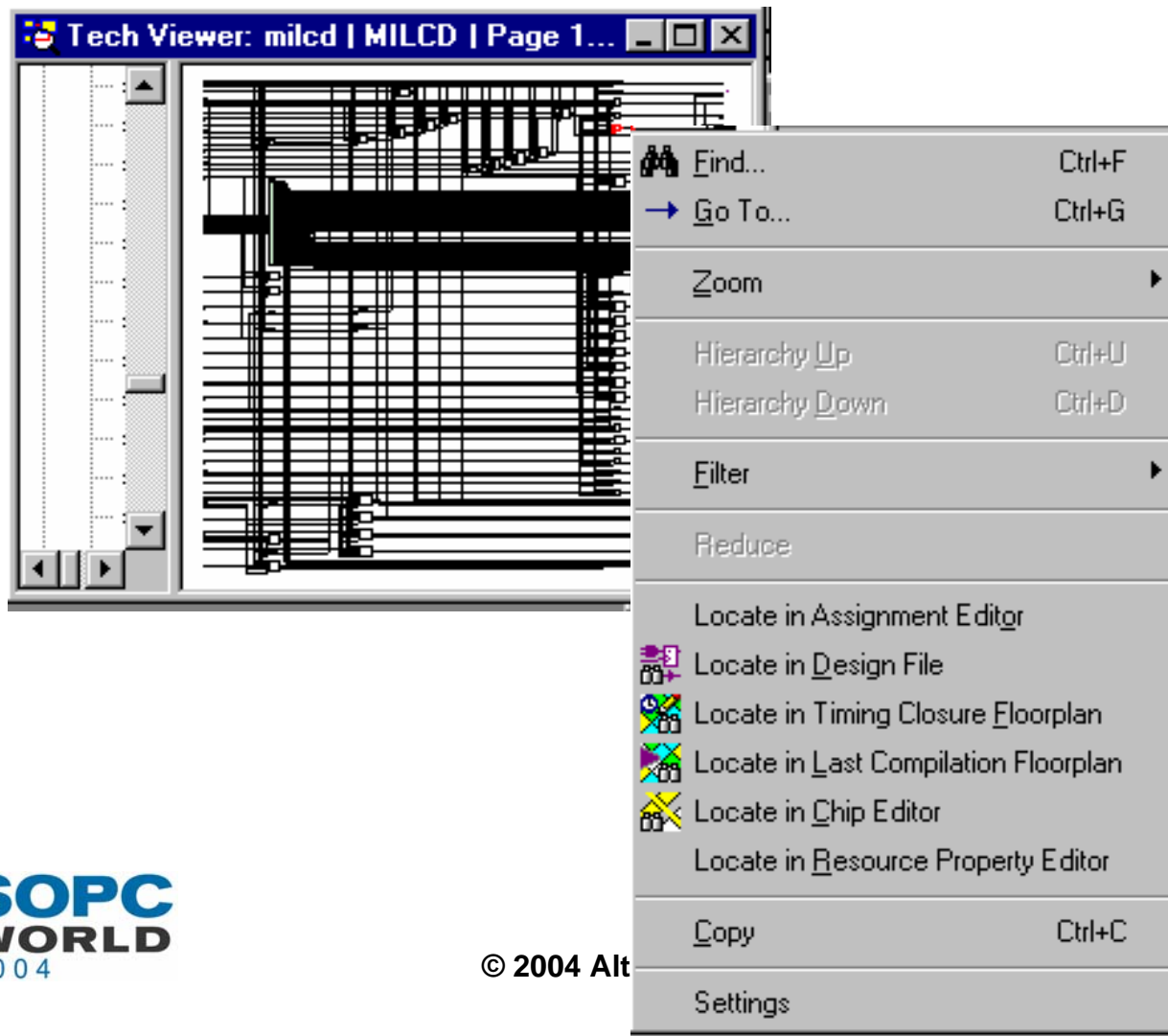■ Useful for Documentation!
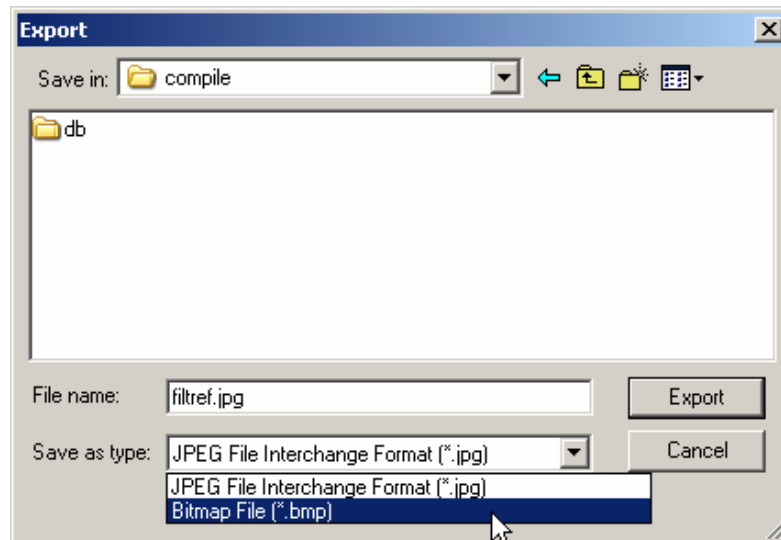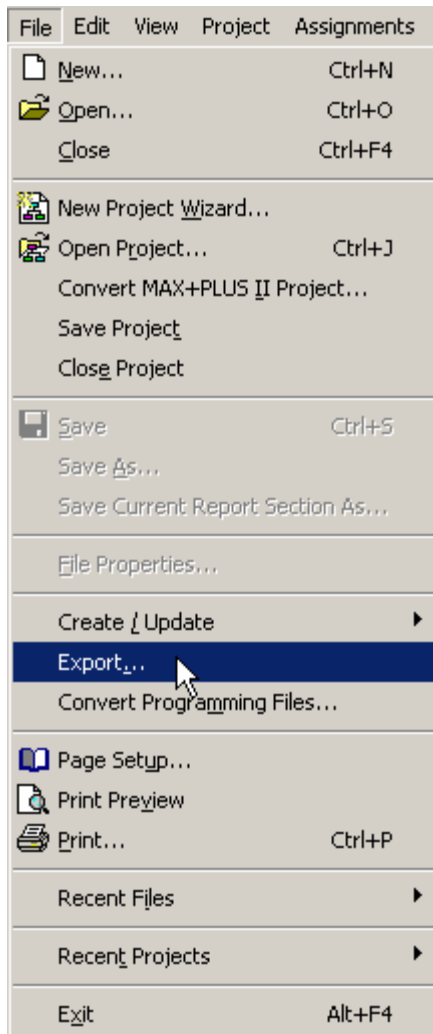
Export Schematic to JPG or BMP File

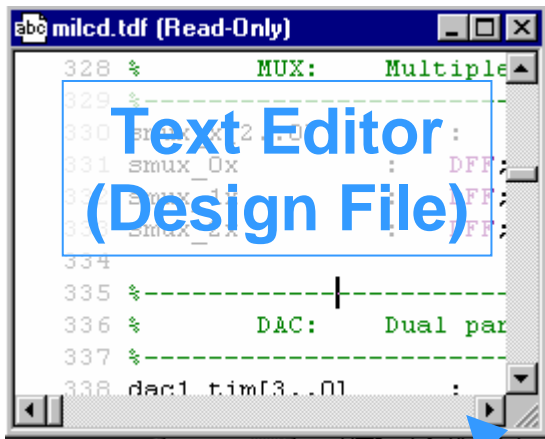**Copy Schematic to Clipboard (Paste to Word, PhotoShop etc.)**

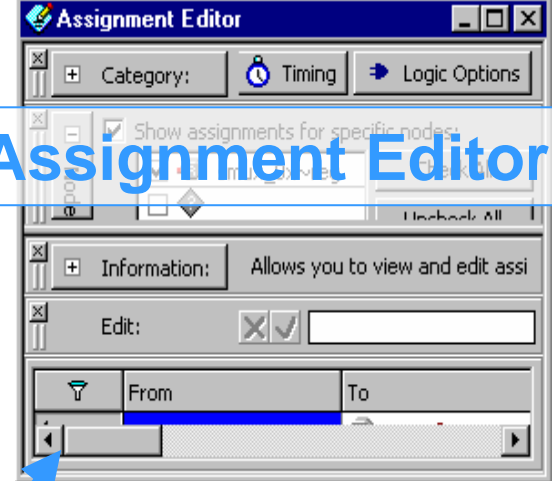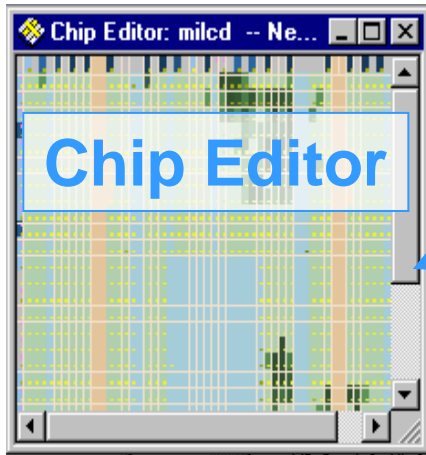# Locate to Other Quartus II Features

■ Select Node(s) and Right-Click
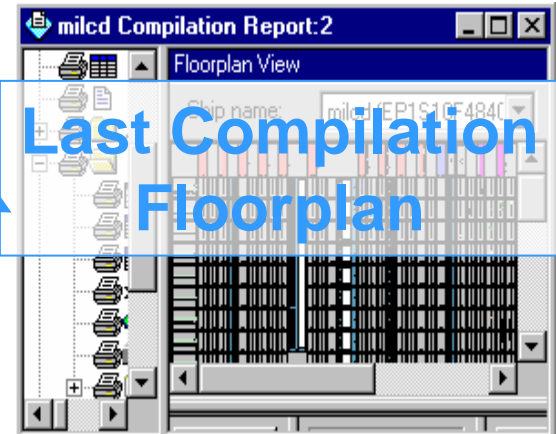
© 2004 Alt

Locate to…

Text Editor (Design File)

milcd.tdf (Read-Only)

```
328  %           MUX:     Multiple
329
330
331  smux_Ox        :        DF
       smux_            FF
       smux_2          FF
334
335  %----------------|
336  %           DAC:     Dual par
337  %----------------
338  dac1_tim[3..0]    :
```

Assignment Editor

Assignment Editor

Category: Timing | Logic Options

Show assignments for specific nodes:

Information: Allows you to view and edit assi

Edit:

From | To

Chip Editor

Chip Editor: milcd -- Ne...

Tech Viewer: milcd | MILCD | Page 1...

Last Compilation Floorplan

milcd Compilation Report:2

Floorplan View

Chip name: milcd (EP1S10F484C

Resource Property Editor

Resource Property Editor

Node name: LC_X17_Y30_N4 -- |MILCD|smux_
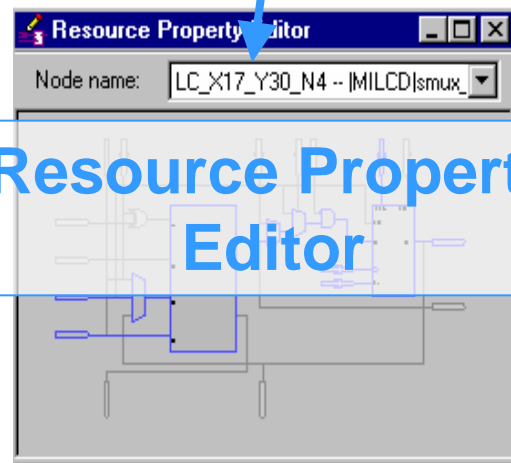
Timing Closure Floorplan
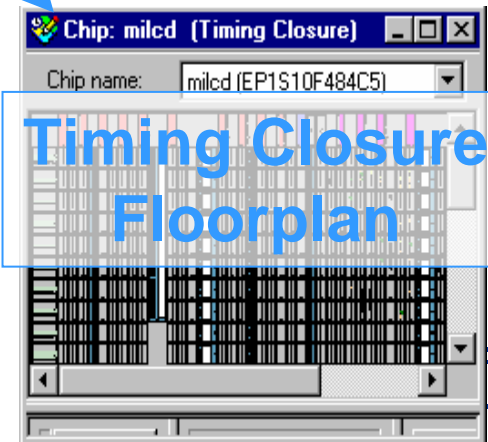
Chip: milcd (Timing Closure)

Chip name: milcd (EP1S10F484C5)

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Agenda

What is the RTL Viewer and Why Use It?

Feature Overview & User Interface Details

Technology Map Viewer

Enhancements & References

Other Enhancements

- Maintains Zoom Across Pages When Traversing Schematic Using Connectors
- Highlighted Net is "Brought to Front" of Schematic so it is not Hidden in Crowded Netlists
- Other SPRs and Suggestions from FAEs
    - Enhancement Requests
    - Cases Where Placement in Viewer Was Not Optimal

Provide More Feedback on What You and Your Customers Want to See in the Viewers!

References

- Quartus II Handbook: [Analyzing Designs with the Quartus II RTL Viewer & Technology Map Viewer](#)

- [On-Line Demos](#): Using the RTL Viewer and Technology Map Viewer to Check Synthesis and Fitting Results

What is ONLY supported in Technology Mapper?

(1) expand and reduce logic in schematic

(2) display timing delay information and timing paths

(3) filter unrelated nodes to isolate selected design elements

(4) specify the number of nodes and ports you want to display per page