The Ultimate Guide to Design Productivity

Design Productivity—Your Competitive Advantage

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Move Faster, Get Optimized, Innovate More

What Can You Do…

to Provide Competitive Advantage?

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What Productivity Means

- Do more with less: Develop more competitive products with fewer resources
- Reuse and share design intellectual property (IP) across projects
- Enable design teams in different geographies to work on the same project
- Lower risk of design errors
- Efficiently adapt to market-focused product change requests
- Enable focus on value-add core competencies

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TIP #1: *Lower Your Risk*

- Look beyond the silicon—all systems consists of hardware and software
- Tools and design methodology improve your productivity
- Supporting IP portfolio should be broad and current to market requirements
- Ensure your vendors can support you from design concept to volume production

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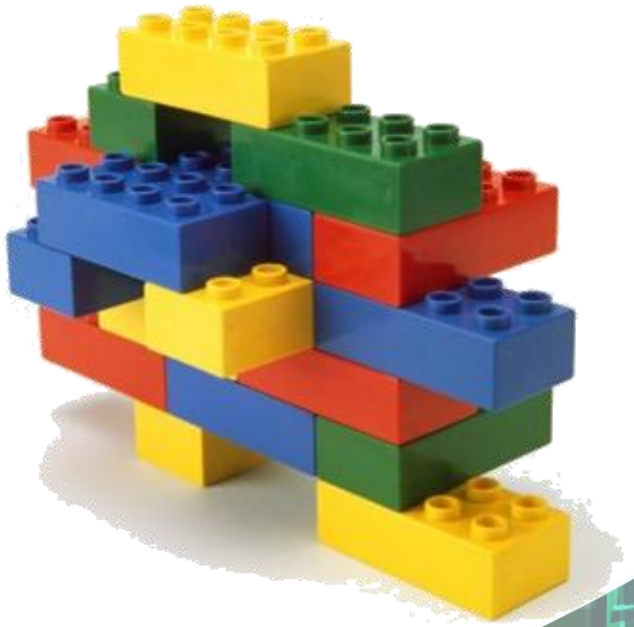
TIP #2: *Look for Flexibility, Scalability and Reusability*

- Add new features as market requirements change
- Reuse designs and IP across different products and teams
- Avoid risk of product obsolescence
- Scale from prototyping to production volumes



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TIP #3: *Think "TCO" – Total Cost of Ownership*

- Evaluate both product cost and development cost
- Remember the additional cost of tools, IP, and design time
- Estimate the cost of respins and lost revenue, if product launch is delayed
- Consider cost of going from prototype to production

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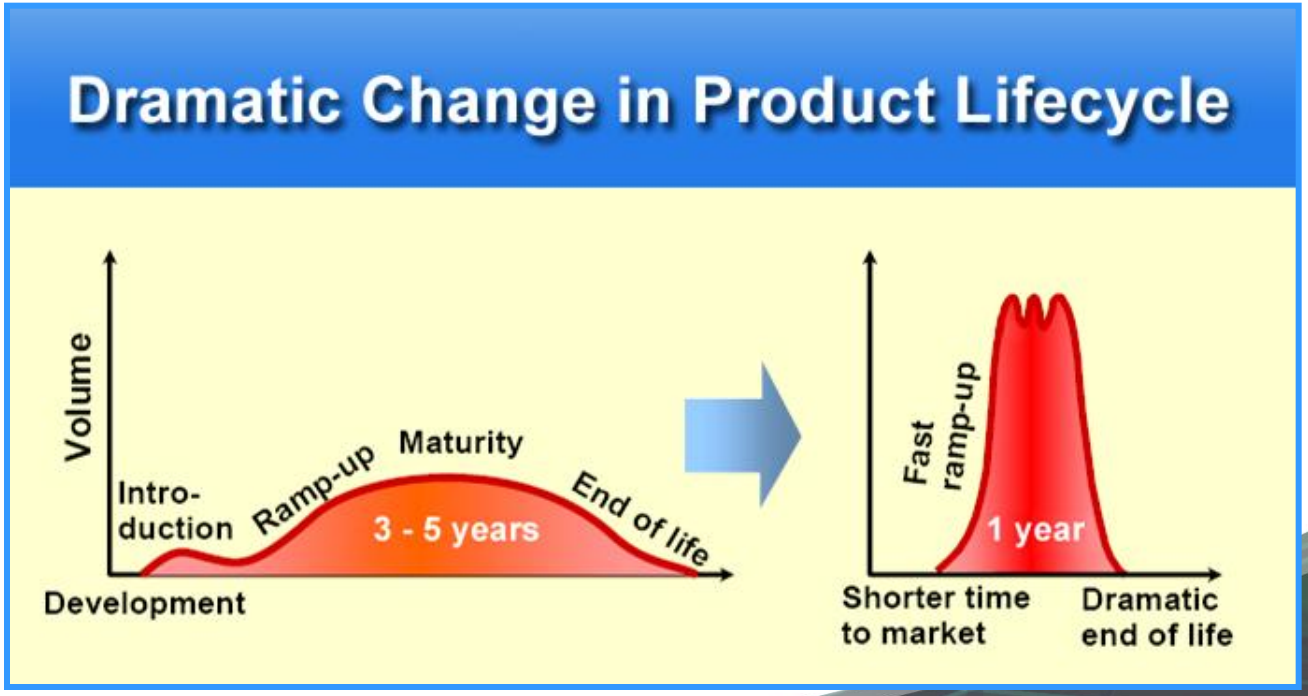
TIP #4. *Think of Time IN Market and Time TO Market*

Increased Competition Makes Most Markets Behave Like the Consumer Market – Time in Market Keeps Shrinking



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TIP #5: *Programmable Solutions Are the Ultimate Productivity Tool*

- Maximum flexibility and low design cost
- No risk of re-spins or obsolescence
- Change the product throughout its lifetime
- Low to no cost design software
- Broad portfolio of IP
- Best prototype to production solution

Spend Less. Do More. Get There First.

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Design With Confidence: Stratix III FPGAs

The Lowest-Power High-Performance FPGAs

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Product Portfolio Today

MAX II | Cyclone II | Stratix II | HardCopy II | Nios II

CPLDs

Low-Cost FPGAs

High-end FPGAs
Including Transceiver Option

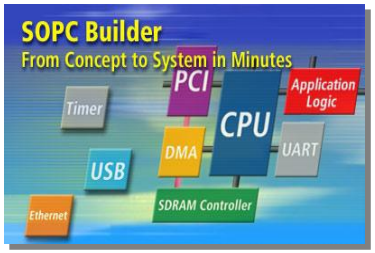
Structured ASICs

Embedded Soft Processors

QUARTUS II

Design Software

Intellectual Property (IP)



Support Tools

Development Kits

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Stratix III FPGA Key Innovations

- Industry's first "Programmable Power Technology"
  - 50% lower power than 90-nm FPGAs at the same performance
- Architecture—2nd-generation ALM logic structure
  - Highest density: 338K logic elements
  - Most efficient interconnect: fastest performance and highest utilization
  - Highest memory and register capacity: 17-Mbit memory and 270K registers
  - Fastest DSP capacity: 896 18X18 multipliers @ 550 MHz

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Stratix III FPGA Key Innovations

- Highest-performance interface capability
  - Modular bank flexibility
  - Industry-leading signal integrity
- Quartus® II design software is industry leader in productivity and performance
  - PowerPlay: Automated implementation of high-performance and lowest-power designs
  - TimeQuest: ASIC-quality timing analysis
    - Synopsys Design Constraint (SDC)-based for FPGAs
  - Team-based design
  - Incremental compilation—fastest compile times

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Industry's First Complete Power-Efficient Technology

Stratix® III Power Reduction Technique	Lower Static Power	Lower Dynamic Power
Silicon Process Optimizations	✓	✓
Programmable Power Technology	✓	✓
Selectable Core Voltage (0.9 V or 1.1 V)	✓	✓
Quartus II PowerPlay Power Optimization	✓	✓

Stratix III Devices are the Lowest-Power High-Performance FPGAs

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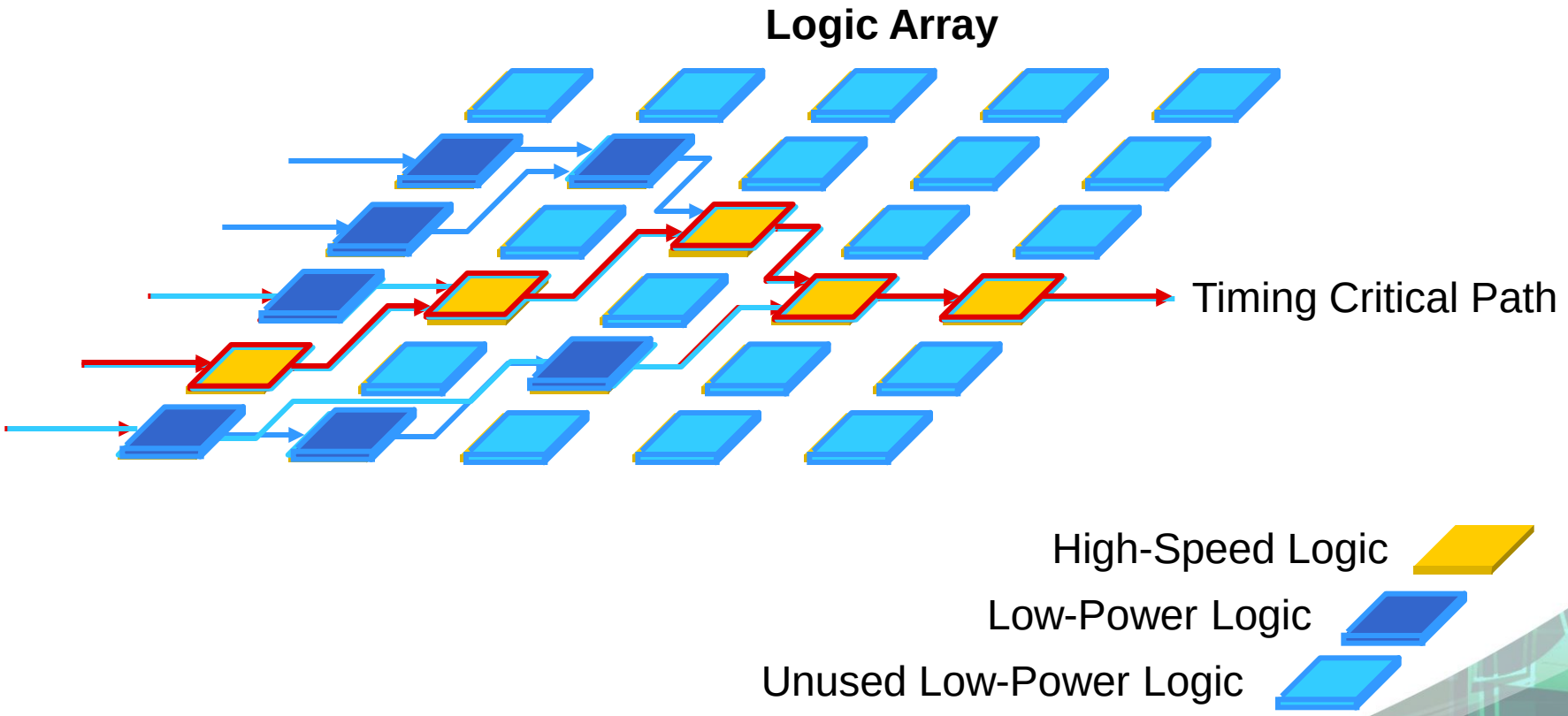
Programmable Power Technology



Performance Where You Need It,
Lowest Power Everywhere Else

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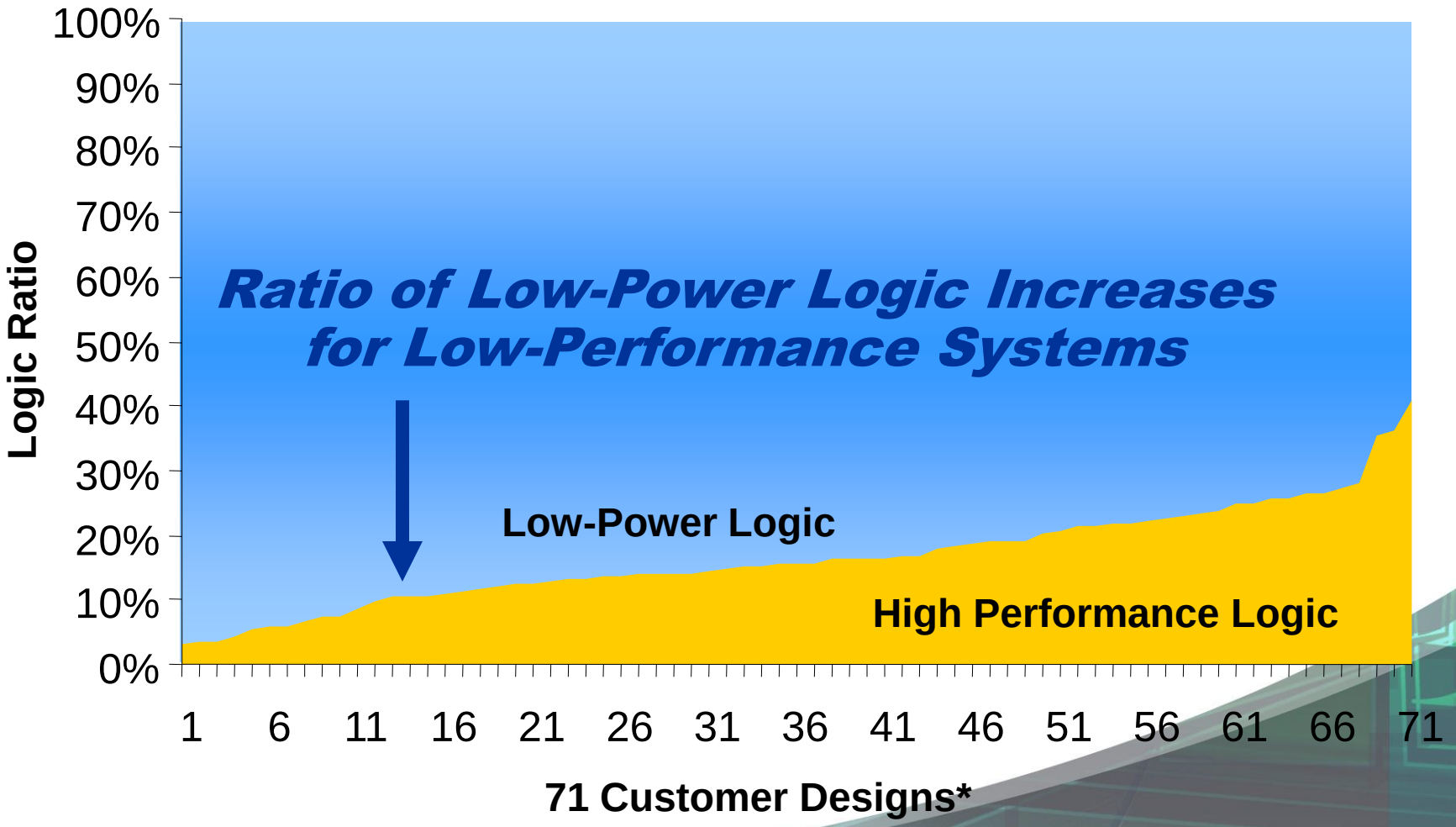
High-Speed vs. Low-Power Logic Ratio



*All designs compiled for maximum performance

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Stratix III Power vs. Performance

Design Clock Frequency	Change in Total Power From Stratix II Devices to Stratix III Devices*
Parity	-50%
+25%	-25%

* Based on average resource utilization from customer design database

Dramatically Reduce Power and Automate Power Management With Stratix III FPGAs

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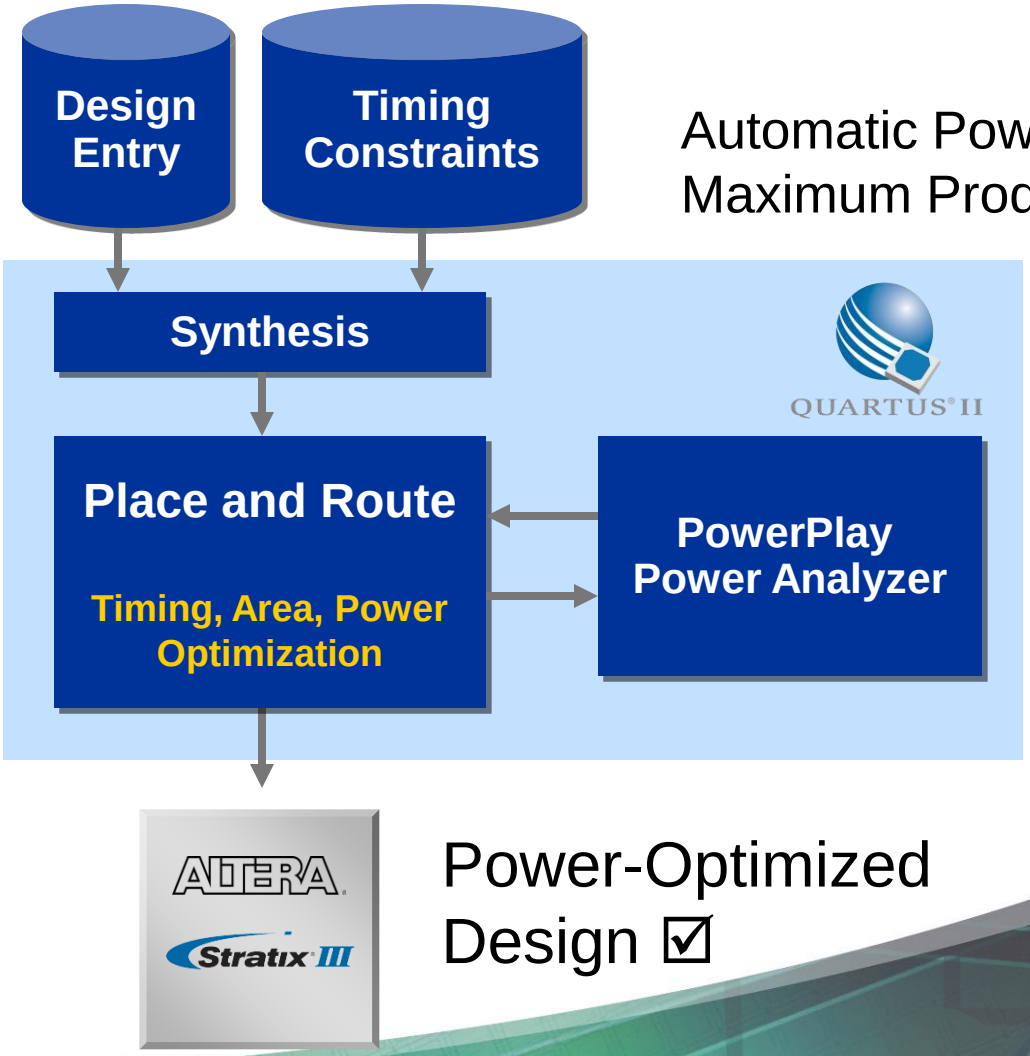
Quartus II Design Flow



Automatic Power Reduction for Maximum Productivity

Power-Optimized Design ☑

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Highest-Performance DSP

- Up to 896 18-bit x 18-bit multipliers performing @ 550 MHz
- Variable bit-width support

Device	Multipliers					
	9x9	12x12	18x18	36x36	18x18 Complex	18x18 Sum of Multipliers
EP3SE110	896	672	448	224	224	896

- DSP blocks cascade modes to maximize overall performance
- Digital signal processing (DSP)-optimized logic and memory fabric
  - MLAB for tapped delay lines
  - Fast 3-input adder in ALM

Stratix III I/O Connectivity

- Increased efficiency and flexibility: 24 banks
- High performance:
  - 1.25-Gbps LVDS
  - 800 Mbps DDR3
- Excellent signal integrity

Meet Today's Interconnect Design Challenges With Stratix III I/Os

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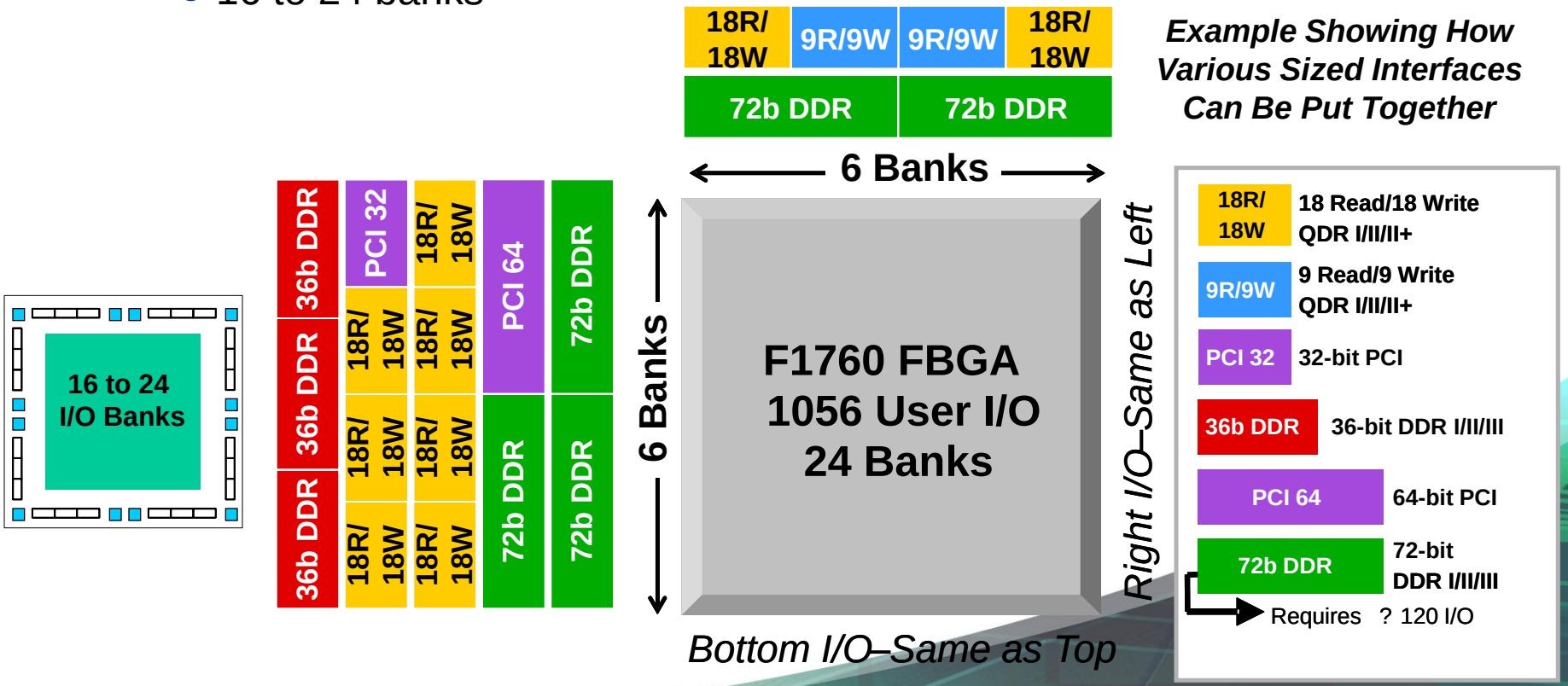
Efficient Modular I/O Banks

- New modular bank structure
  - Many small I/O banks
    - 24, 32, 36, 40, or 48 user I/Os per bank
    - 16 to 24 banks



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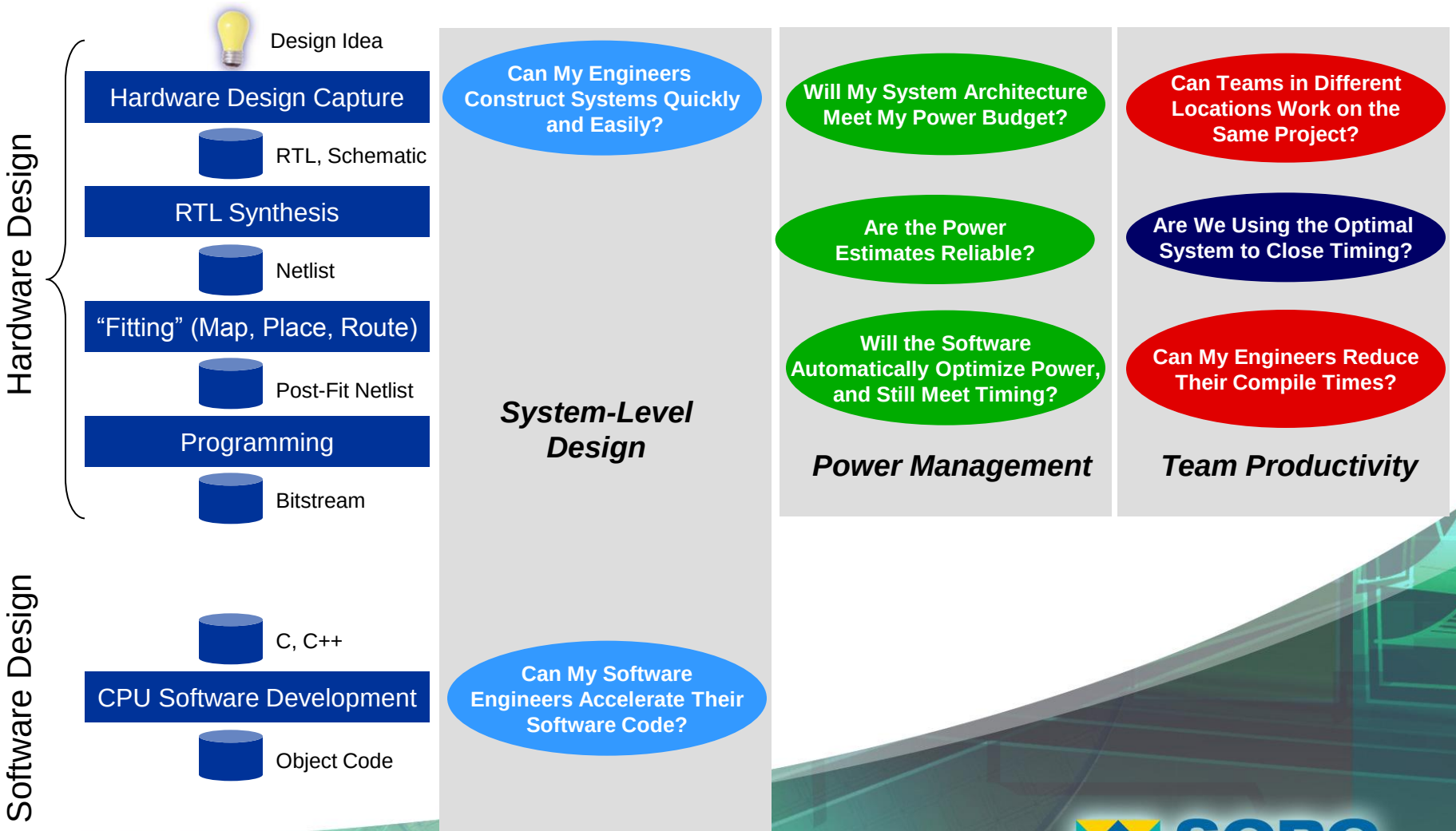
Key Productivity Challenges



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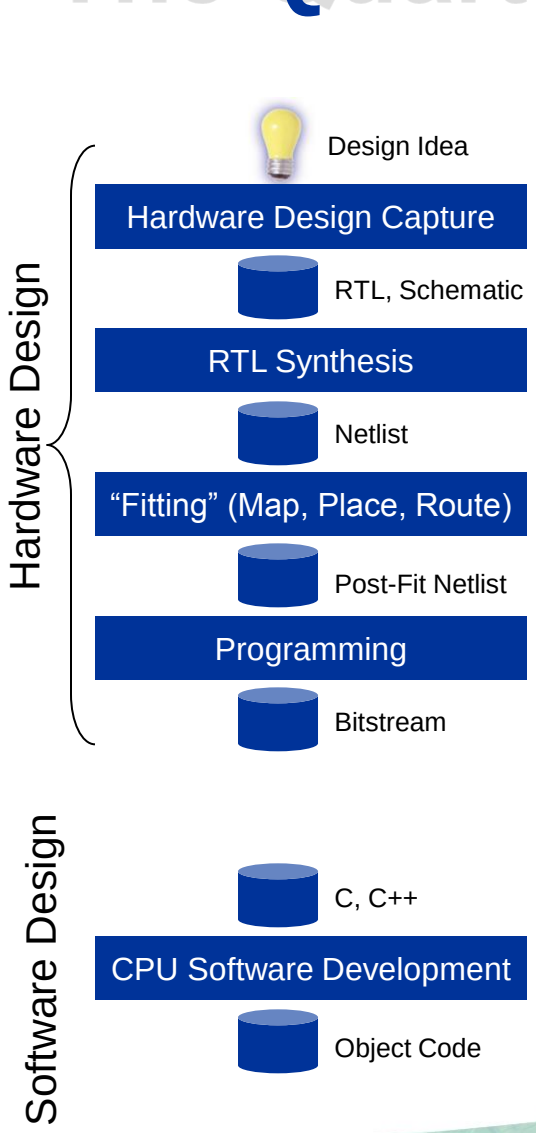
The Quartus II Software Advantage



Can My Engineers Construct Systems Quickly and Easily?

SOPC Builder

System-Level Design

Will My System Architecture Meet My Power Budget?

Are The Power Estimates Reliable?

Will the Software Automatically Optimize Power, and Still Meet Timing?

Power Management

PowerPlay

Team-Based Design and Incremental Compile

Can Teams in Different Locations Work on the Same Project?

TimeQuest

Are We Using The Optimal System to Close Timing?

Can My Engineers Reduce Their Compile Times?

Team Productivity

Nios® II C2H

Can My Software Engineers Accelerate Their Software Code?

Unique Quartus II Productivity Technologies Save Weeks to Months of Engineering Effort

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Stratix III High-End FPGAs

General Applications

- Balanced logic, memory, and multipliers

Memory- and DSP-Rich Applications

- More memory and multipliers per logic
- Ideal for wireless, medical imaging, and military applications

High-Interface Bandwidth Applications

- Integrated multigigabit transceivers
- Ideal for telecom, broadcast, test equipment, computer, and storage applications

High-Volume Applications

- Low cost, higher performance, and lower power
- Seamless migration from Stratix III FPGAs

Application-Optimized Solutions With Cost-Reduction Path

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Stratix III—Your Productivity Edge

- Lowers risk
  - Lowest power, high performance FPGA
  - Proven architecture
  - Track record for on-time delivery
- Flexible, scalable, and reusable
  - Most comprehensive development tool set: Quartus II software
  - Broad IP portfolio
  - Team-based design

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Stratix III—Your Productivity Edge

- Lowest total cost of ownership (TCO)
  - Lowest cost of development tools, IP, and programmable silicon
  - Comprehensive worldwide training and technical support
  - Industry's only complete prototype-to-production solution
- Lengthens time *in* market
  - FPGAs allow early market introduction and in-field upgrades to meet market demands
  - Migrate from FPGAs to structured ASICs for volume, then replace with compatible FPGAs to add features and standards, while staying in market

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THANK YOU
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