

nbit_adder: adderx

GENERIC MAP (x => 8)

PORT MAP (AddSubR: G, H: M, CarryIn: 0)

multiplexer: mux2to3

GENERIC MAP (x => 1)

PORT MAP (A: 0, Z: 0, S: 0, G: 0)

AddSubR_n <= (OTHERS => 0)

Managing Technology Risk in 65 nm and Beyond

Expected Benefits of Semiconductor Process Advances



Die Shrinkage



Lower Cost

Higher Performance

Impact of Semiconductor Product Choices

- What features and capabilities to include
- Process maturity
- Design-for-manufacturability
- Device check-out procedures
- Foundry partner



- Product delivery (on-schedule vs. late)
- Product availability (improving yields vs. poor yields)
- Product quality and reliability

Altera Meets Rollout Commitments

	Altera® Device Family	First Prototypes	Months From First Prototypes to Production	Months Until All Devices Available
130 nm	Cyclone® FPGAs	December 2002	3	4
	Stratix® FPGAs	May 2002	5	10
	Stratix GX FPGAs	January 2003	10	7
90 nm	Cyclone II FPGAs	January 2005	3	7
	Stratix II FPGAs	June 2004	6	8
	Stratix II GX FPGAs	March 2006	8	N/A

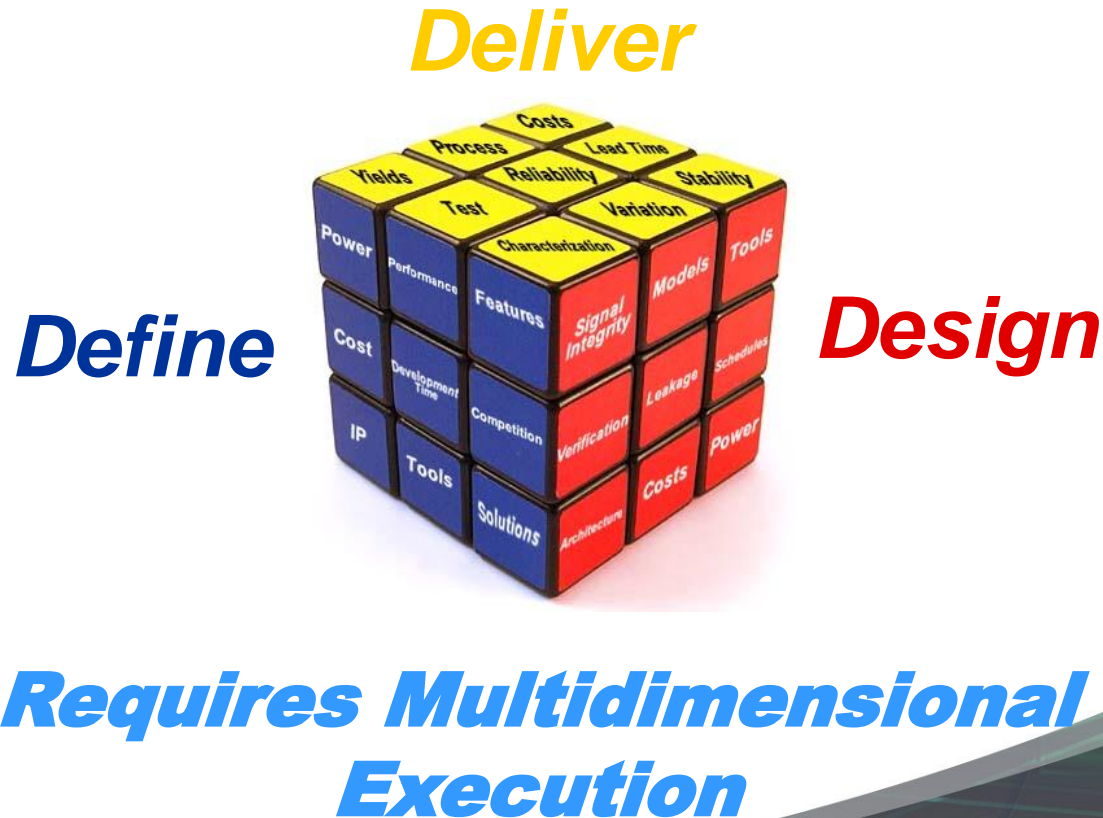
***The Right Technology Choices Deliver
Predictable, Timely Results***

***The Wrong Choices Can Result in Delayed Rollouts,
Limited Availability, and Product Recalls***

How Does Altera Consistently Deliver?

What Really Matters to Altera's Customers

- Increased productivity and risk reduction



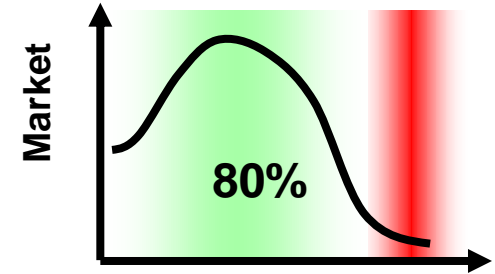
Altera's Strategies for Delivering New Products

1. Precise investments in feature and capabilities
 - Intense research required to determine the right feature set that satisfies customer needs **and** results in a successful product

Precise Product Investment in Features and Capabilities

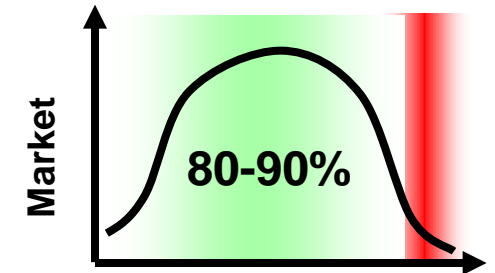
Core Performance

- 20% designs above 250-MHz core performance
- “More performance is always better”
- Large cost and power penalties



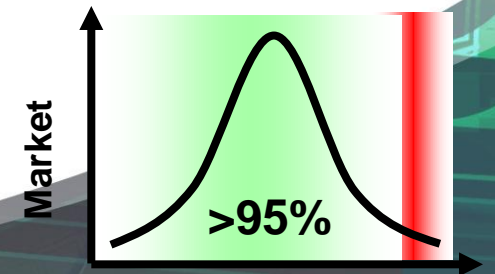
Memory Speed

- To achieve additional 10-20% market in performance means...
- Additional cost 30-40%
- Additional risks with signal integrity

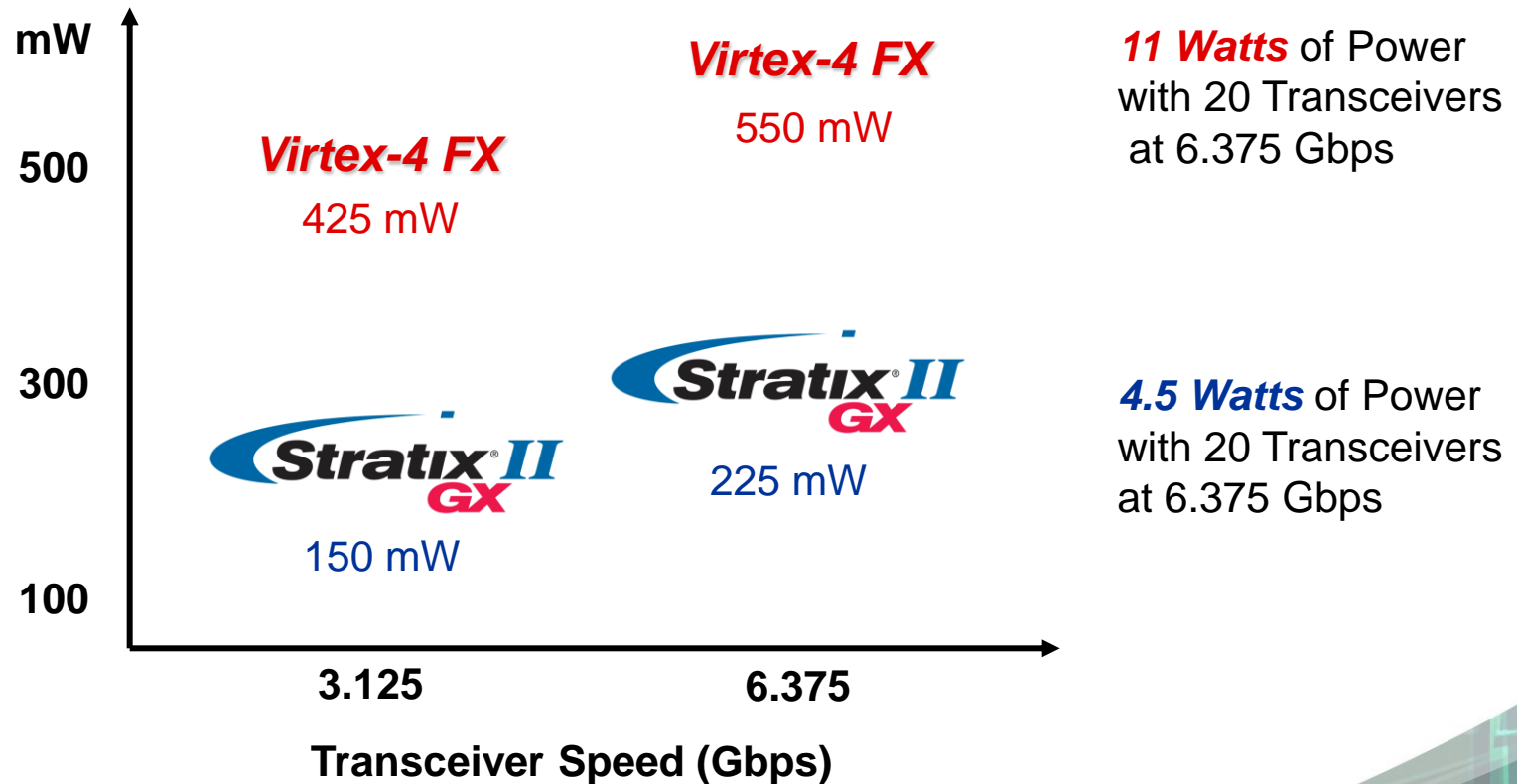


Serial Interface

- > 95% FPGA 155 MHz to 6.5 GHz
- Additional 5% carries risk, cost, and power penalties



Aggressiveness Is Not Free

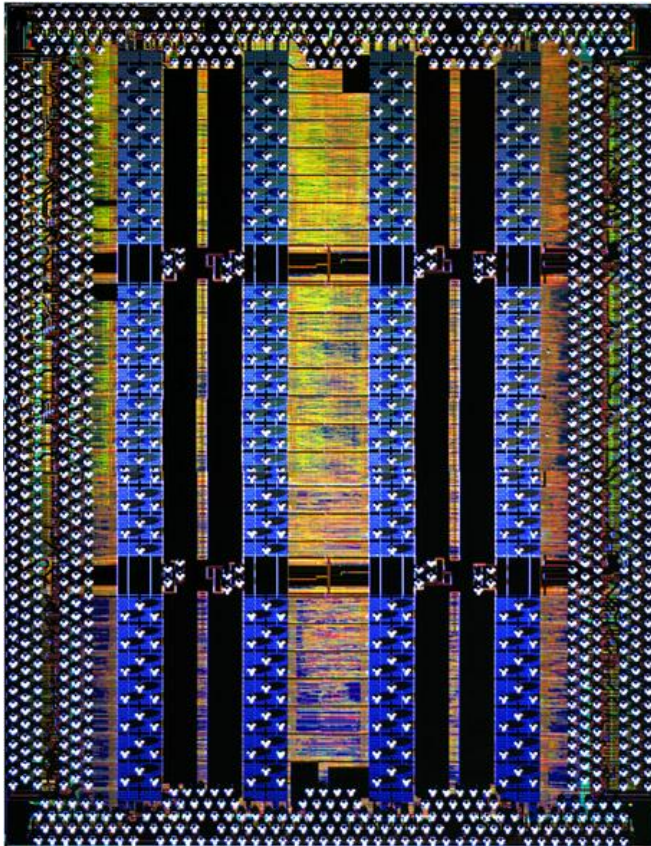


***Benefit of Band-Optimizing Technology
for 622 Mbps – 6.375 Gbps***

Altera's Strategies for Delivering New Products

1. Precise investment in features and capabilities
2. Industry's most comprehensive test chip program
 - Early collaboration on process development and design verification enables reliable new product delivery

Industry's Most Comprehensive Test Chip Plan



Altera Test Chips

Early Technology Assessment

Feasibility Testing

Circuit and Feature Validation

Routing Structure Confirmation

Architectural Verification

Design Optimization and
Refinement

Altera's Eleven 65-nm Test Chips

Test Chips	Tape Out
TC1	Q2 2003
TC2	Q3 2004
TC3A	Q2 2005
TC3B	Q2 2005
TC4	Q3 2005
TC5A	Q3 2005
TC5B	Q3 2005
TC6A	Q4 2005
TC6B	Q4 2005
TC7	Q1 2006
TC8	Q2 2006

***Comprehensive Test Chip Program
Identifies and Resolves Issues Before
Product Introduction***

Altera's Strategies for Delivering New Products

1. Precise investment in features and capabilities
2. Industry's most comprehensive test chip program
3. Rigorous device check-out procedures
 - Methodical and thorough check-out procedures help identify and resolve issues before products are released to customers

Altera's Rigorous 8-Step Product Checkout

1. IC design ensures design meets function, performance, and power specifications.
2. CAD and layout ensure that mask meets Altera's and TSMC's mask rules.
3. Cross-functional teams perform design-for-manufacturability (DFM) analysis to ensure robust manufacturing.
4. TSMC checks masks for high-volume, high-yield manufacturability.

Altera's Rigorous 8-Step Product Checkout

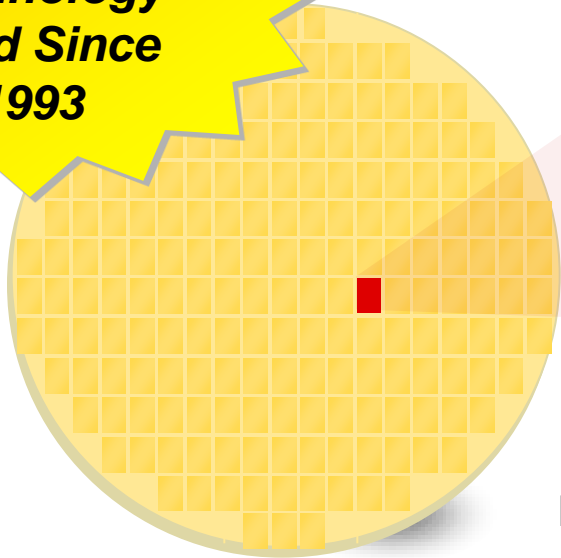
5. Altera and TSMC check transistor characteristics, layer thicknesses, line widths and resistances, etc.
6. Product engineering characterizes wafers and packaged units, gives feedback to improve yield.
7. Applications engineering exercises device from user perspective.
8. Reliability group ensures quality of final product before it is shipped to customers.

Altera's Strategies for Delivering New Products

1. Precise investment in features and capabilities
2. Industry's most comprehensive test chip program
3. Rigorous device check-out procedures
4. Unique patented redundancy technology
 - Unique Altera technology provides 7x to 8x yield improvement early in process life cycle
 - One of many DFM techniques Altera employs

Patented Redundancy Technology

**Patented
Redundancy
Technology
Used Since
1993**

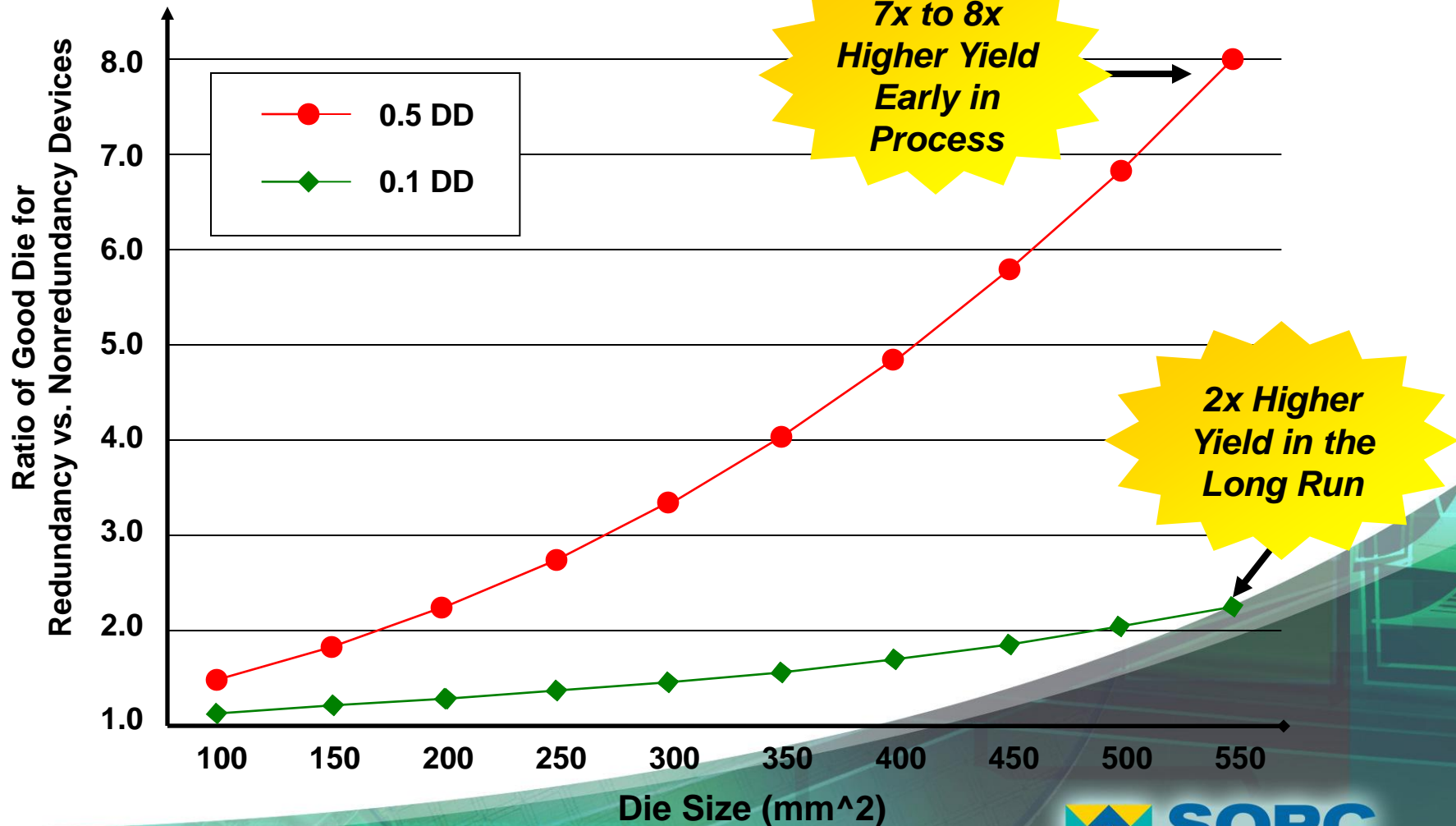


Column
With Defect
Deactivated

Redundant
Column
Activated

***Altera's 7th-Generation Patented
Redundancy Technology Improves
Yields***

Redundancy Enables Predictable Manufacturability



Altera's Strategies for Delivering New Products

1. Precise investment in features and capabilities
2. Industry's most comprehensive test chip program
3. Rigorous device check-out procedures
4. Patented redundancy technology
5. Focused foundry partnership
 - Industry's longest and stronger foundry partnership
 - Accelerates improvement in yield, improves supply

Altera's Foundry Partner: TSMC

- TSMC leads the foundry industry
 - Over 50% market share
 - Annual R&D investment 55% greater than nearest competitor
 - Leader in DFM and lithography
 - Longest-running mask making facility
- Semiconductor industry leaders are driving TSMC's 65-nm process to success



The Industry's Strongest Foundry Partnership



What Altera Gets:

Access to most advanced process without huge R&D investments

Pure play foundry—no capacity conflict

Mutual benefit of an exclusive relationship

Ability to get process tuned to its needs

Benefit to



FPGA Structure

Memory structure
Large dies
Dense interconnect
High performance

What TSMC Gets:

Defect identification
Defect density reduction
Back-end improvements
Front-end improvements

Focused Partnership of Industry Leaders Drives Both to Success

Benefits of Focused Foundry Partnership

■ Better product availability

- Total wafer volume through single foundry maximizes yield enhancement
- Eliminates inefficiency of multiple foundries, simplifies supply chain

■ Streamlined inventory management

- Multiple foundries may require managing multiple codes for “same” device

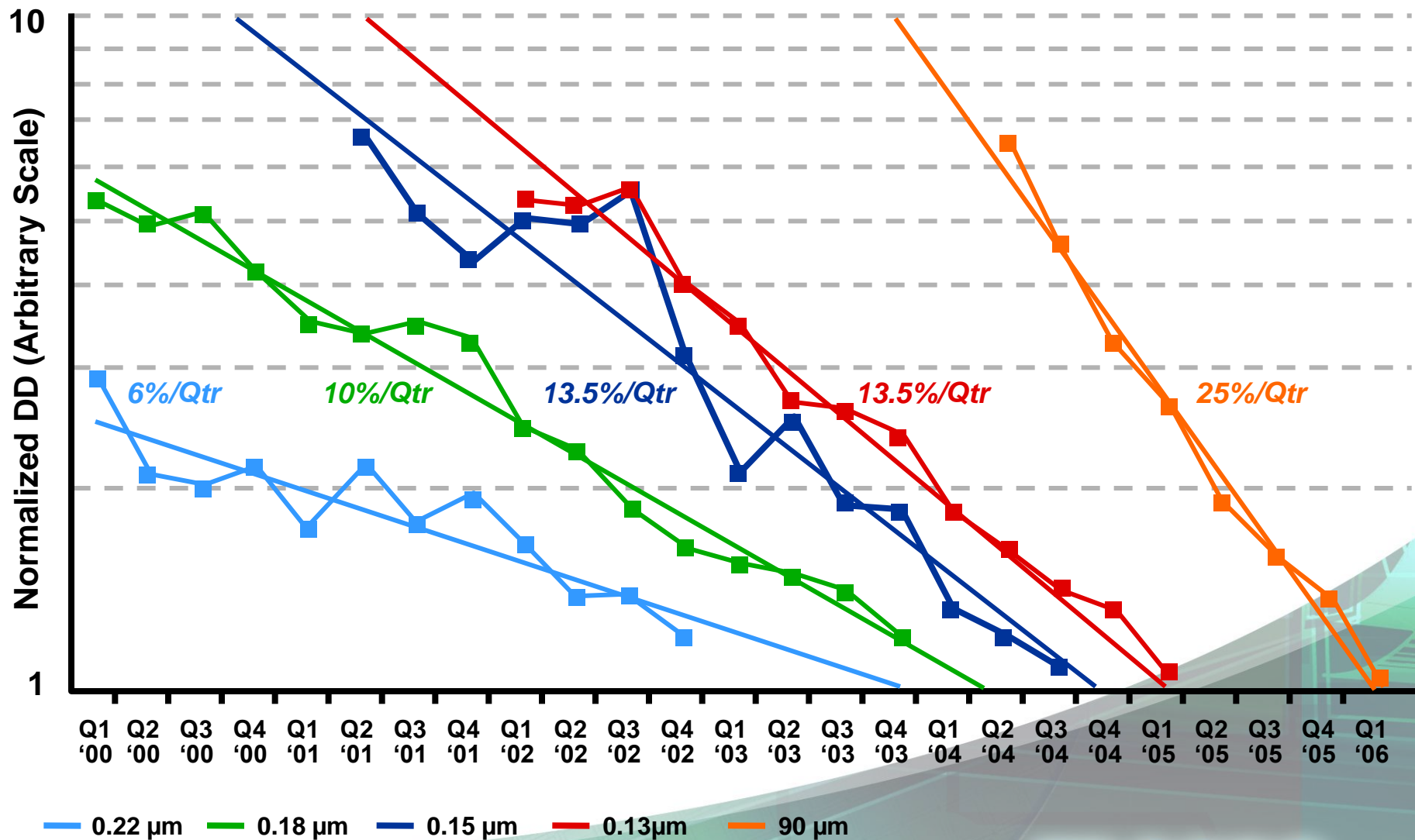
■ Fewer device qualifications

- Single characterization effort
- Eliminates need to do qualifications for more than one foundry

■ Consistent product performance characteristics

- One manufacturing process produces the most uniform results
- Avoids inconsistencies arising from multiple mask sets among multiple foundries

Altera-TSMC Record of Defect Density Reduction



0.22 μm 0.18 μm 0.15 μm 0.13 μm 90 μm

Conclusion

- Altera makes technology choices aimed at successfully delivering products to customers
- Altera has the best industry record of reliably delivering the benefits of new semiconductor process technology
- Metrics for our mutual success:
 - Meeting commitments to deliver new products on schedule
 - Achieving smooth ramps to volume production
 - Resolving product issues *before* product introduction

***Altera Products Fulfill the
Promise of Increased
Productivity and Minimized Risk***


```
nbit_adder: adderx
    GENERIC MAP (x => n)
    PORT MAP (AddSubR_n, G, H, M, carry_in);
multiplexer: mux2to1
    GENERIC MAP (x => n)
    PORT MAP (A, B, Z, S, carry_in);
AddSubR_n <= (OTHERS => AddSubR_1)
M <= Z XOR AddSubR_n
carry_out XOR G(n-1) XOR H(n-1) XOR M(n-1);
```

Thank You Q & A