Implementing Video and Image Processing Designs Using FPGAs

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Agenda

- Key trends in video and image processing
- Video and Image Processing Suite
- Model-based design for video processing
- Tutorial

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Video and Imaging With FPGAs

Broadcast Infrastructure

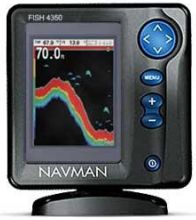
HDTV Videoconferencing

HDTV Display

Security DVR

Medical Imaging

HD Security Camera



Consumer/Auto Display

Document Imaging

Military Imaging

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Key Trends in Video and Imaging

- Higher resolutions
  - 3,000 x 3,000 (and higher): medical imaging, military, machine vision
  - 4,096 x 1,714: digital cinema
  - 1,920 x 1,080: HDTV, broadcast
  - 1,280 x 720: video surveillance, videoconferencing
- Advanced video compression
  - H.264, JPEG2000, VC1

Current Solutions Do Not Deliver

Video/ Imaging ASSPs	*Not optimized for target applications* *Risk of obsolescence*
DSP	*Cannot achieve high definition in single device*
ASIC	*High development cost* *Cannot keep up with fast-evolving applications*

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Altera's FPGA Solution

- High performance in a single device
- Fast time-to-market
- Easy to upgrade
- Low development cost
- Obsolescence proof
- Lower unit costs at high volumes

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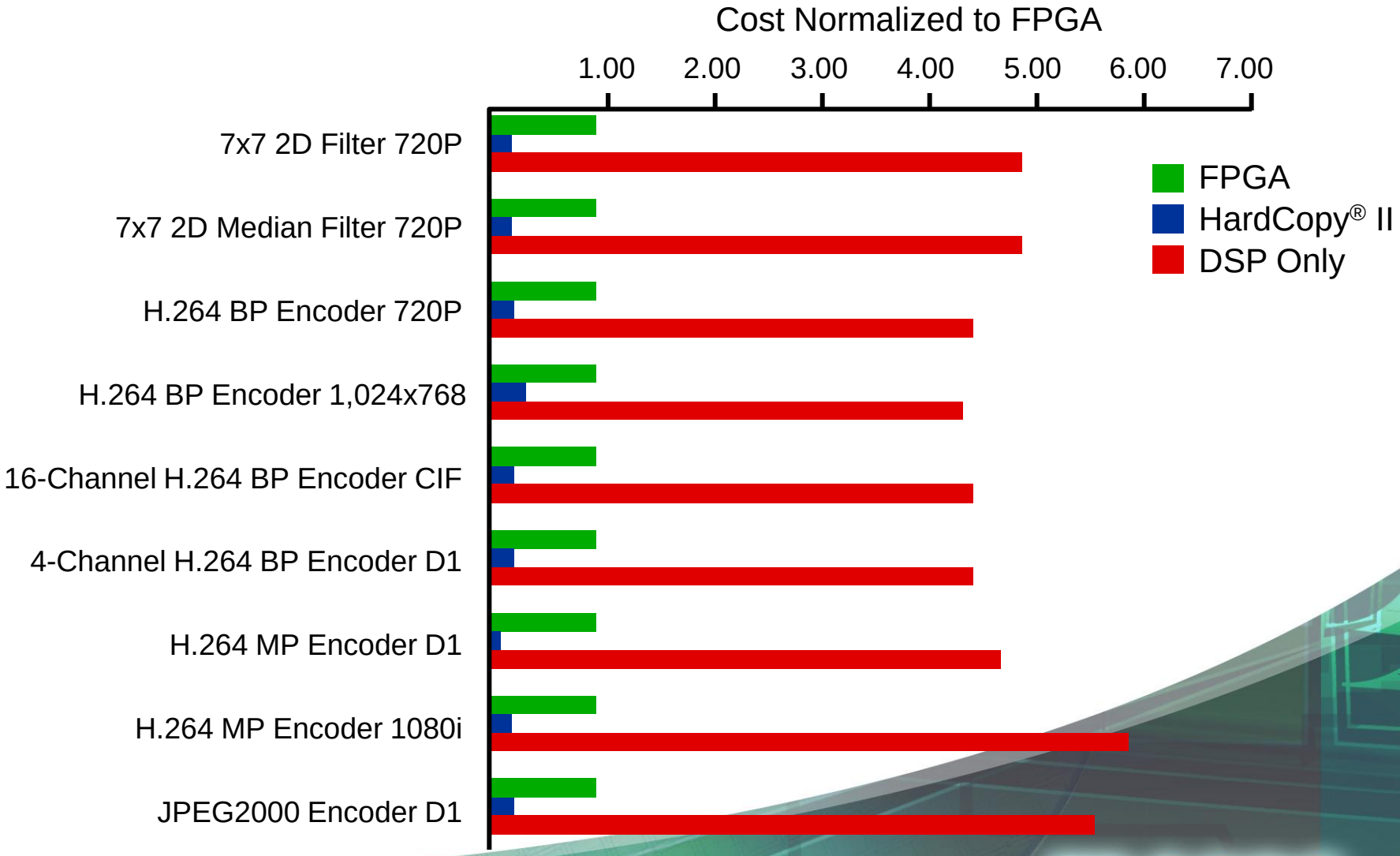
Video Benchmarks



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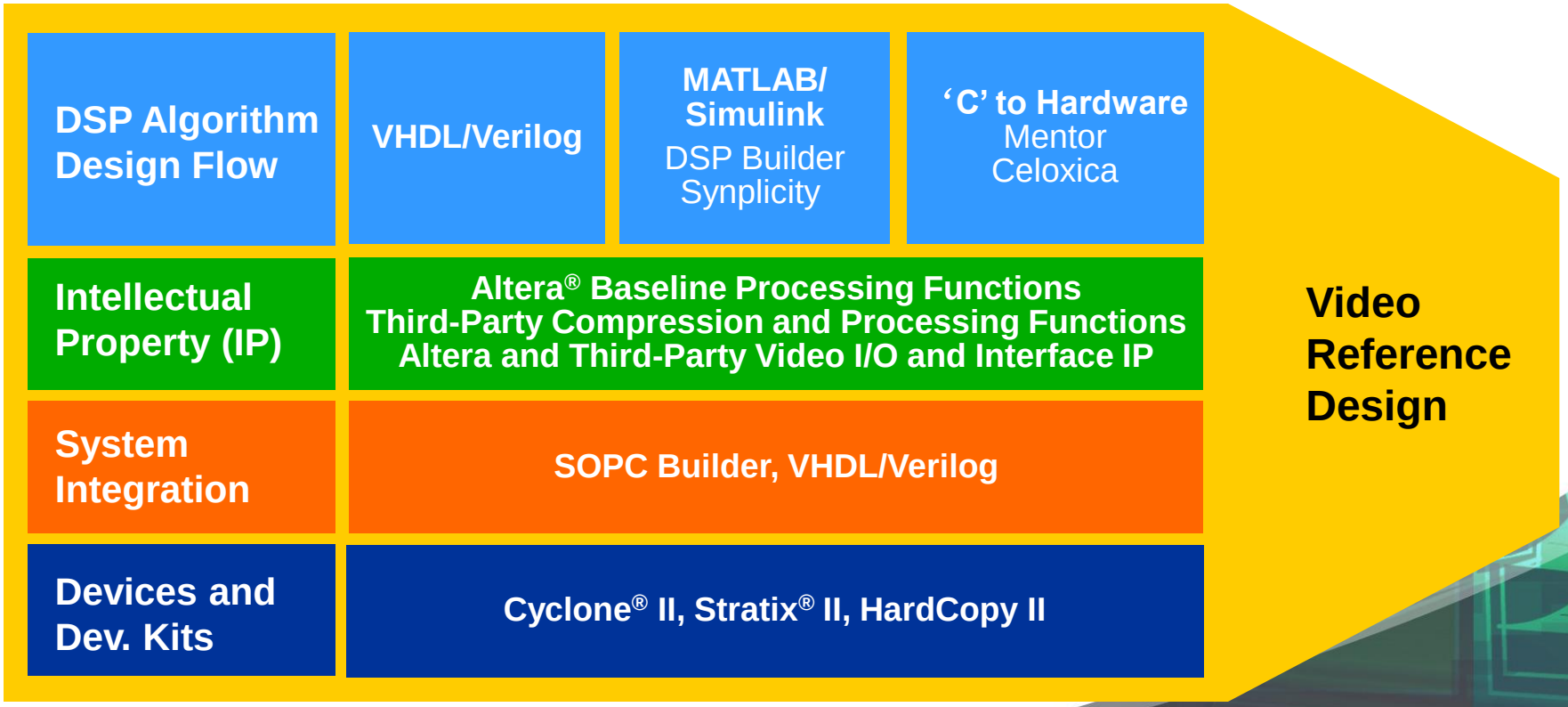
Altera Video and Image Processing Solutions Overview



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IP Examples – Video

I/O and System

- PCI Express
- Serial Rapid I/O
- EMIF Interface
- ASI
- SDI
- ATA HDD (Nuvation)
- MPEG2 Transport
- 10/100/1000 Ethernet
- DDR/DDR2 Controller

Pre-/Post-Processing

- Scaler
- Deinterlacer
- 2D FIR Filter
- 2D Median Filter
- Color Space Converter
- Chroma Resampler
- Gamma Corrector
- Alpha Blender
- Highest Quality HDTV Upconversion (Let It Wave)
- AES/DES/Sha-1 Encryption (CAST)

Video and Image Processing Suite

Compression

- H.264 MP, HP (ATEME)
- H.264 BP (4i2i, CAST, W&W)
- H.264 CABAC/CAVLC (ATEME)
- H.264 Loop Filter (ATEME)
- MPEG4 SP/ASP (CAST, Barco)
- JPEG (CAST, Barco)
- JPEG2000 (CAST, Barco, Broadmotion)

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HDTV Upconversion – Let It Wave

- Breakthrough super-resolution Bandlet technology for HDTV upconversion
- Broadcasting equipment
  - Upconverter implemented on cost-effective Altera FPGA
    - Main features
      - Standard definition (SD) to high definition (HD) up to 1080P
      - 2-frame delay
      - Color conversion
      - Per pixel automatic film mode and cadence detection
      - Aspect ratio conversion
    - Additional features
      - Cross conversion 720P to 1080I
      - HD to SD down conversion
      - Video enhancement
    - Board reference design available

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Video and Image Processing Suite

Altera Video and Image Processing Suite

- Baseline set of IP with standard interfaces and protocols that allow users to easily add their own proprietary algorithms
- Optimized for Altera FPGAs
- Works with any design flow
  - RTL, model-based design, C-based design

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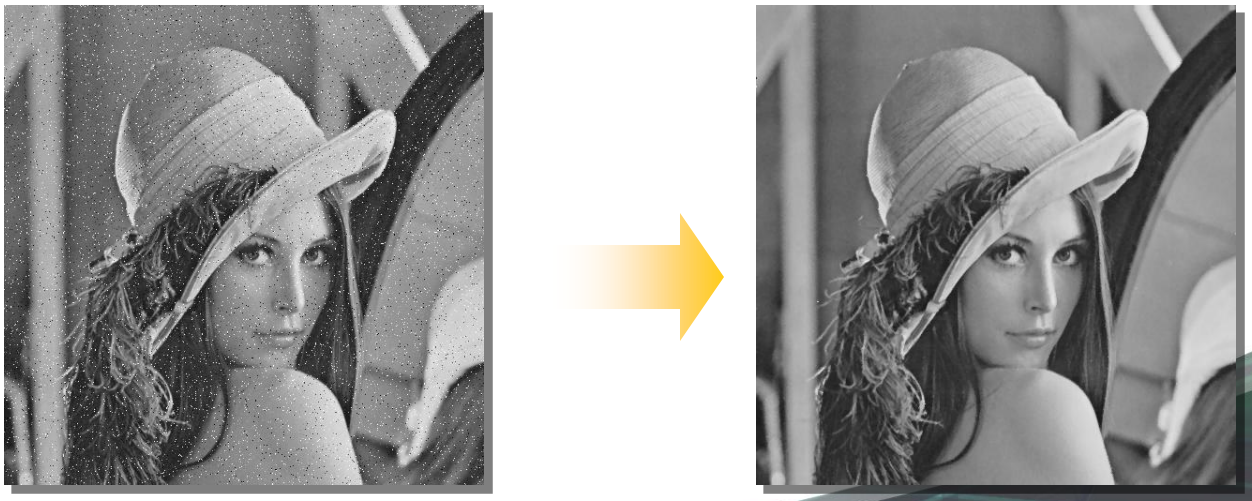
Video and Image Processing Suite

Core	Function
Deinterlacer	Converts interlaced video formats to progressive video format
Color space converter	Converts image data between a variety of different color spaces
Scaler	Resizes and clips image frames
Gamma corrector	Performs gamma correction on a color space
Alpha blending mixer	Mixes and blends multiple image streams, including picture-in-picture (PIP)
Chroma resampler	Changes the sampling rate of the chroma data for image frames
2D filter	Implements a 3x3, 5x5, or 7x7 finite impulse response (FIR) filter on an image data stream to smooth or sharpen images
2D median filter	Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Line buffer compiler	Efficiently maps image line buffers to Altera on-chip memory

2D Filtering

- 2D FIR filter and 2D median filter
  - 3x3, 5x5 or 7x7 filter sizes
- Useful for noise reduction and smoothing filters
- Supports symmetric optimization

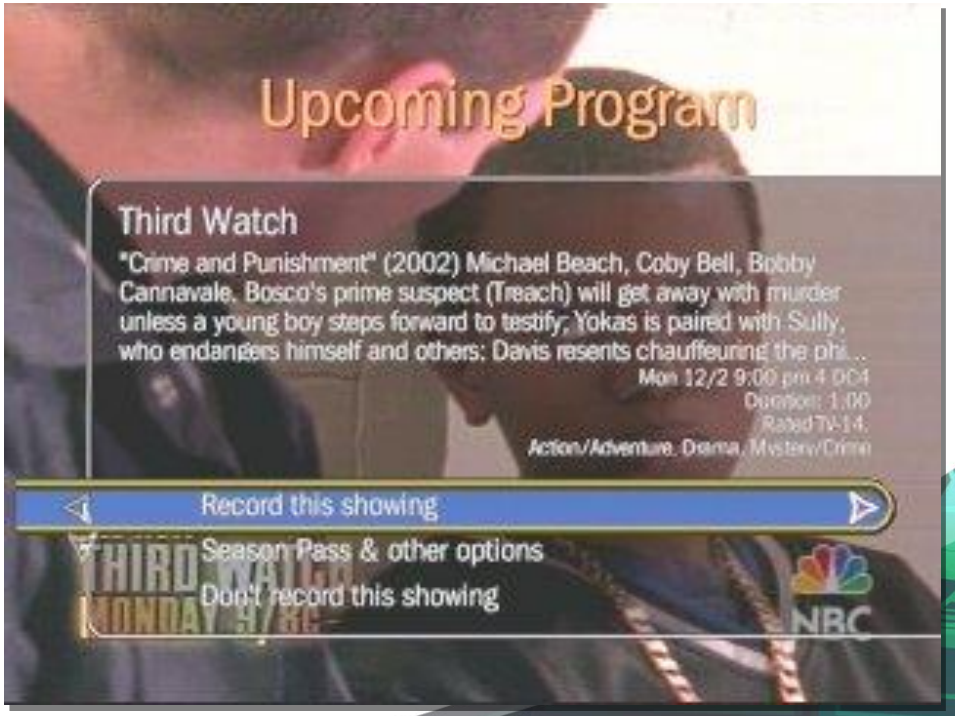


Color Format Conversion

- Supplied as three separate cores
  - Color space converter
  - Chroma resampler
  - Gamma corrector
- Supports
  - RGB (computer and studio formats)
  - YIQ/YUV (NTSC, PAL, SECAM)
  - YCbCr (4:4:4, 4:2:2, 4:2:0)

Image Blending and Picture-in-Picture Mixing

- Multi-layer mixing (2 to 8 layers)
- Per-pixel alpha blending
- Run-time control of picture-in-picture location



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Scaling

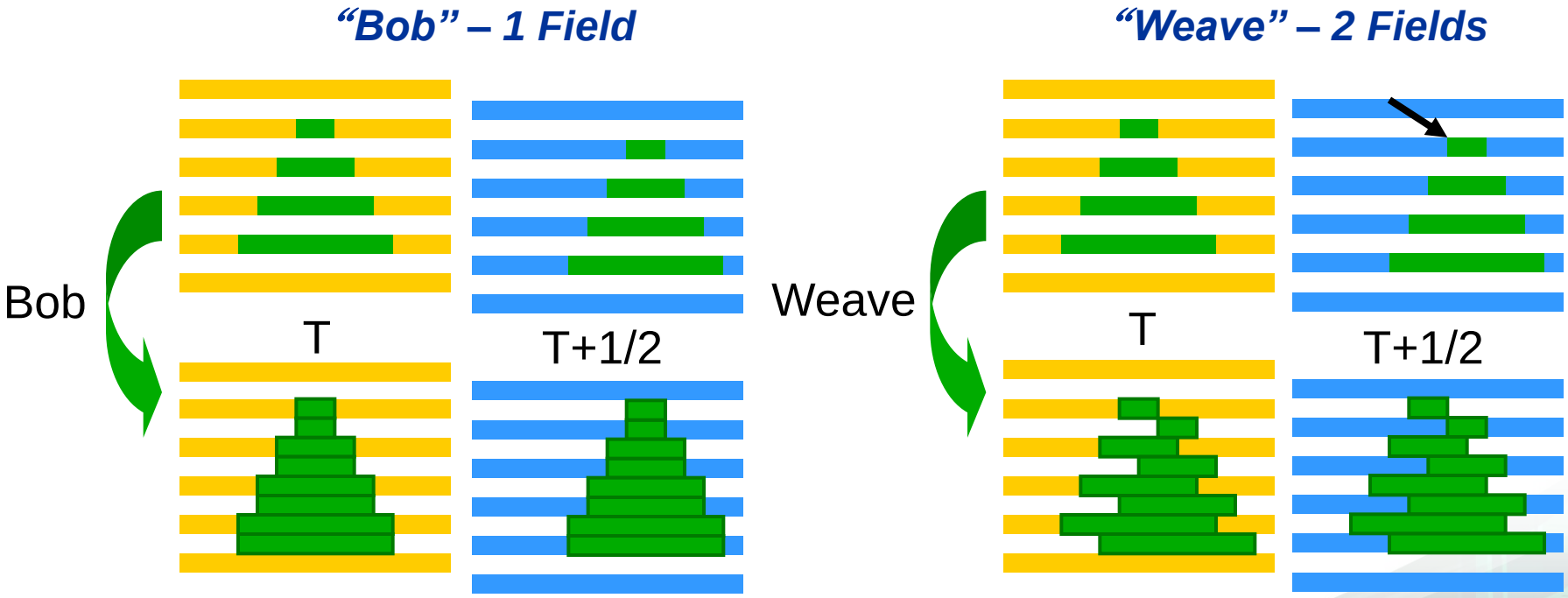
D1/SDTV: 720 x 480

HDTV 1080p: 1920 x 1080

- Supports standard-resolution conversions
- Nearest neighbor or bilinear filtering
- Clipping

Deinterlacing

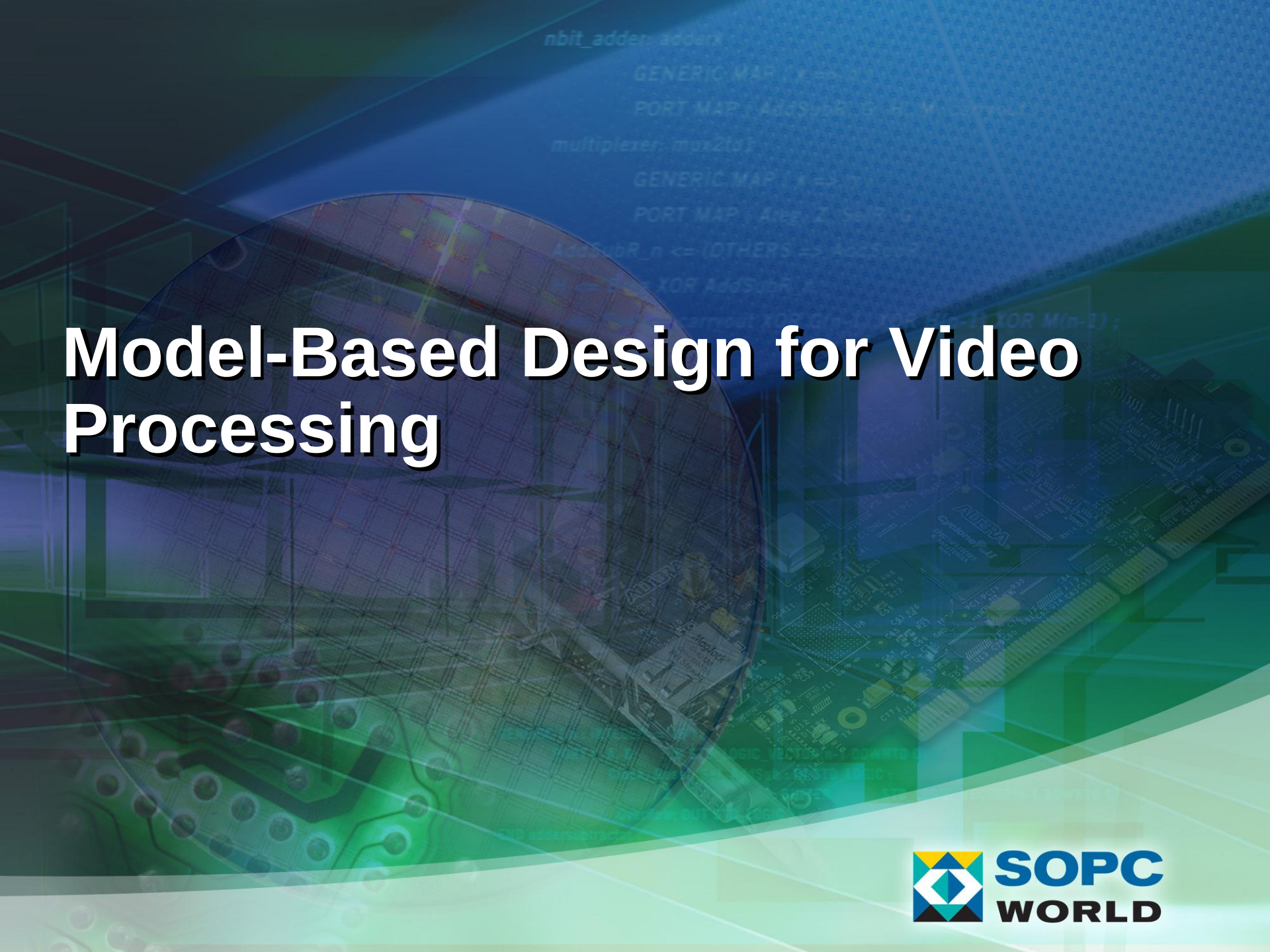
- "Bob" and "Weave" supported



Line Buffer Compiler

- Provides line buffers, making efficient use of FPGA internal memories
- Optimized for typical SD and HD resolutions
- Any number of bits per color plane
  - Choose line length, width, number of lines

Model-Based Design for Video Processing



Design Flow Starting with Model-Based Design

- DSP Builder for data path
  - Design
  - Simulation
  - Creation of an SOPC Builder component
- SOPC Builder for system integration
  - External RAM controllers
  - Sources and sinks
  - Processor integration
    - Nios® II or external processor
- Compile in Quartus® II software

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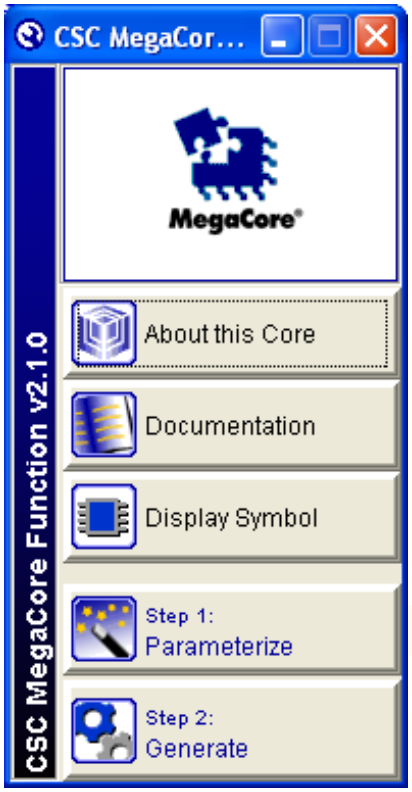
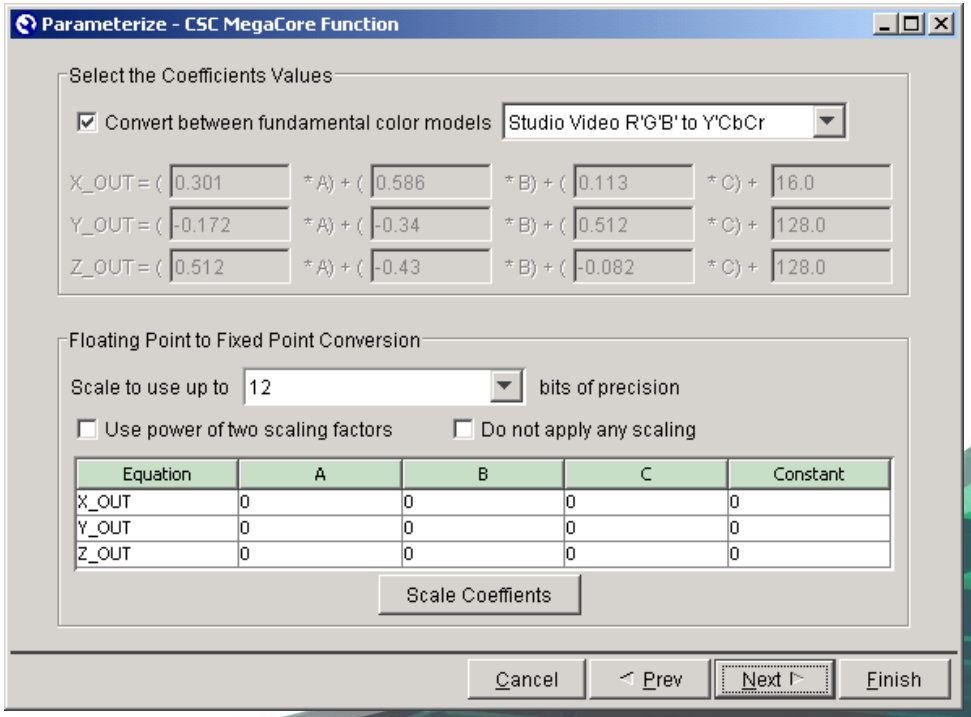
Configure Blocks with GUI

- IP Toolbench
  - Launched from Quartus II software or directly in DSP Builder





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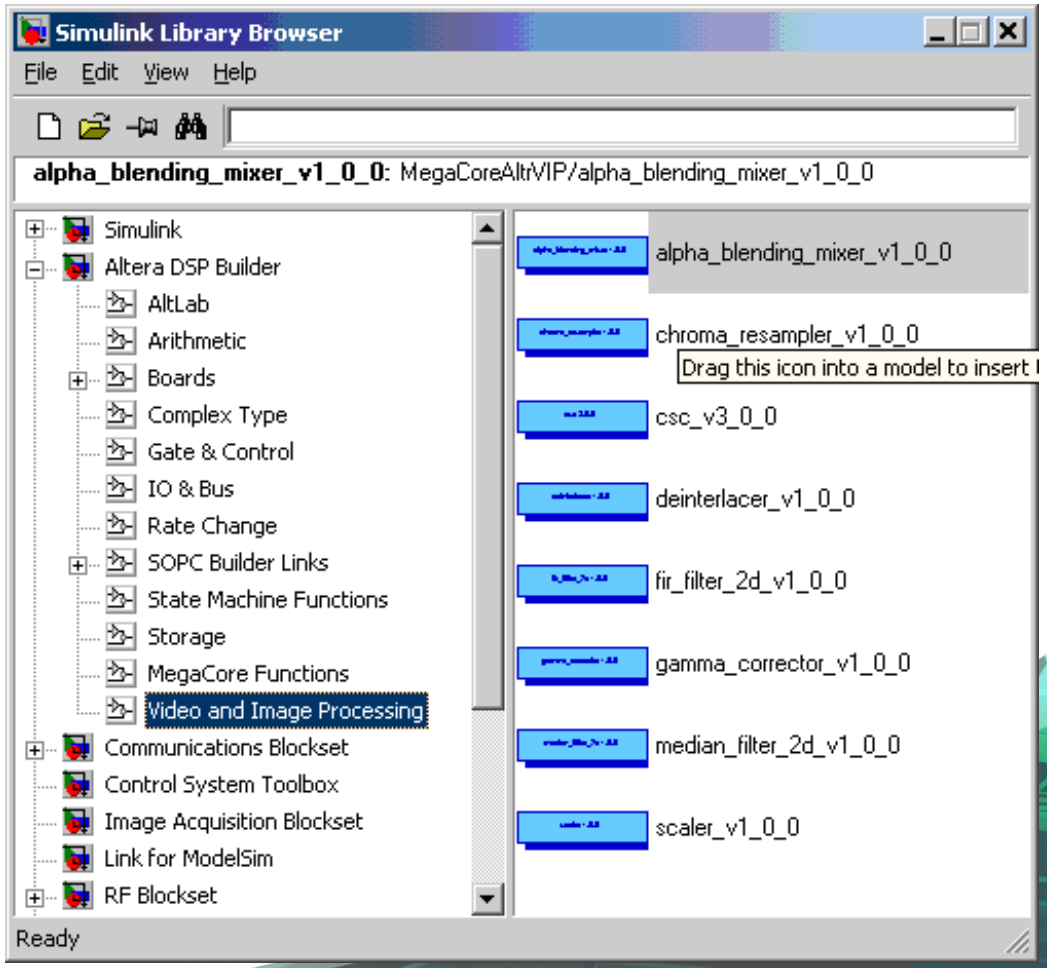
DSP Builder Video Library

- Alpha blending mixer
- Chroma resampler
- Color space converter
- Gamma corrector
- Deinterlacer
- 2D FIR filter
- 2D median filter
- Scaler



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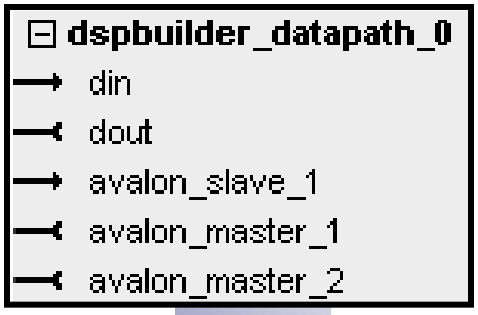
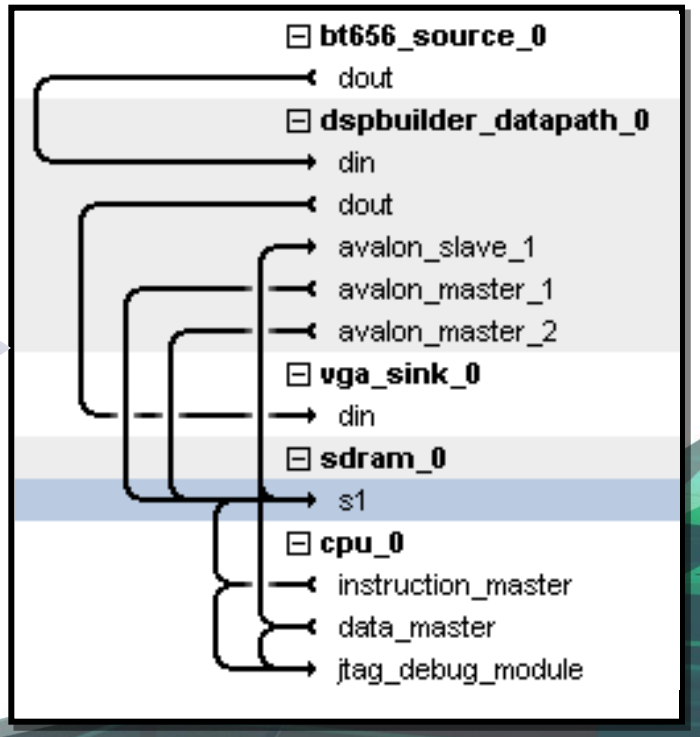
SOPC Builder System Integration

DSP Builder Data Path



SOPC Builder System



- Add
  - Sources
  - Sinks
  - Arbitrated DDR, SDR
  - Control

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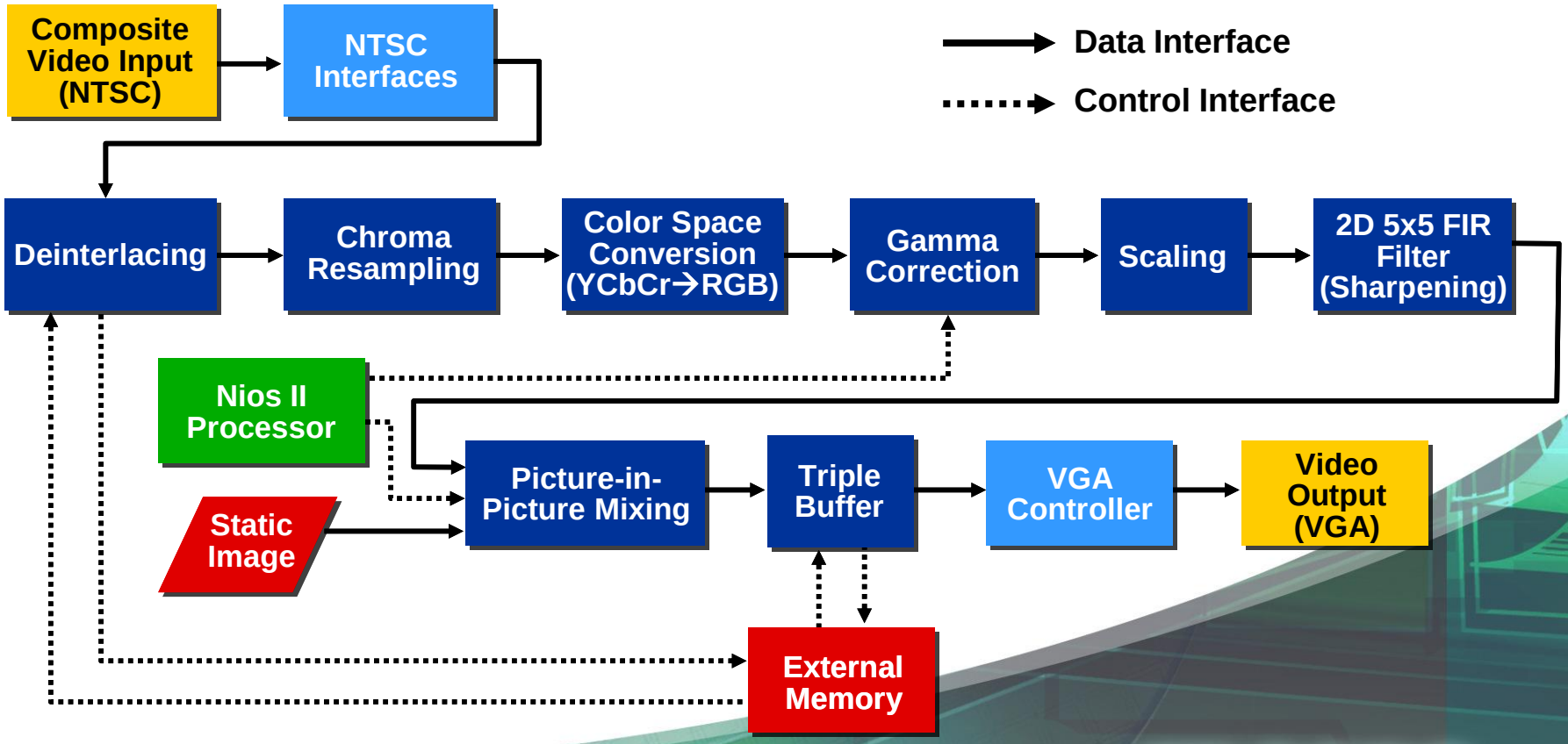
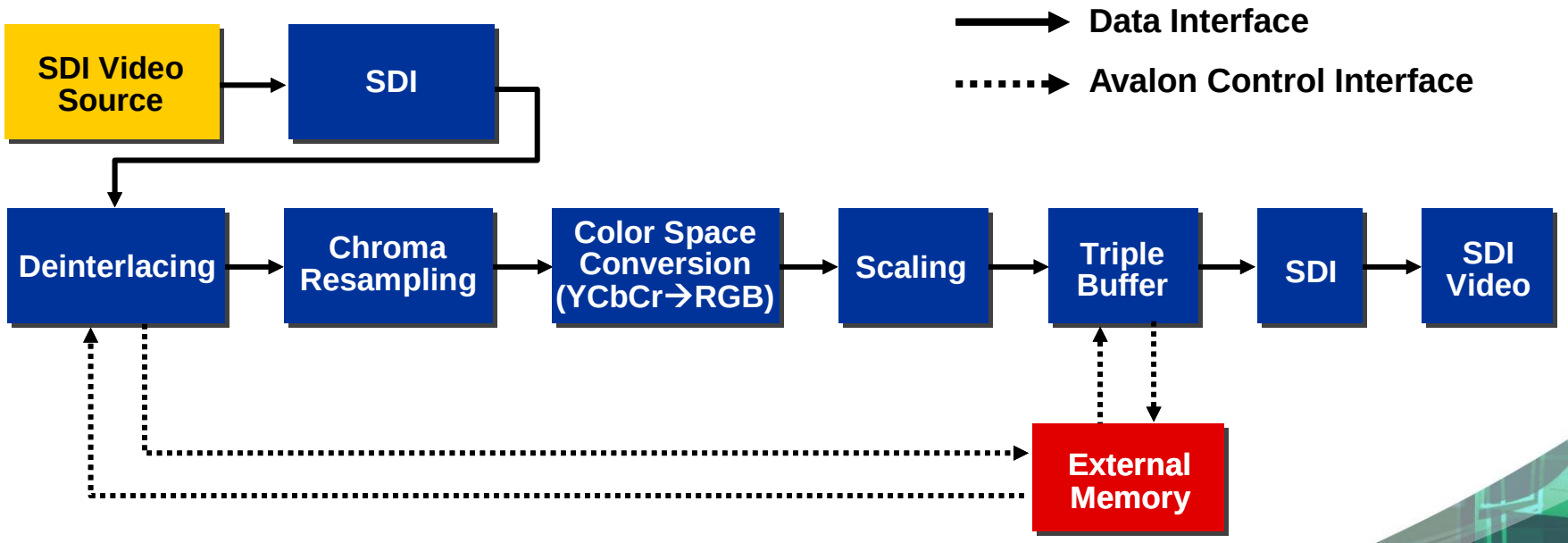
Example 1: Single Input Video Channel

- Composite video input
- VGA output



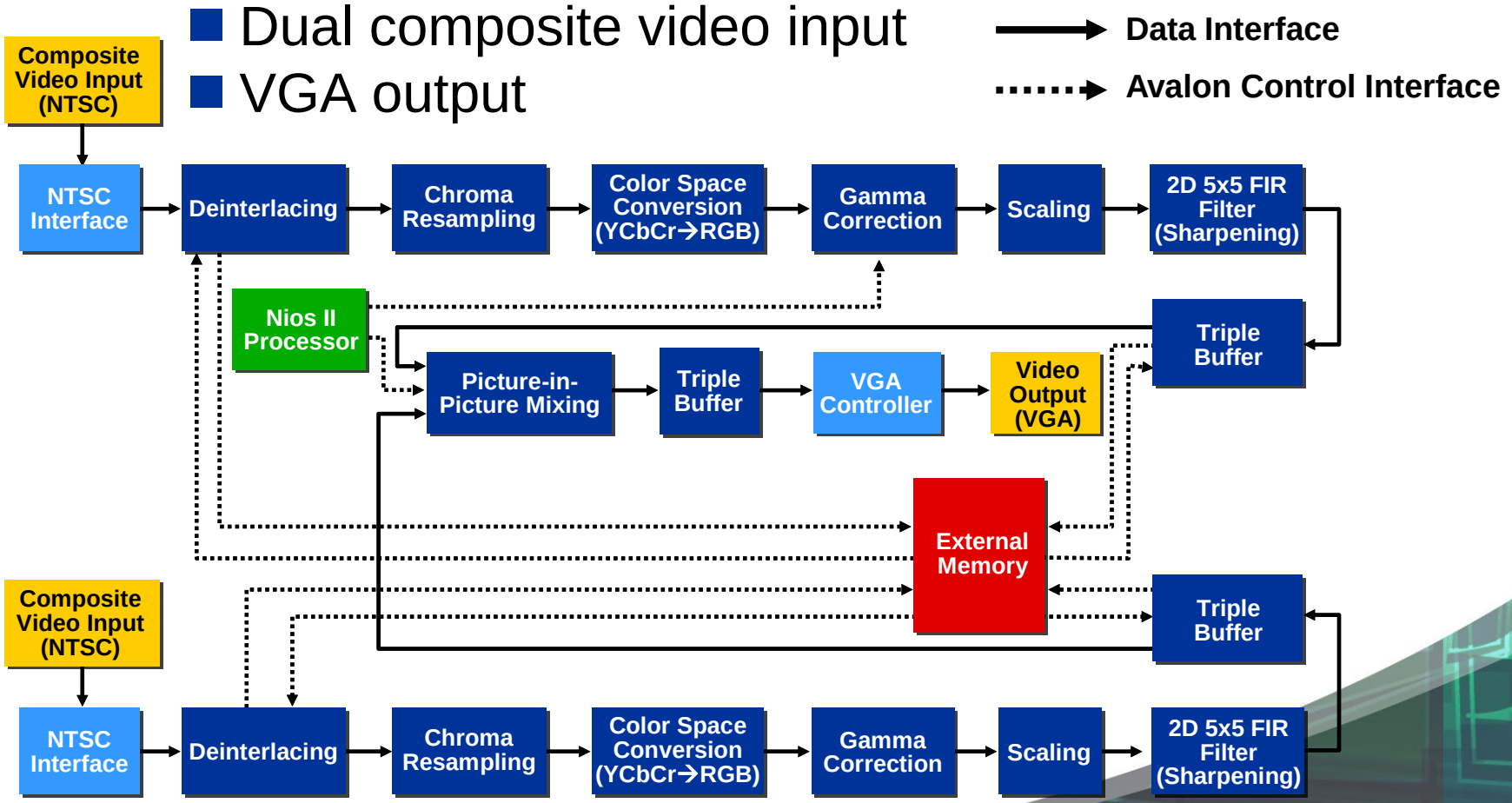
Example 2: Single Input Video Channel

- SDI video input/output

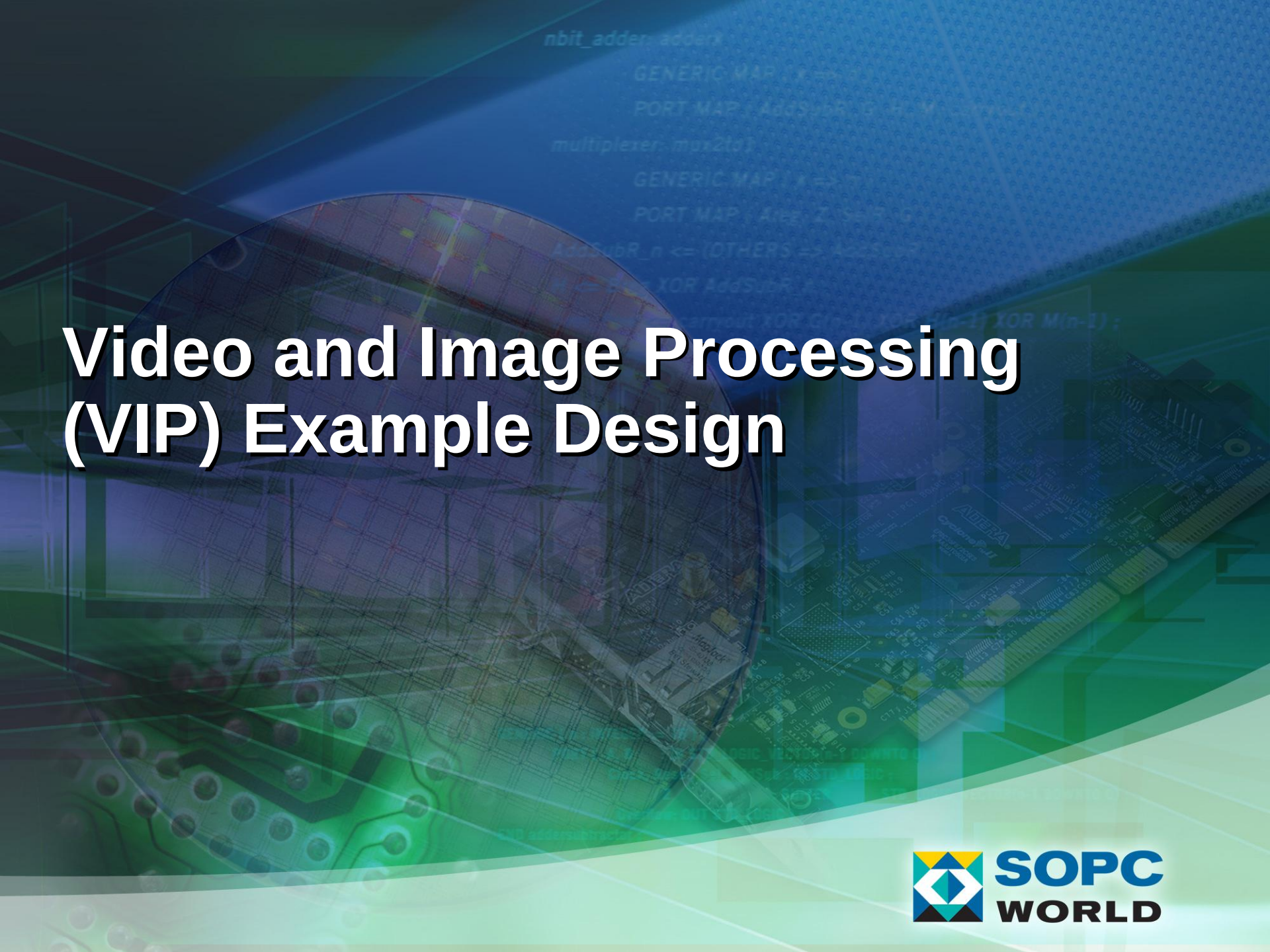


Example 3: Multiple Video Channel Input

- Dual composite video input
- VGA output



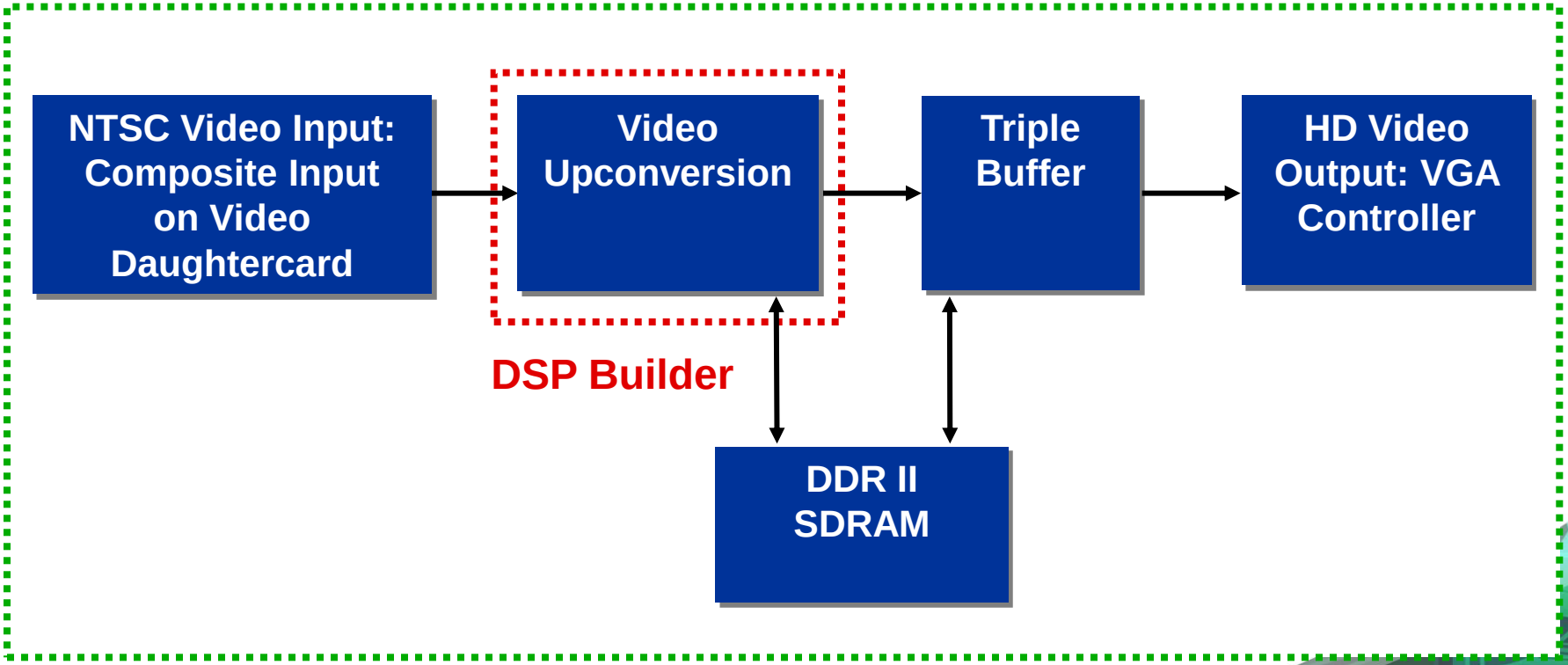
Video and Image Processing (VIP) Example Design



Example of a Video System

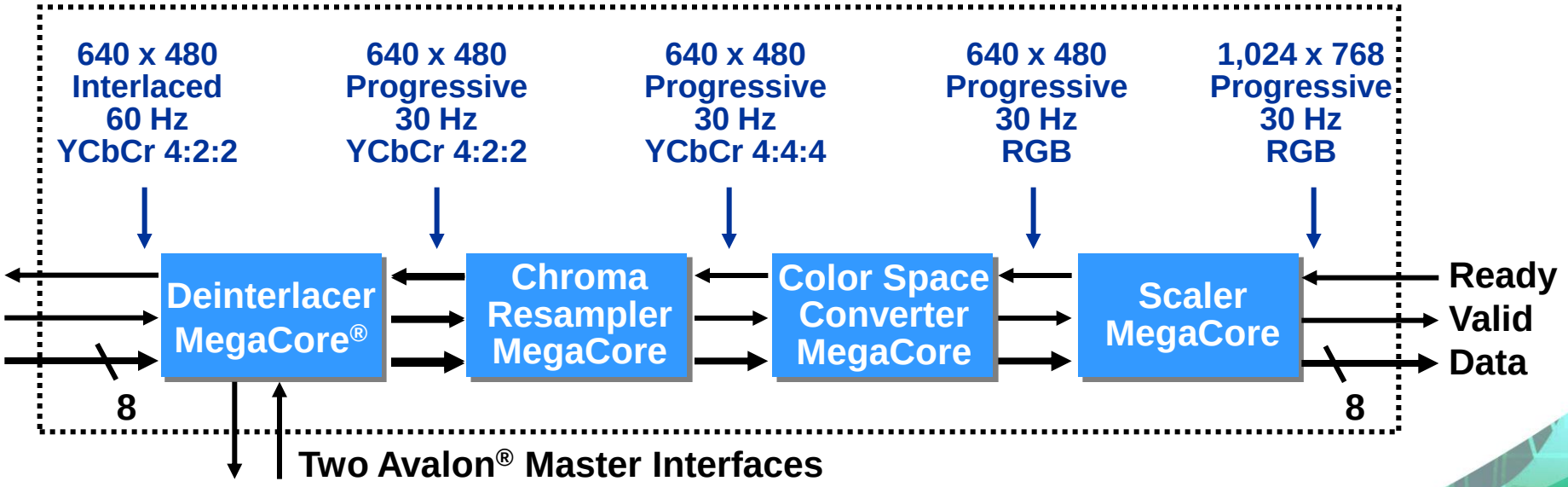
- System block diagram
- DSP Builder
  - Implementation
  - Simulation
  - Conversion to HDL
- SOPC Builder integration
- Program hardware platform

VIP Upconversion System



Video Upconversion Data Path

- Entire data path is assembled in DSP Builder



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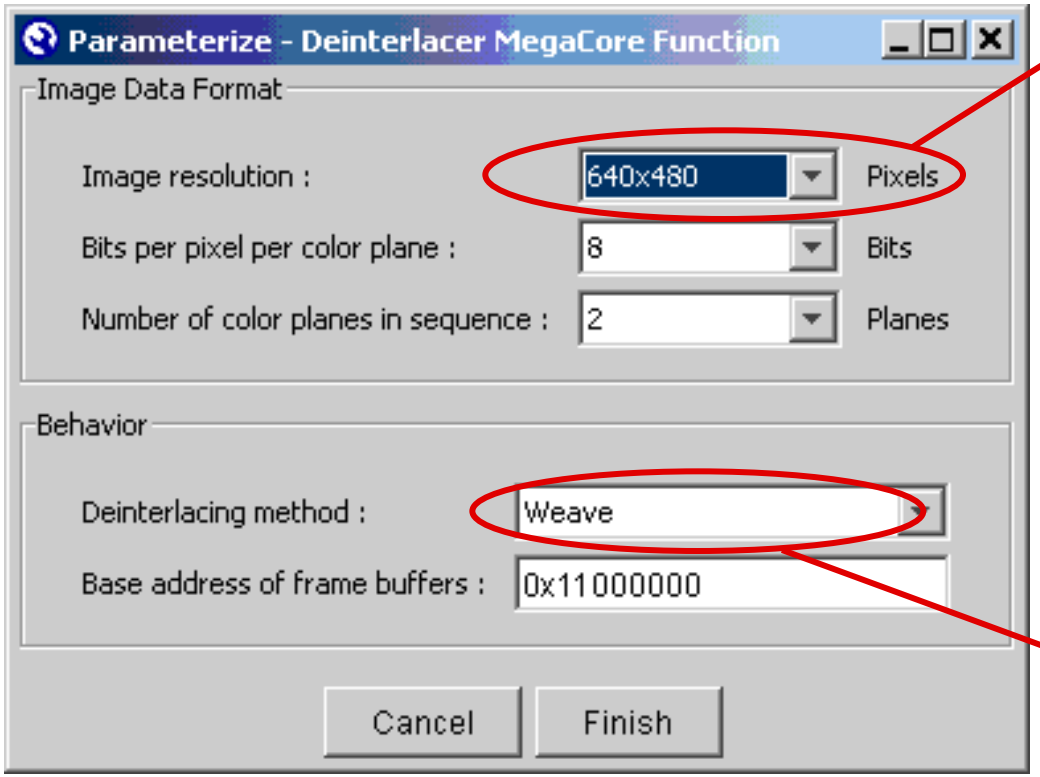
DSP Builder Implementation - Deinterlacer

Parameterize Deinterlacer



Up to 1920 x 1080 Supported

Bob and Weave Supported

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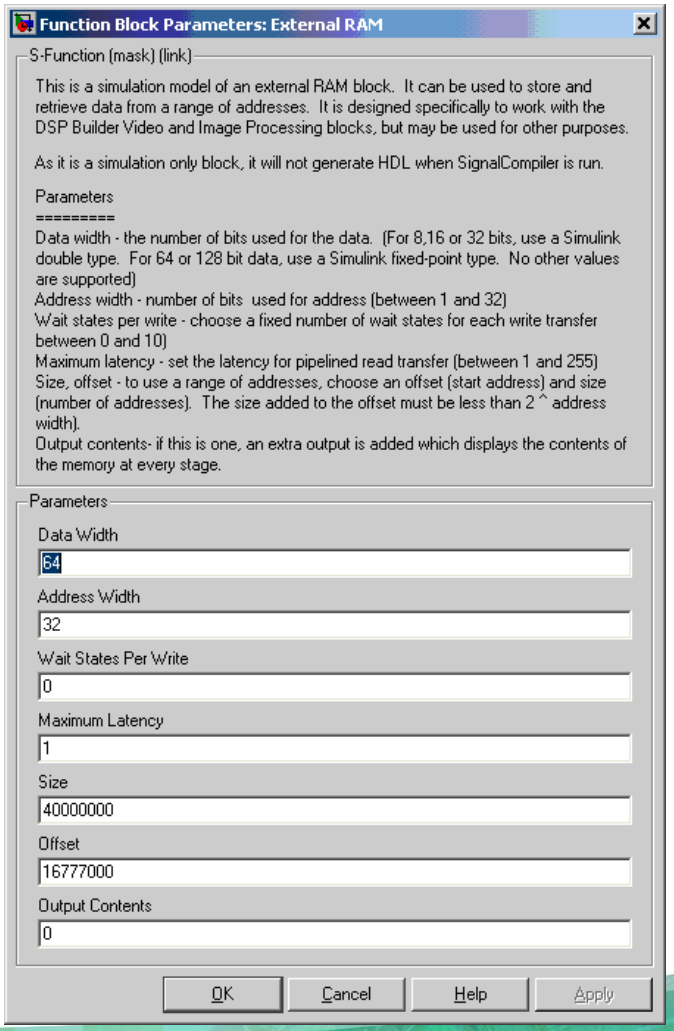
DSP Builder Implementation: External Memory for Deinterlacer



Parameterize External Memory (Simulation-Only Model)

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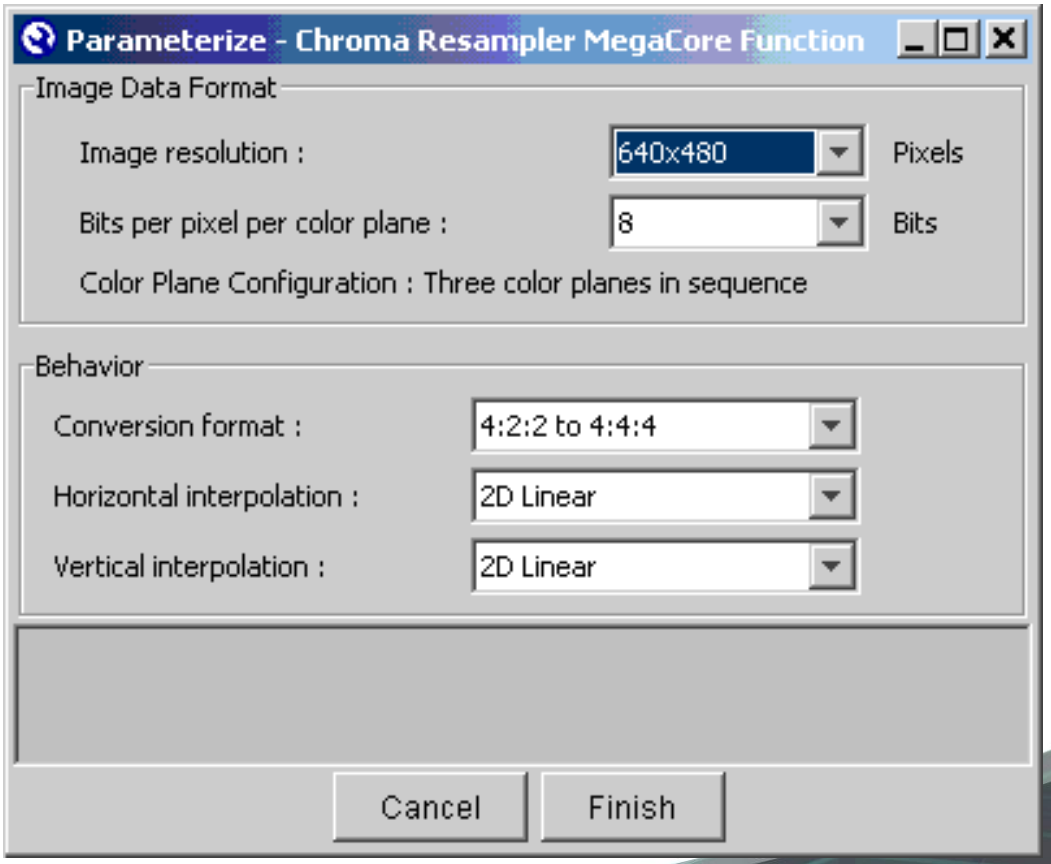
DSP Builder Implementation: Chroma Resampler



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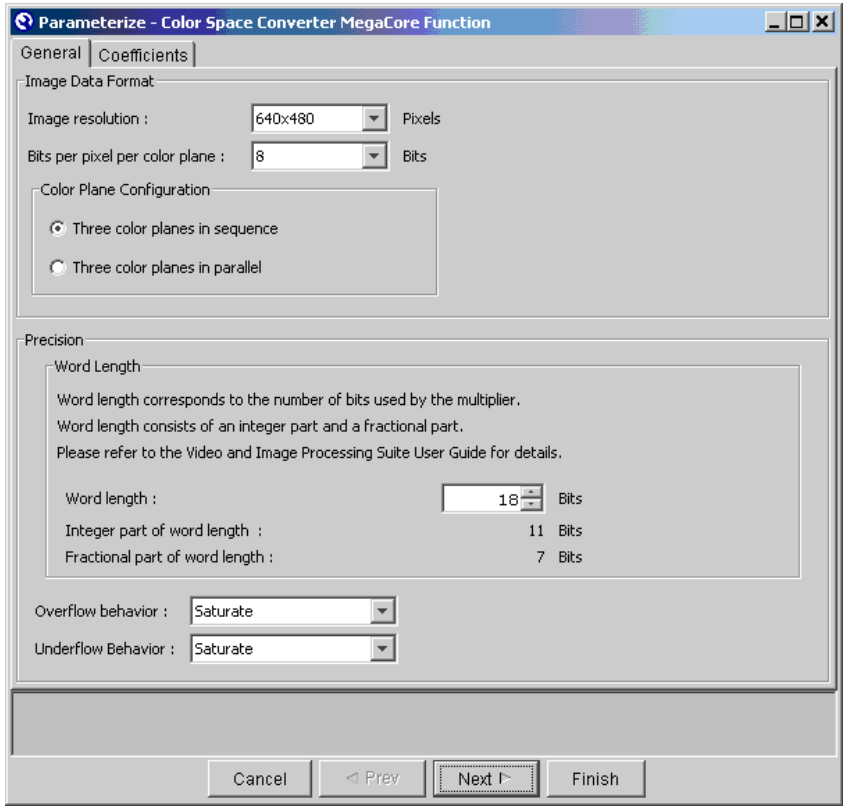
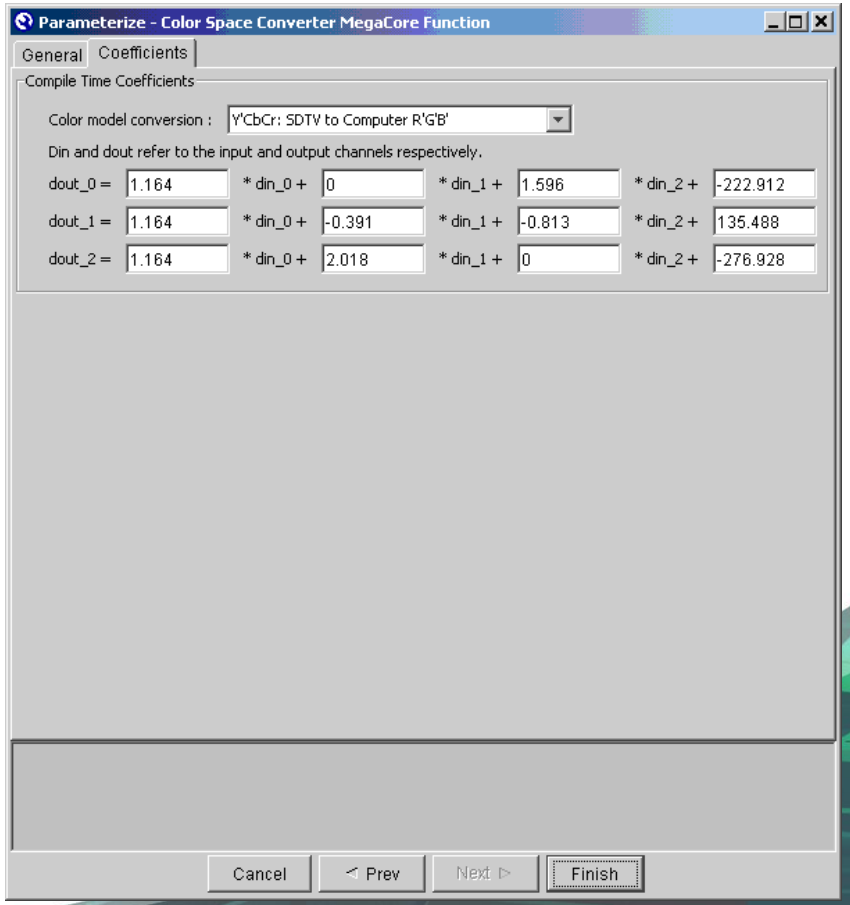
DSP Builder Implementation: Color Space Converter





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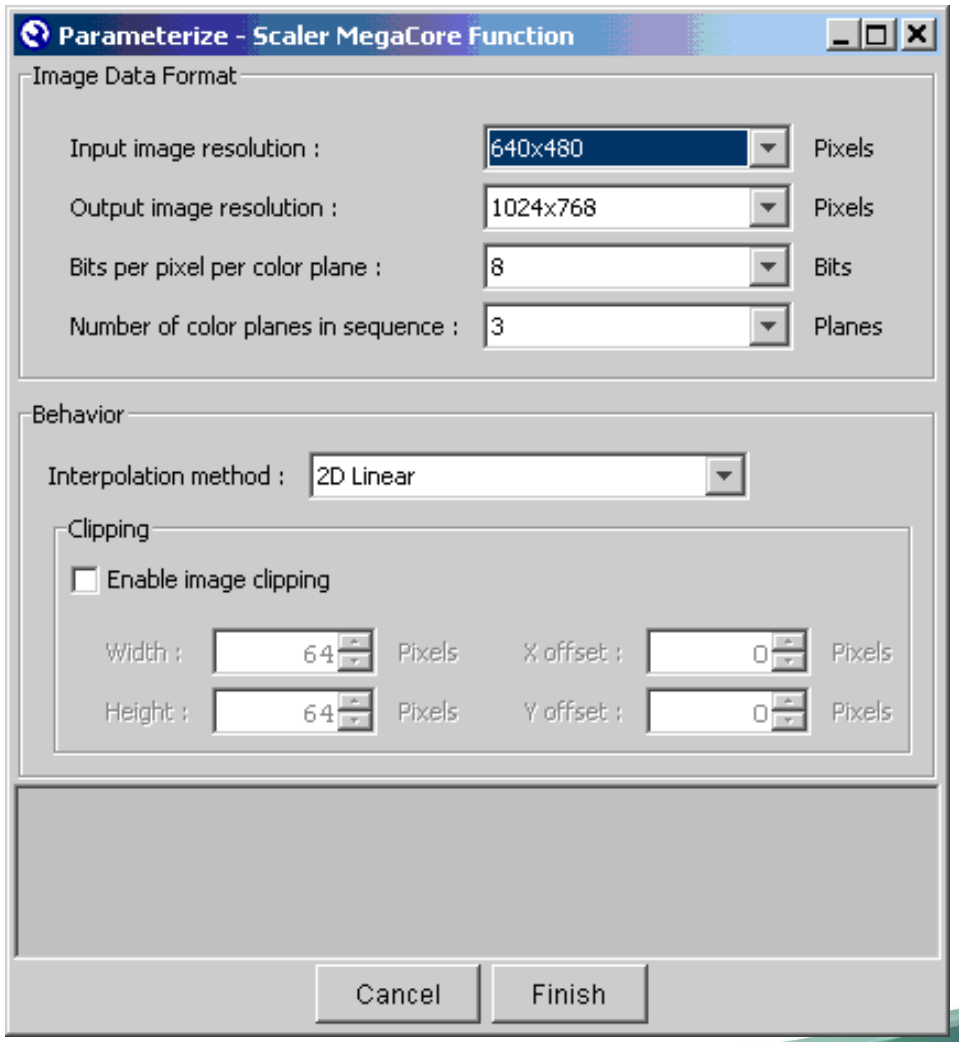
DSP Builder Implementation: Scaler



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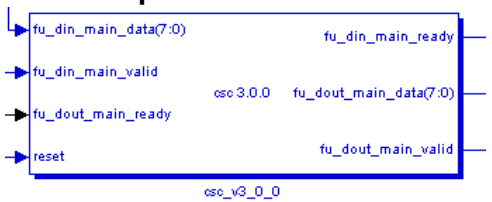
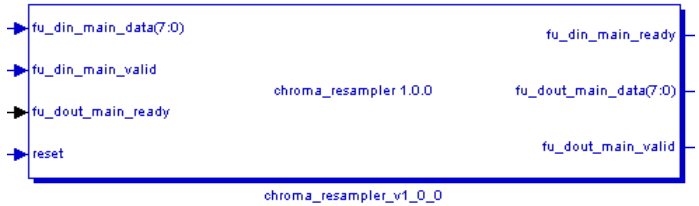
DSP Builder Implementation: Libraries Generated

Deinterlacer

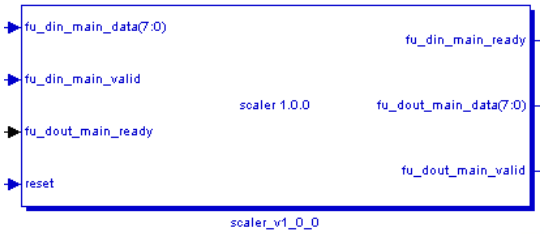
Color Space Converter



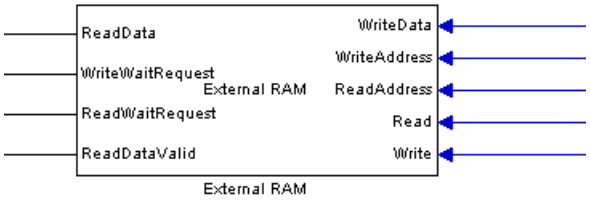
Chroma Resampler



Scaler



External Memory (Simulation)



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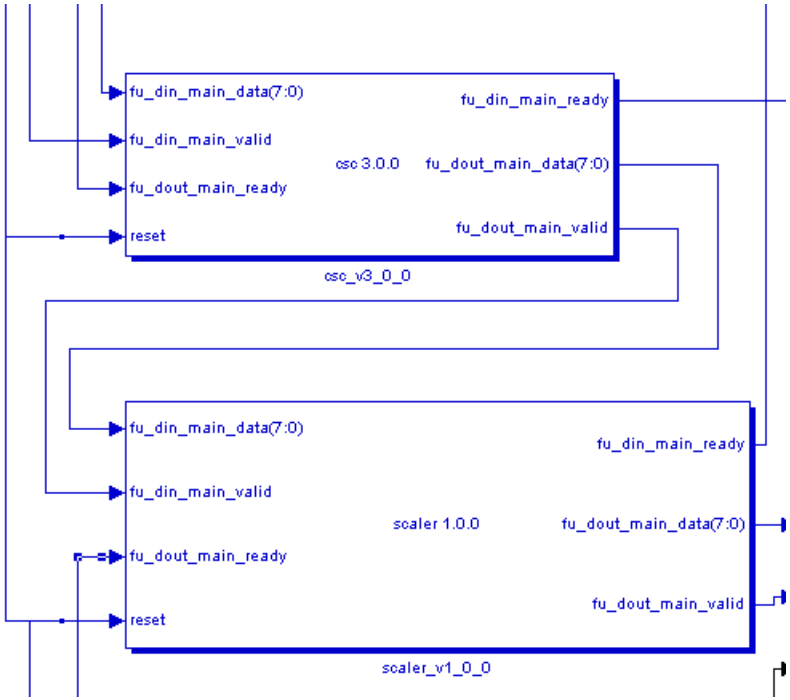
DSP Builder Implementation: Connecting Functions

- Connecting library functions is simple due to standard interface and protocol



Connections Between the Color Space Converter and Scaler

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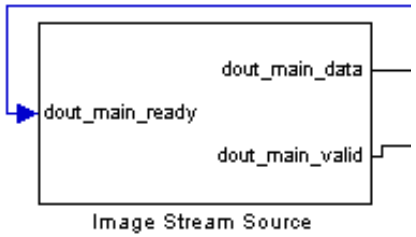
Simulation: Video Input

1



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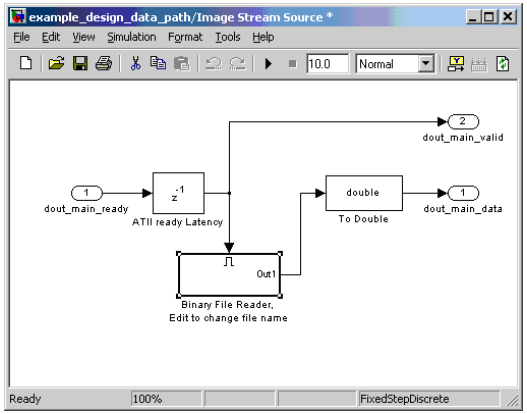

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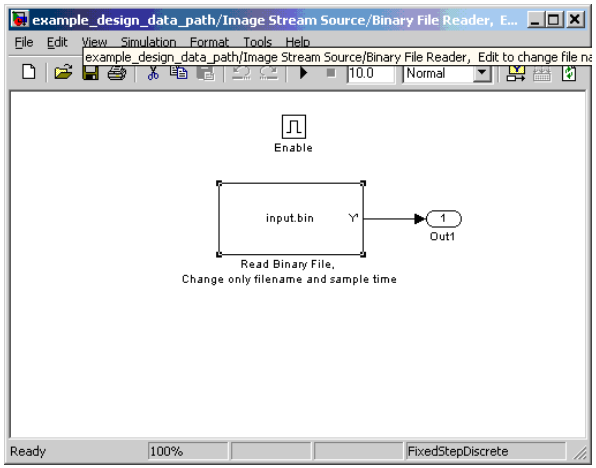

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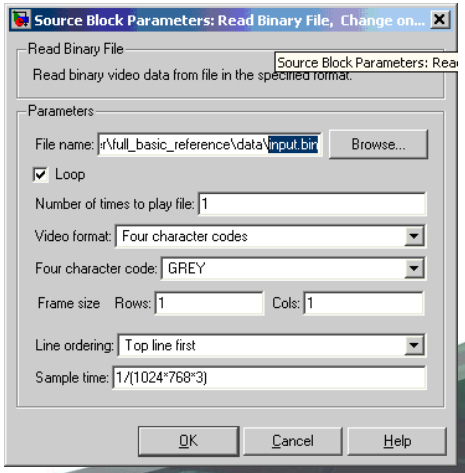

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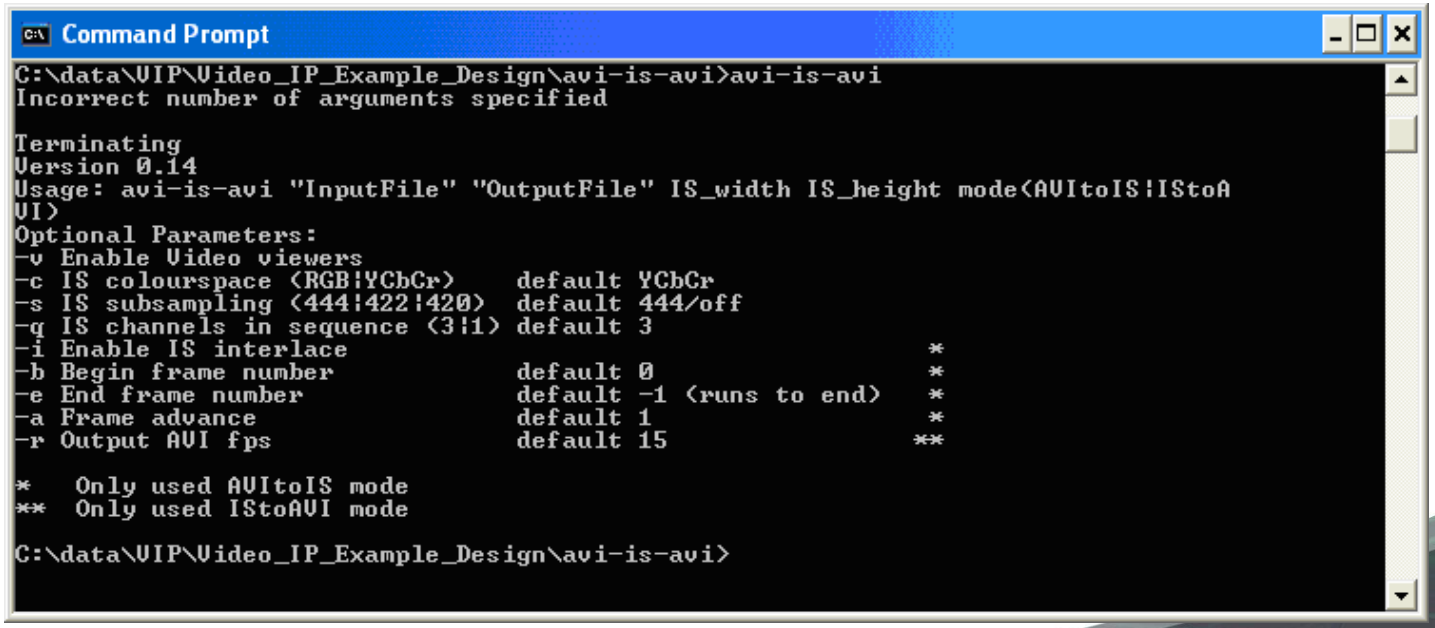
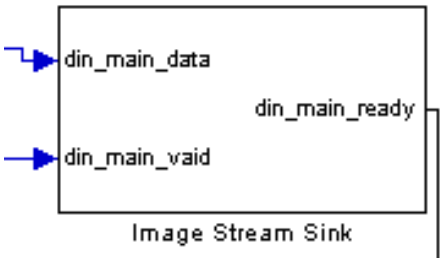
Simulation: Generate Video Binary File

- Command Line Utility converts AVI file to a binary file for use within DSP Builder environment
- Also converts binary output to an AVI file for convenient playback



Simulation: Video Output

1



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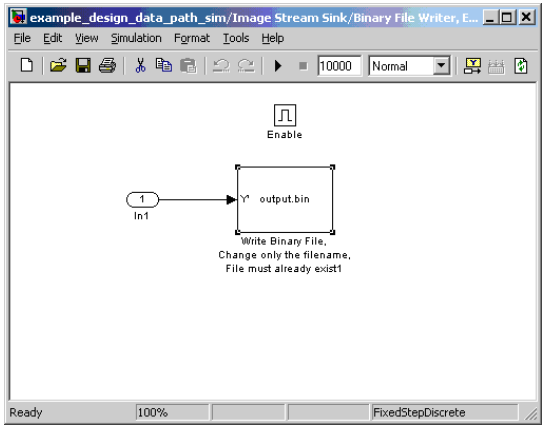

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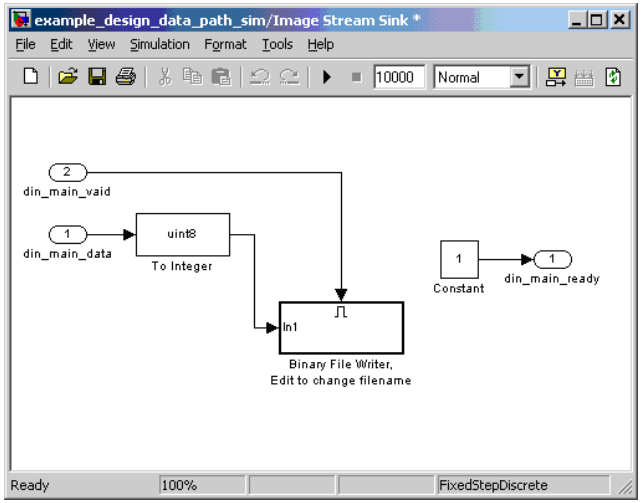

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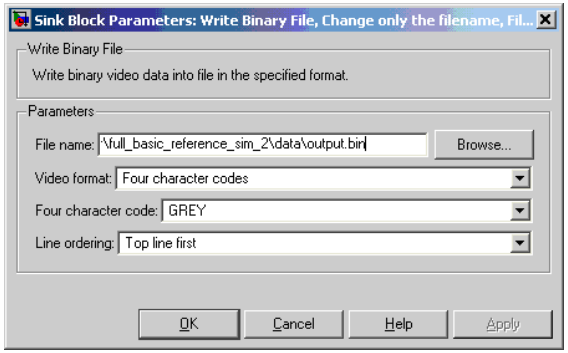

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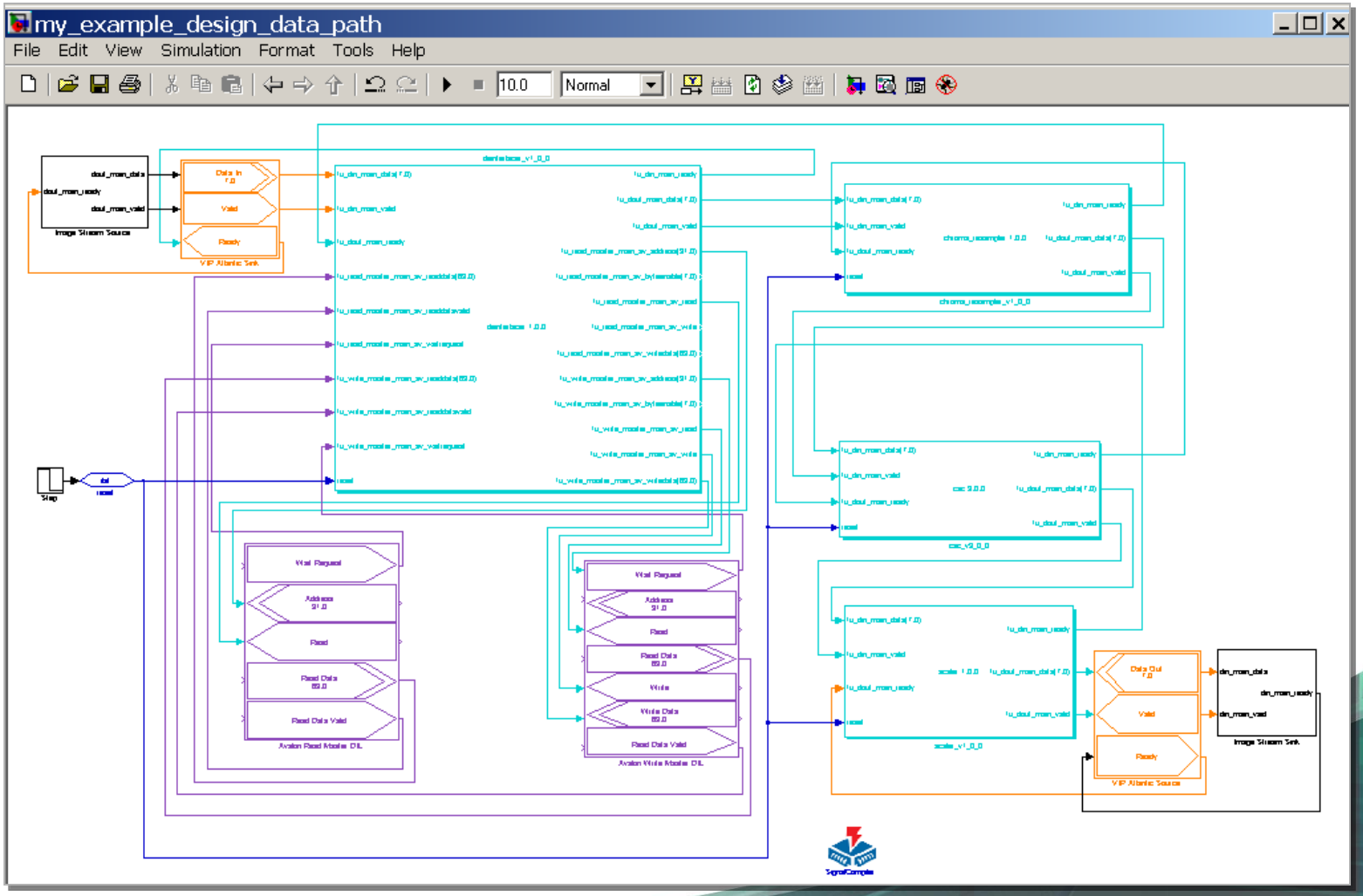
Simulation: Upconversion Subsystem



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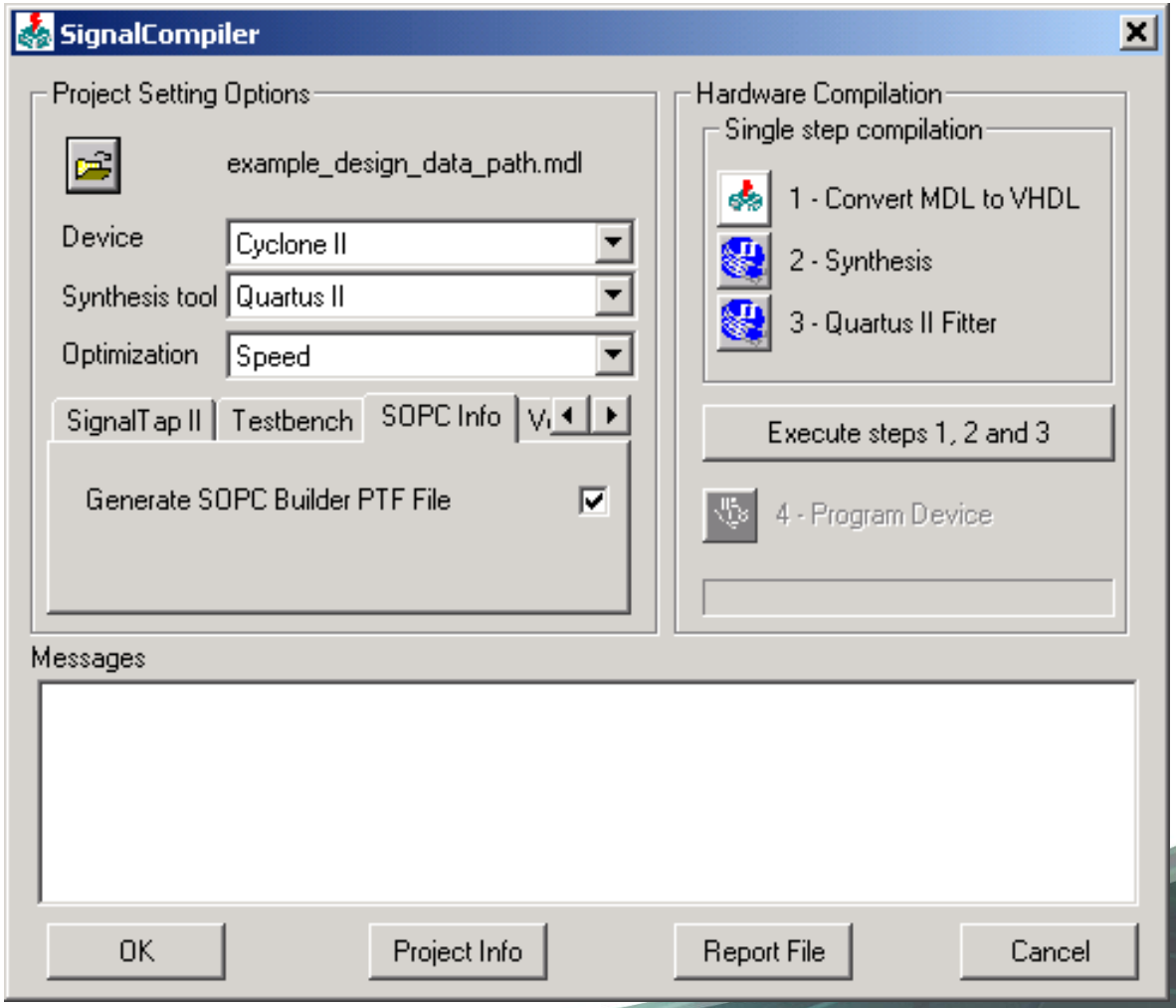
Convert to VHDL: Signal Compiler



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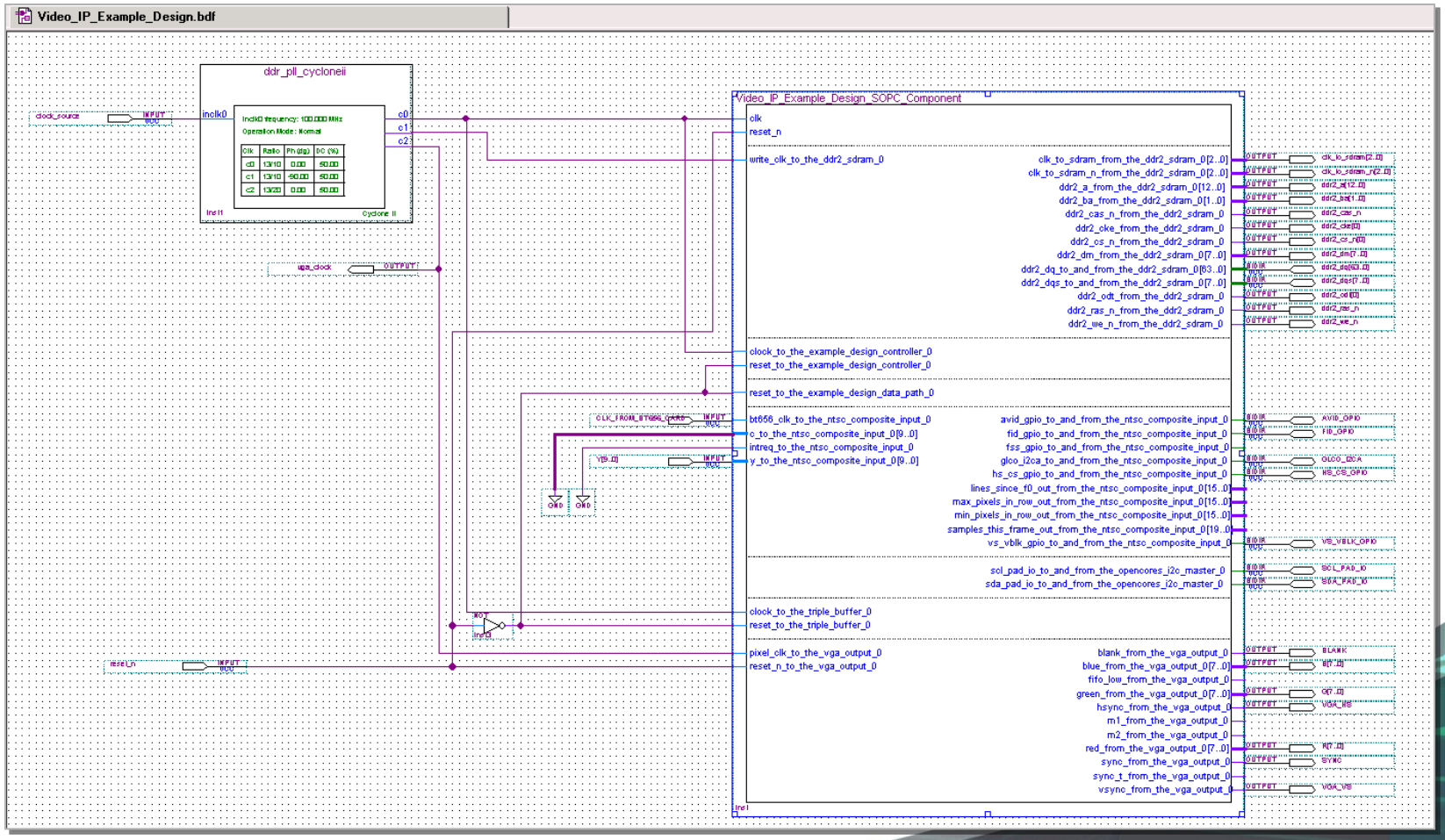
Top-Level Design File in Quartus II



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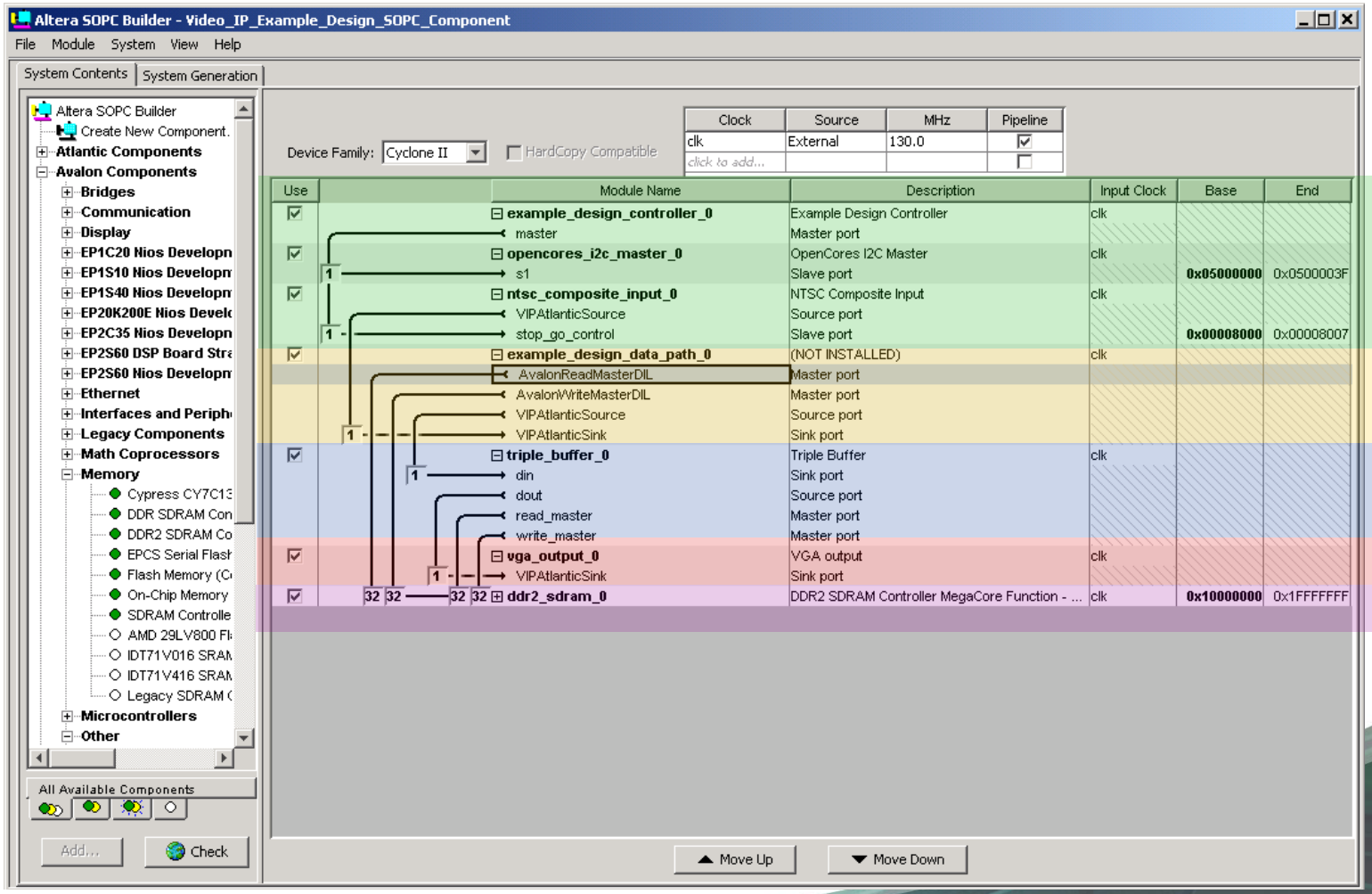
System Integration: SOPC Builder



NTSC BT.656

DSP Builder - Data Path

Buffer

VGA Out

DDR2

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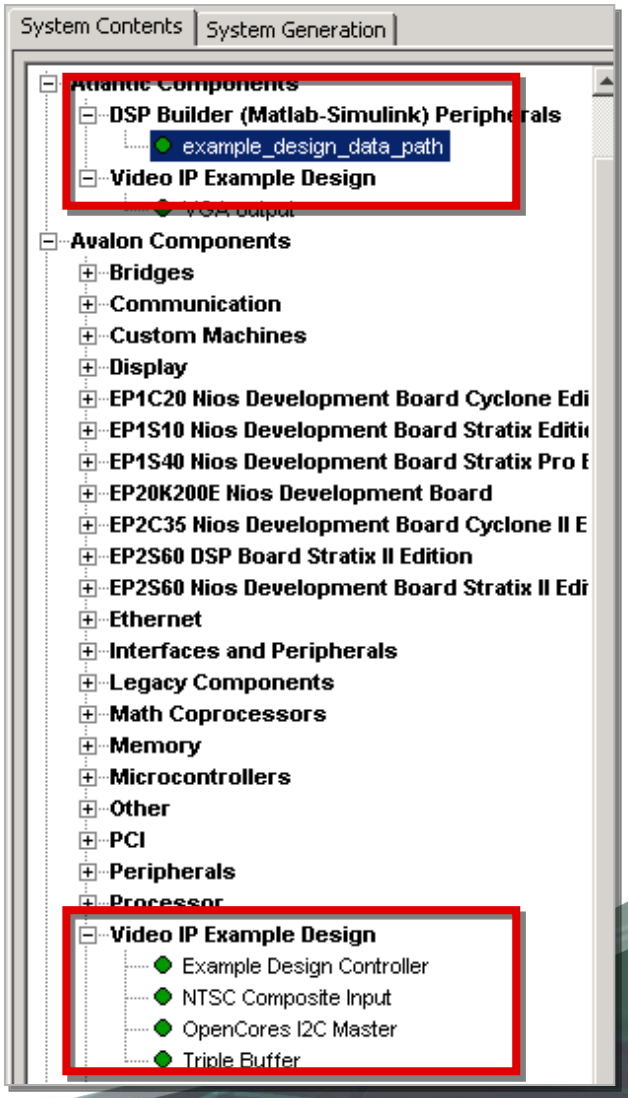
Custom Hardware

- Generated custom video interfaces IP
  - Available within reference design package



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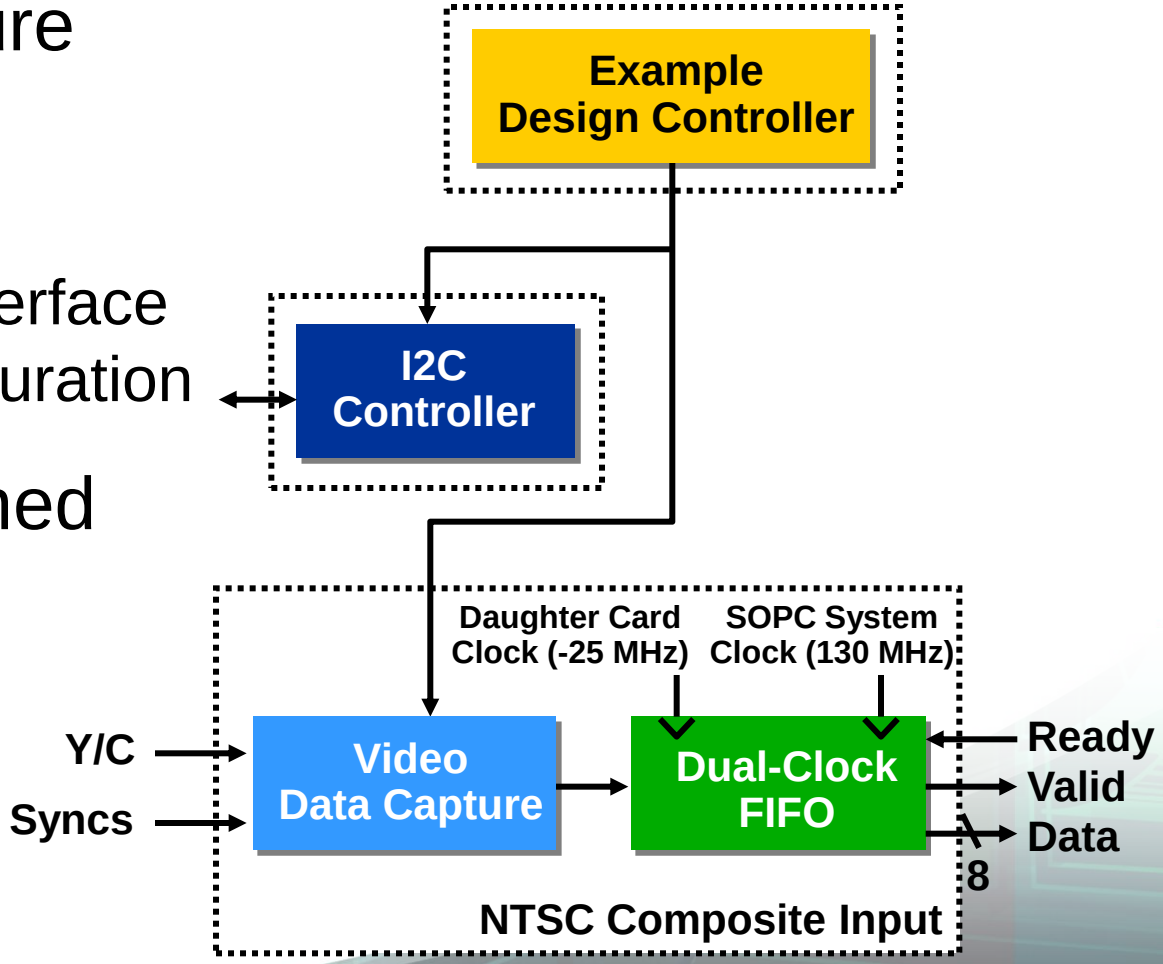
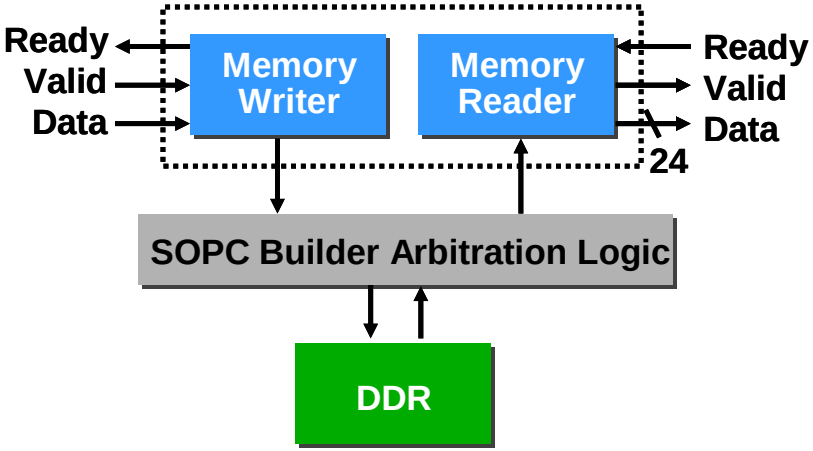
NTSC Video Input

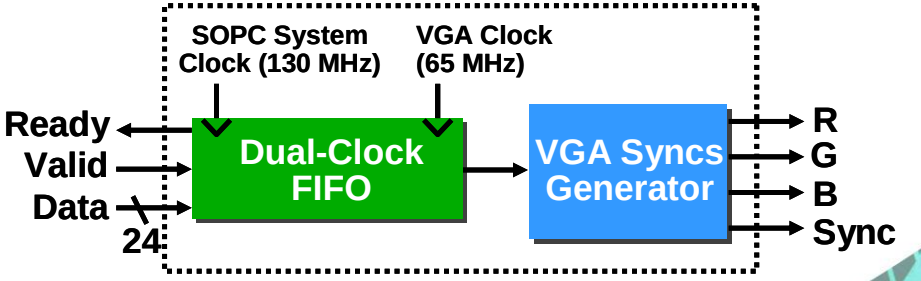
- Video data capture with TI TVP5146 decoder
  - I2C is control interface for device configuration
- Controller designed in HDL
  - Imported into SOPC Builder



Triple Buffer and VGA Output

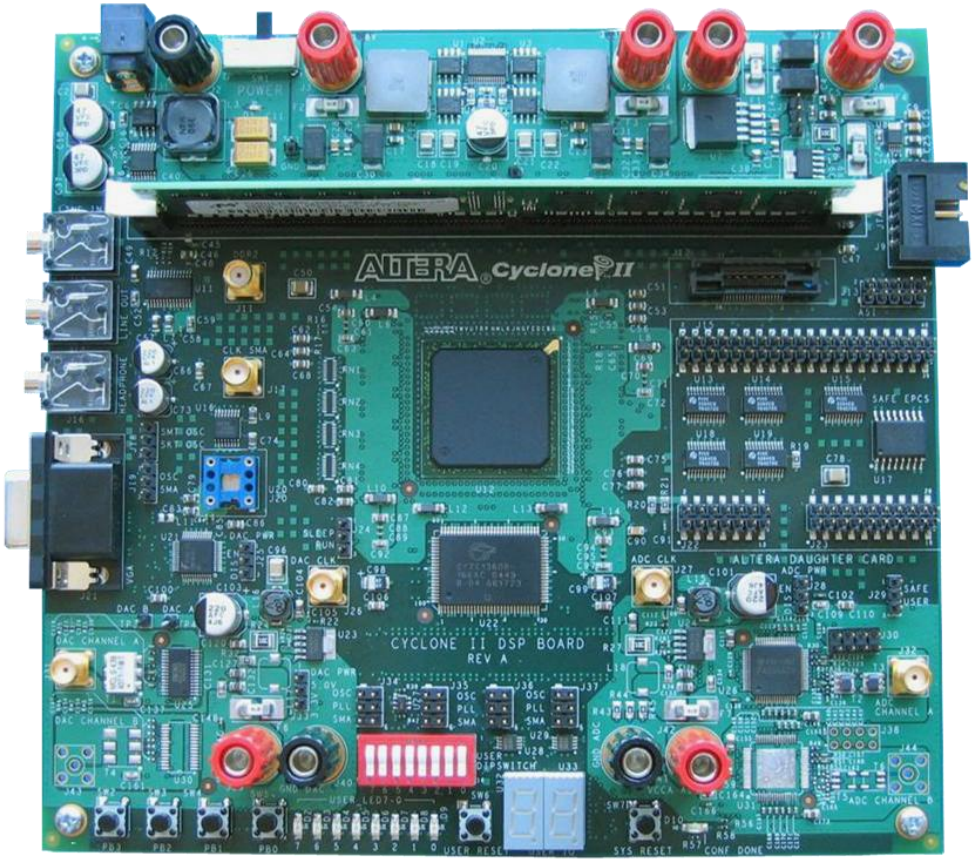
- Allows inputs and output to run asynchronously and at different frame rates
  - Video output: 1,024 x 768 progressive at 30 frame/s
  - VGA output: must run at least 60 fps
- HDL design, imported into SOPC Builder





SOPC WORLD

Video Development Kit, Cyclone II Edition



- Device: EP2C70
- Bundled software:
  - Quartus II development kit edition
  - DSP Builder
  - MATLAB/Simulink evaluation software
  - Altera OpenCore® Plus evaluation IP
- Includes video input daughter card

SOPC WORLD

Video Input Daughter Card

- Features:
  - Dual composite video inputs (NTSC & PAL)
  - Compatible with other Altera development boards that feature a Santa Cruz connector

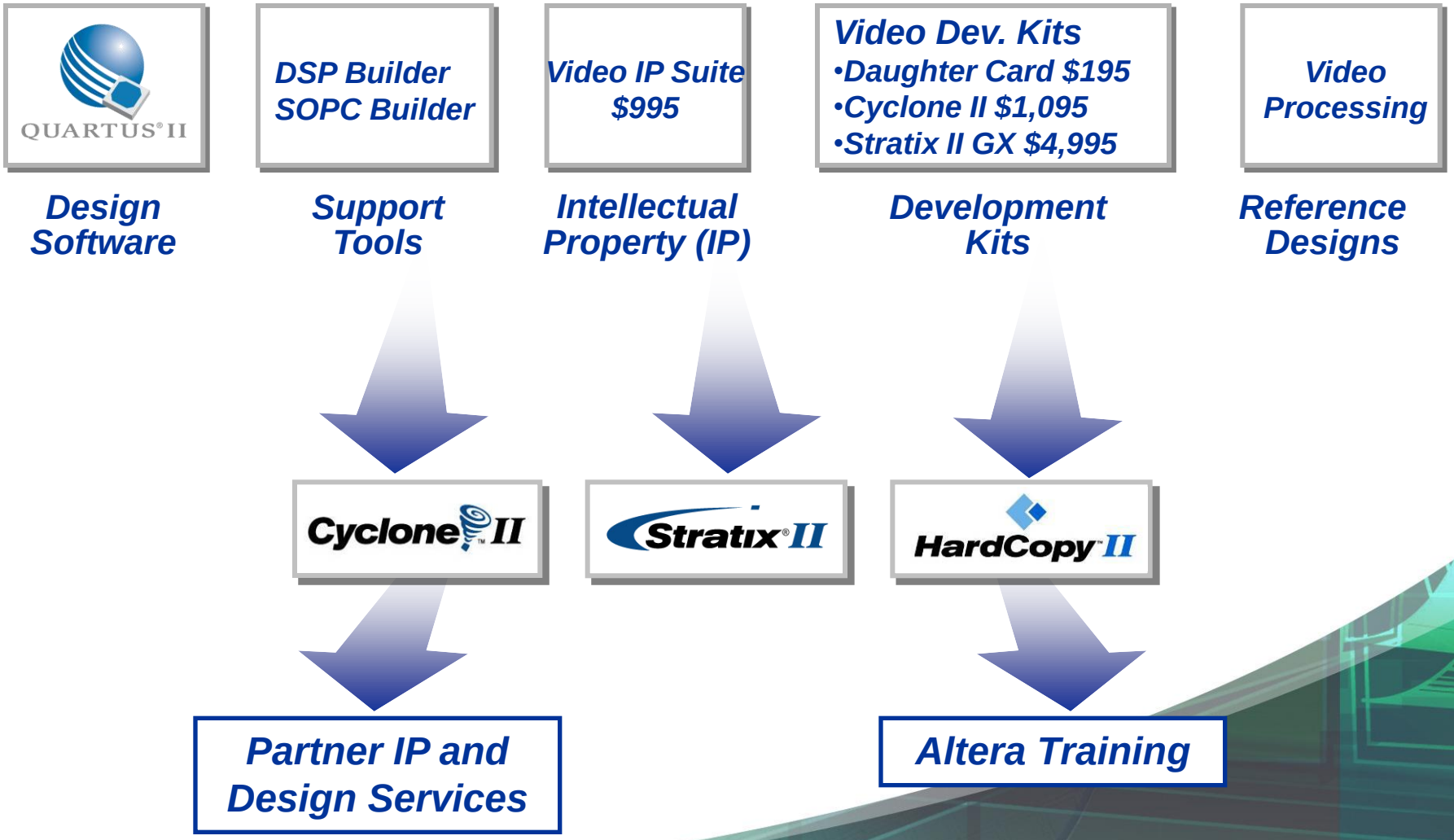
SOPC WORLD

Download to Hardware

- Resource utilization
  - 9,500 logic elements, 48 M4K, 11 multipliers
  - Fits in EP2C15 device
- Program Video Development Kit, Cyclone II Edition
- Hardware debug
  - JTAG/SignalTap® logic analyzer

Getting Started

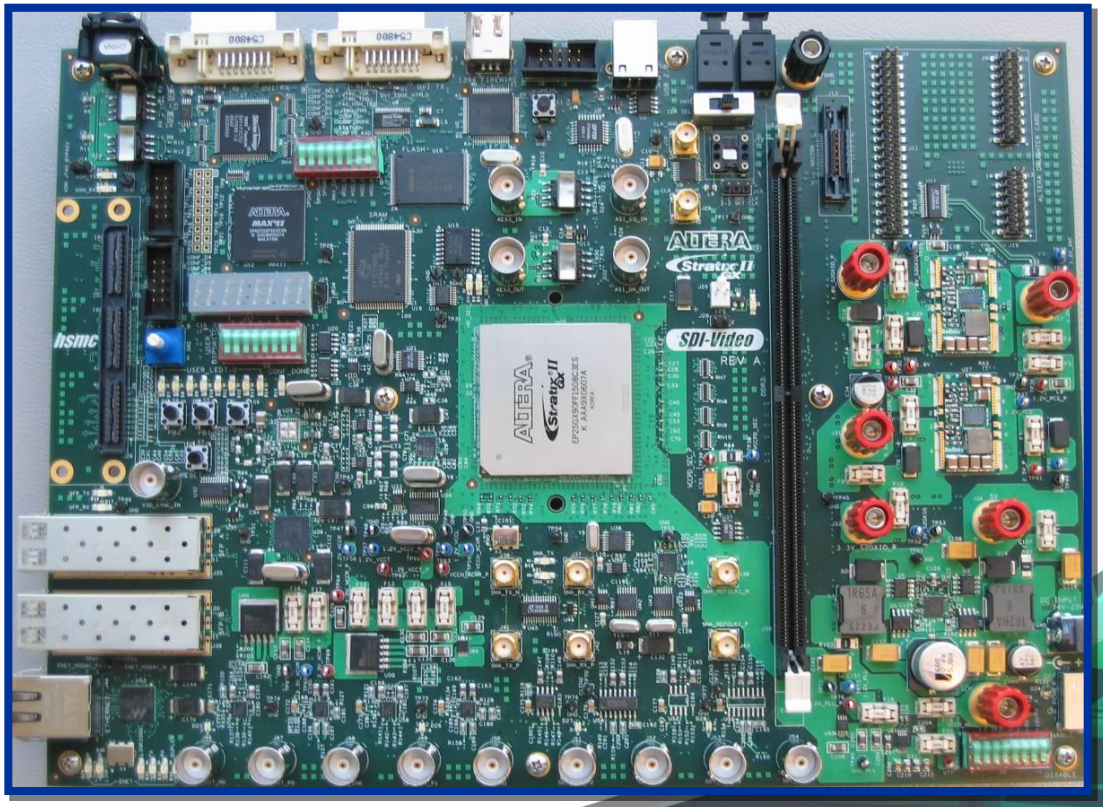
Altera Video Solutions



SOPC WORLD

Audio Video Development Kit, Stratix II GX Edition

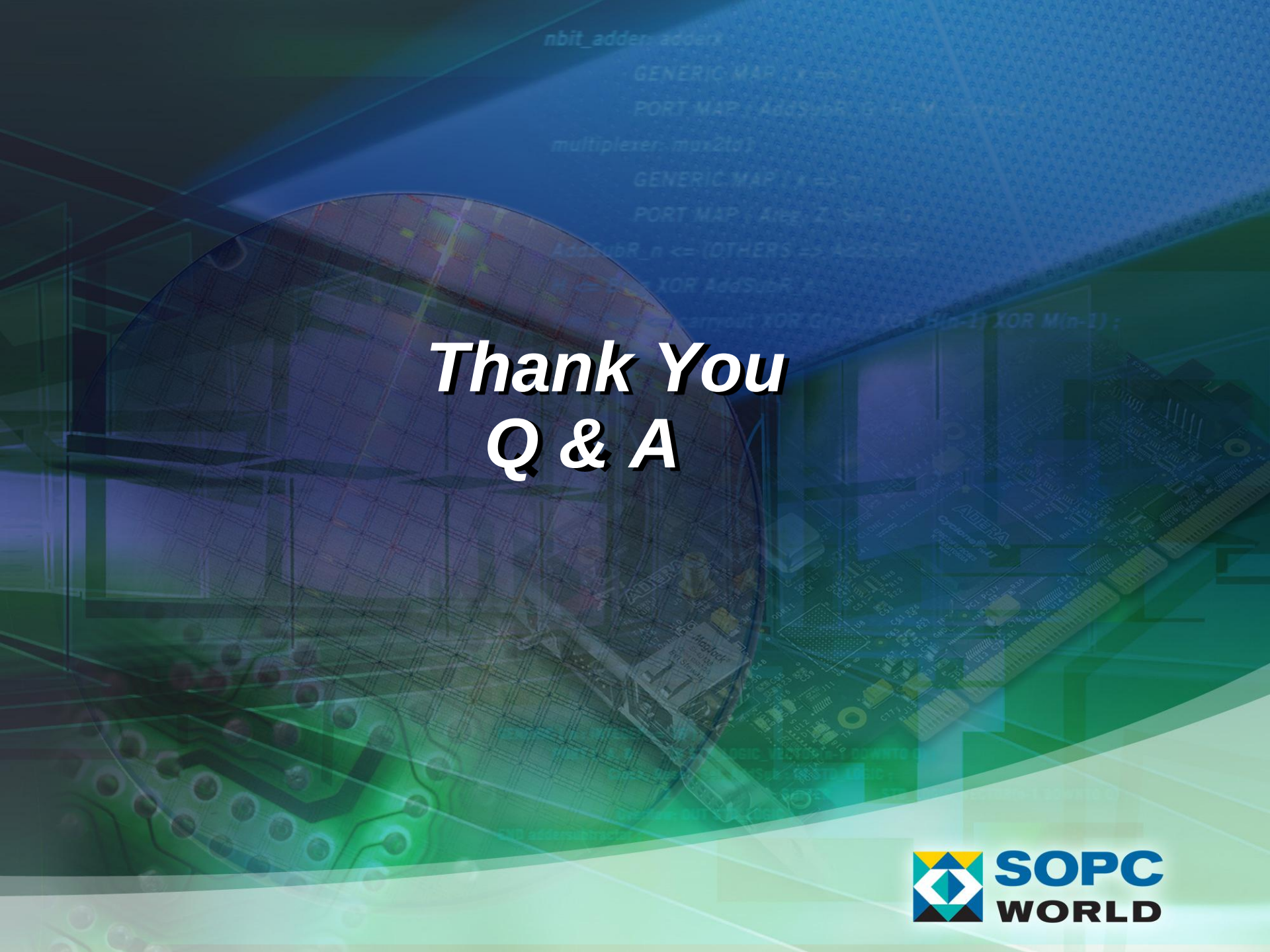
- Device: EP2SGX90
- Video interfaces:
  - 4 SDI/HD-SDI channels
  - DVI
- Audio interfaces:
  - AES3/EBU, SPDIF
- High-speed data interfaces:
  - ASI
  - FireWire (IEEE1394)
  - USB 2.0
  - 10/100/1000 Ethernet
- Bundled with SDI and video processing reference design



SOPC WORLD

Get Started Now

Product	Description	Ordering Code	Price
Video and Image Processing Suite	9 video and image processing IP cores	IPS-VIDEO	$995
Video Development Kit, Cyclone II Edition	Cyclone II DSP board + video input daughtercard	DK-VIDEO-2C70N	$1,095
Video Input Daughter Card	2 composite video inputs (NTSC/PAL Support)	DC-VIDEO-TVP5146N	$195
Audio Video Development Kit, Stratix II GX Edition	Stratix II GX video board with ASI, SDI, DVI, Gigabit Ethernet, FireWire, USB2.0, S/PDIF, AES	DK-VIDEO-2SGX90N	$4,995


Thank You
Q & A
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