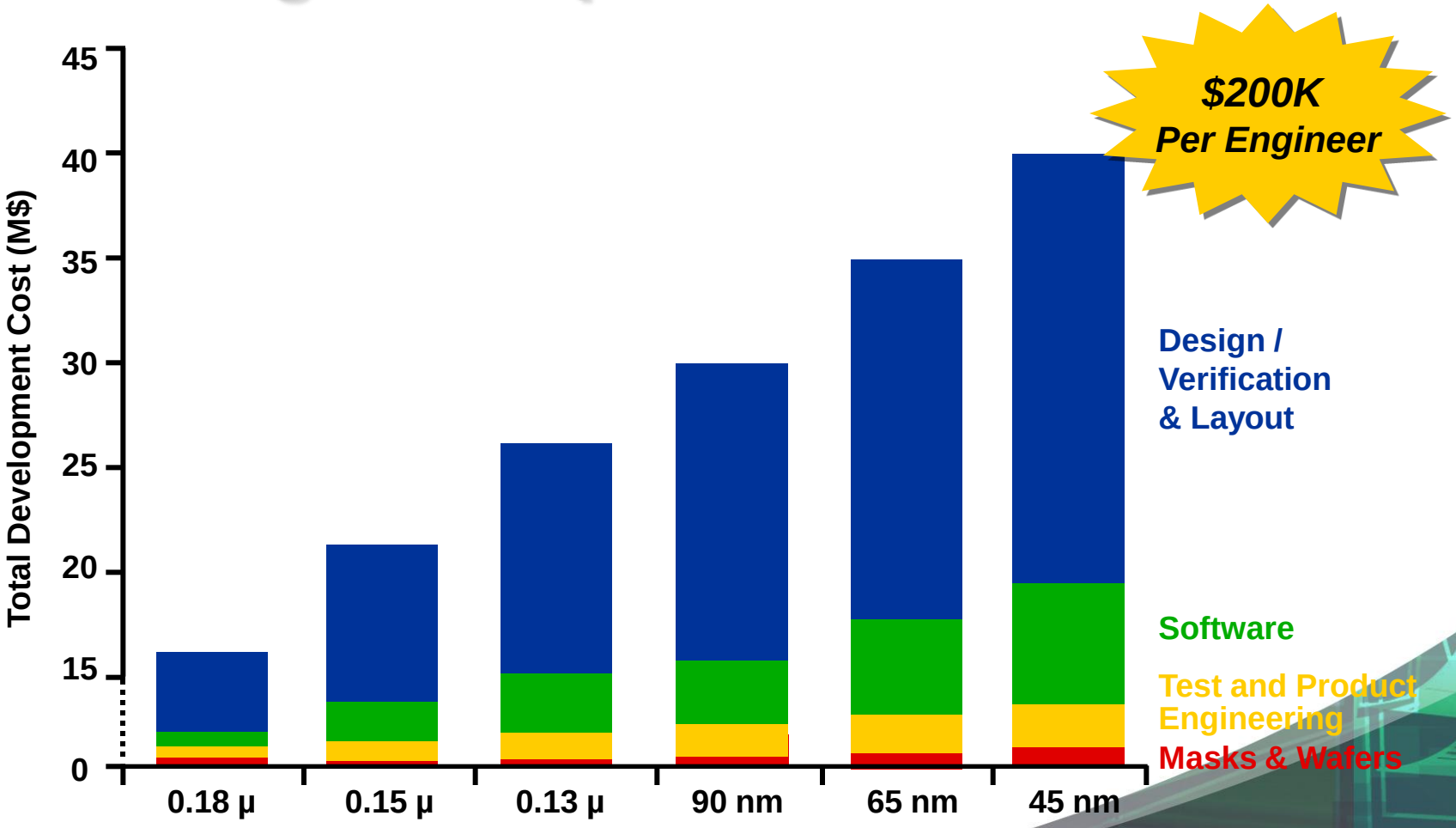
Seamless, Risk-Free FPGA-to-Structured ASIC Migration Flow

SOPC WORLD

Increasing Development Cost



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Constant Increase in Mask Charges

- Costs increase exponentially as process geometry decreases
  - New mask making technologies required
    - Drawn geometries are smaller than wavelength of light used to expose masks
    - Optical proximity correction (OPC) used to pre-distort shapes
  - Tighter geometry decreases mask yields
- Mask costs for structured ASICs substantially lower than standard cell ASICs
  - Vendor amortizes pre-fab base costs over many designs
  - Customer pays only for customization of specific layers
    - 2 – 5 masks vs. 40+ masks for standard cell ASICs

SOPC WORLD

Risks in Digital Designs

- Design implementation risks
  - 67% first-spin failure rate for 130-nm designs in 2003*
  - 40% failure rate after three design spins*
- Product feature risks
  - Uncertainties during initial product definition
  - Field trials are necessary
- Market adoption risks
  - Predicting volumes
  - How much should a company risk to introduce new products?

*Source: Collett and Associates

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Value Proposition for Prototyping

- Faster time-to-silicon
- Faster and more comprehensive verification
- Earlier software development
- Costly ASIC re-spins prevented
- Field trials and test marketing

Over 40% of ASIC Designers Prototype Today

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Historical Obstacles to ASIC Prototyping

- Before: FPGAs and ASICs used different design flows
- Today: Altera's FPGAs and HardCopy structured ASICs support ASIC tools
  - Synthesis: Design Compiler FPGA
  - Simulation: VCS, Incisive, and ModelSim®
  - Formal Verification: Formality and Encounter Conformal
  - Static Timing Analysis: Primetime
- Before: FPGAs were too small
- Today: 78% of ASIC designs can fit on a single Stratix® II FPGA
  - Stratix II FPGAs and HardCopy II structured ASICs
    - 2.2 million useable ASIC gates
    - 9 Mbits of configurable SRAM
    - 1.6 million additional gates for digital signal processing (DSP) functional blocks

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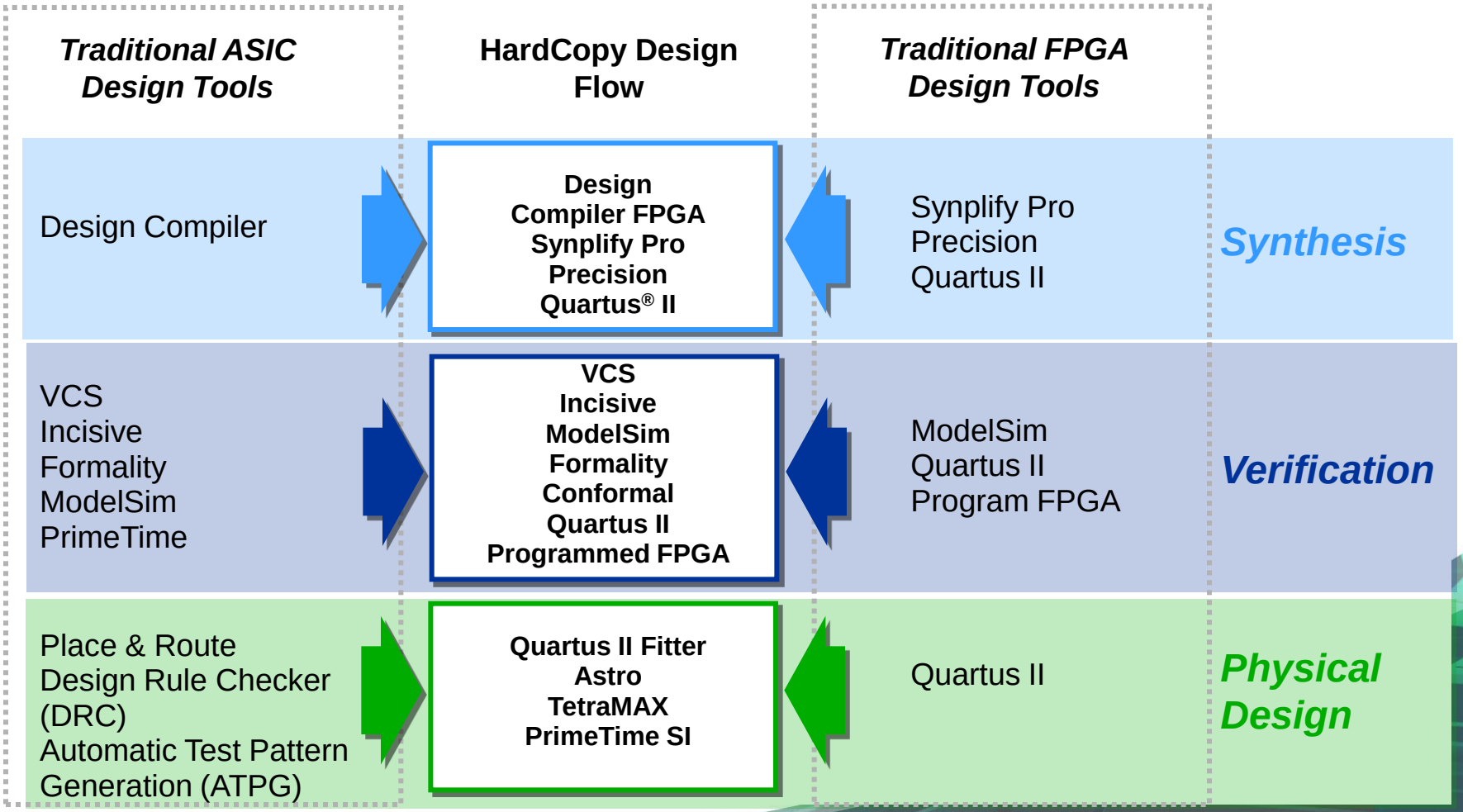
Flexible HardCopy Design Methodology



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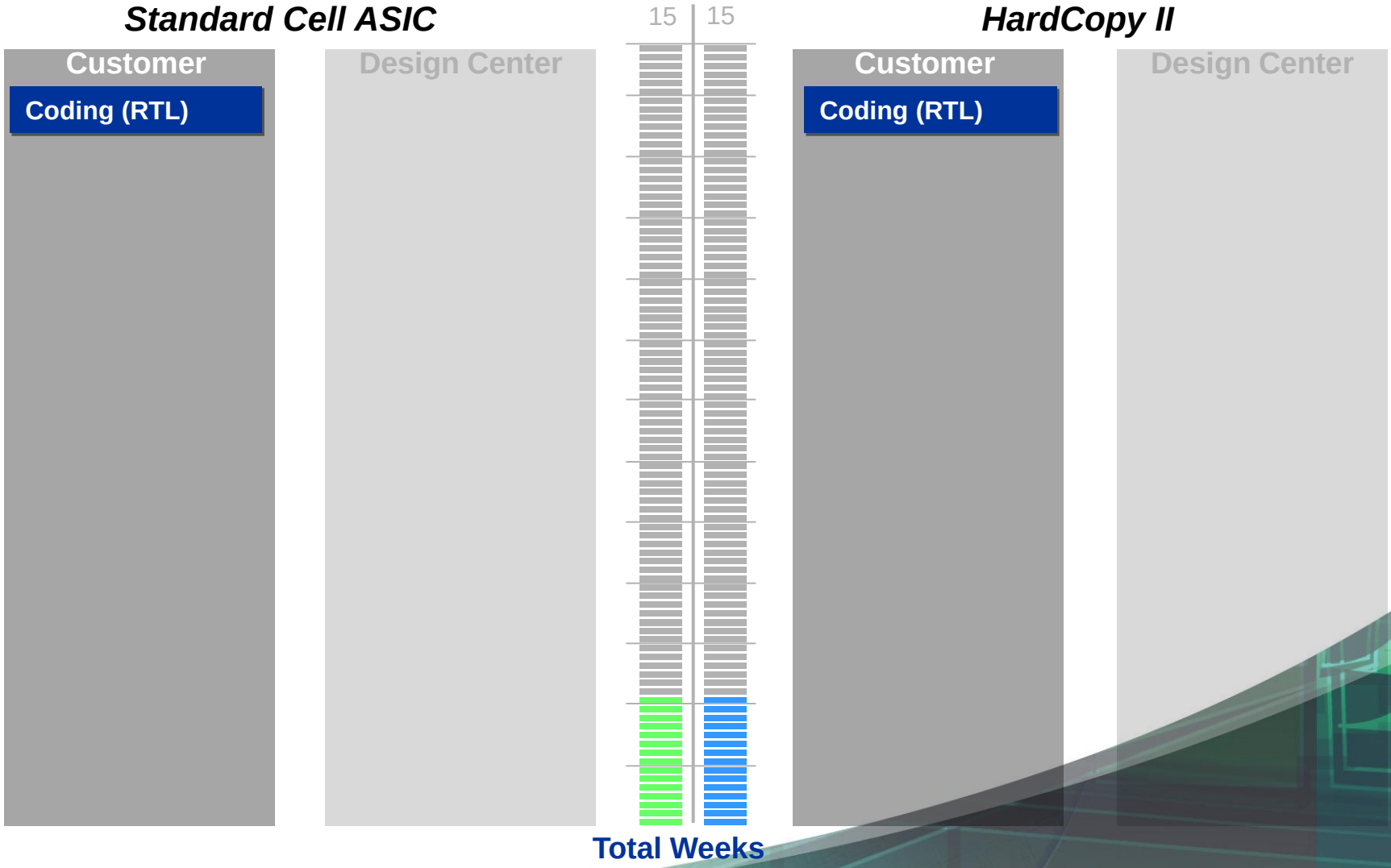
Walking Through the Design Process

Comparing ASIC vs. HardCopy Design Process

- Apple-to-apple comparison of design implemented in structured or standard cell ASICs vs. HardCopy structured ASICs
- Basic assumptions:
  - Moderate gate count: 1M-2M gates
  - Moderate performance: 100-200 MHz
  - Skipping ASIC prototyping for the non-HardCopy implementation
- Comparing
  - Time to market (TTM)
  - Time to mass production (TTP)
- Tool, non-recurring engineering (NRE), major last-minute design change support (ECO support) costs are not factored in

RTL Coding



- ASIC and HardCopy code generation are very similar.

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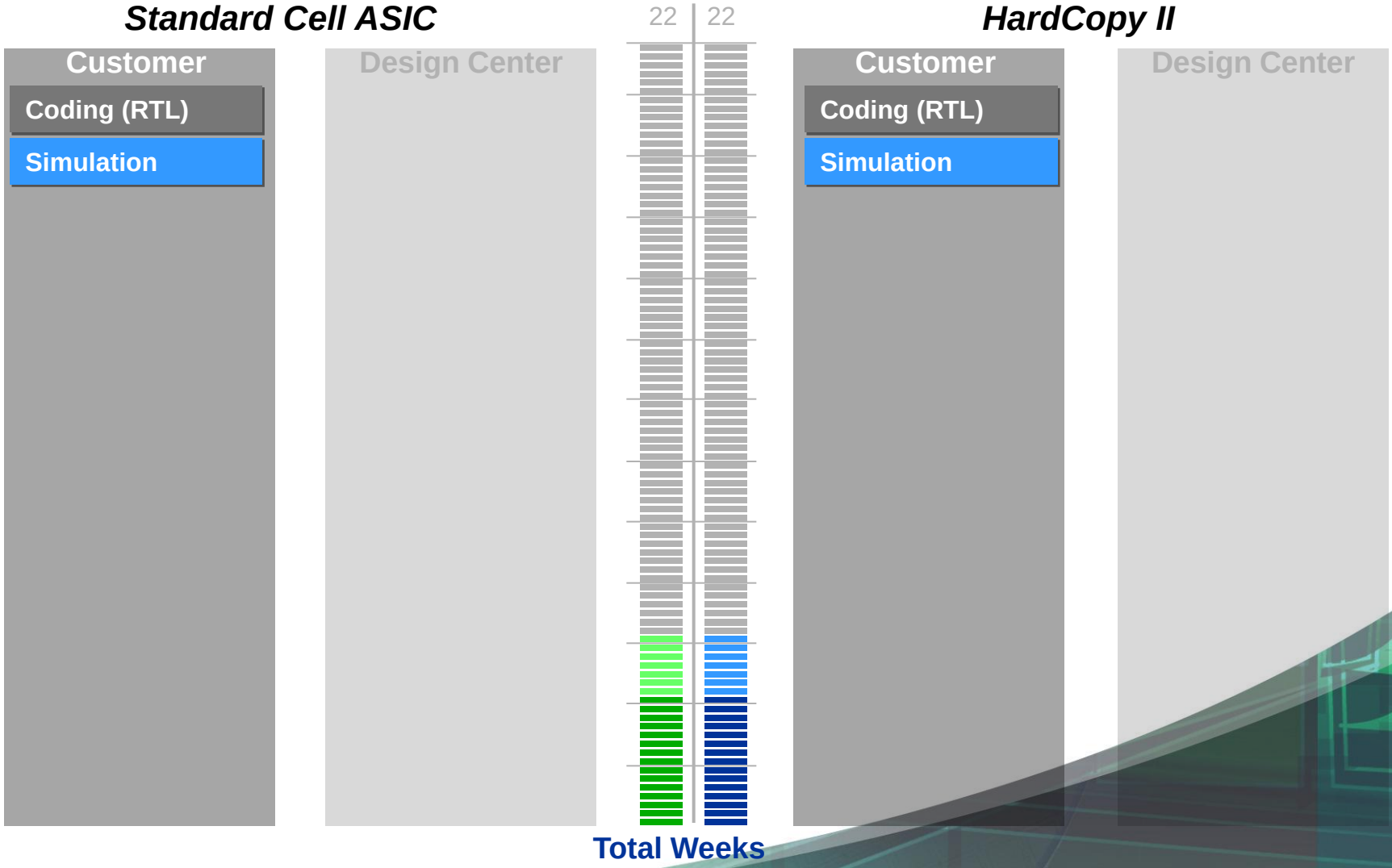
Behavior Simulation



- ASIC and HardCopy behavior simulation are very similar.

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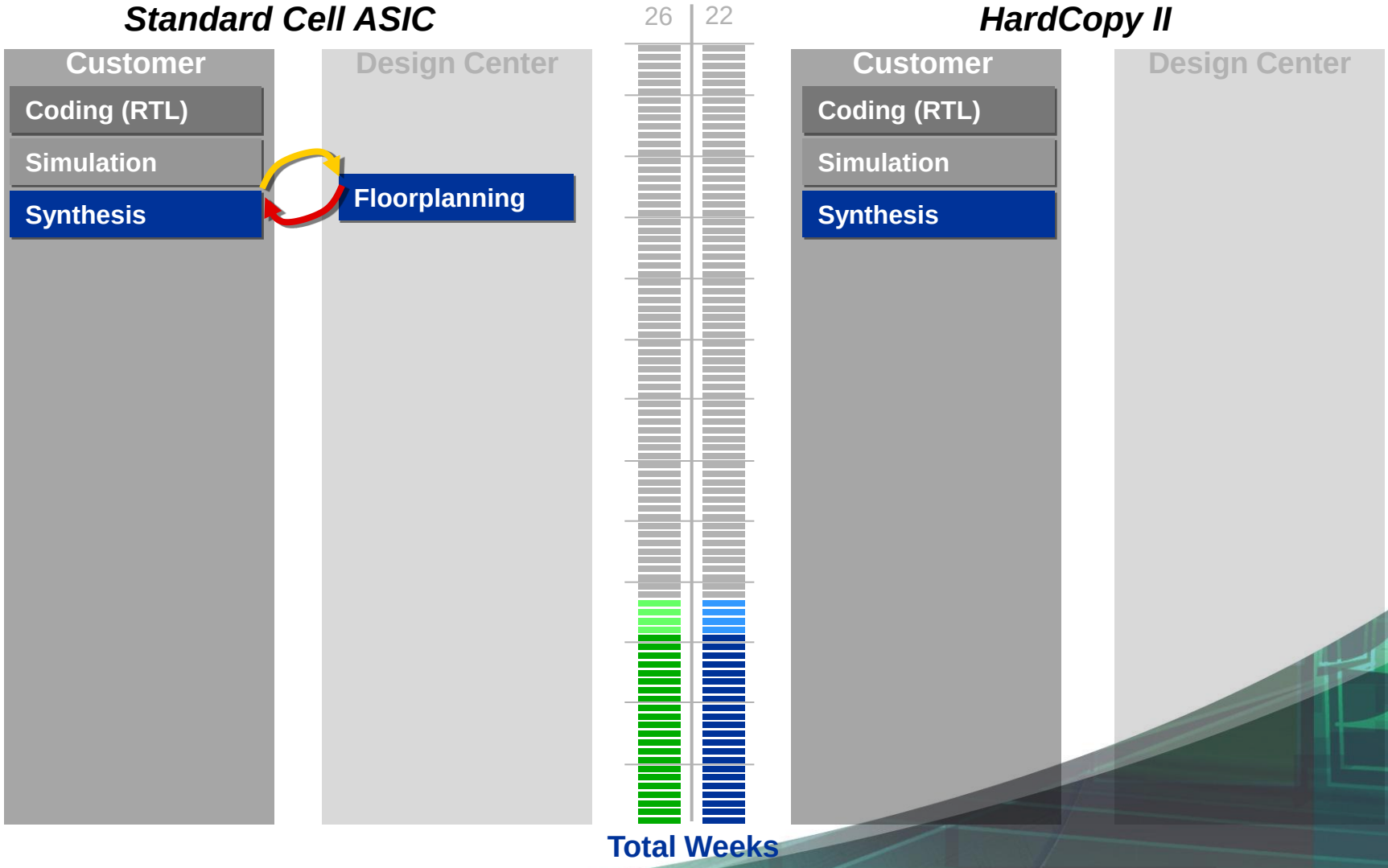
Synthesis



- ASIC synthesis: Design Compiler (also requires Design Center Support for timing extraction)
- HardCopy synthesis: DC FPGA, Synplify, Precision, and Quartus II software

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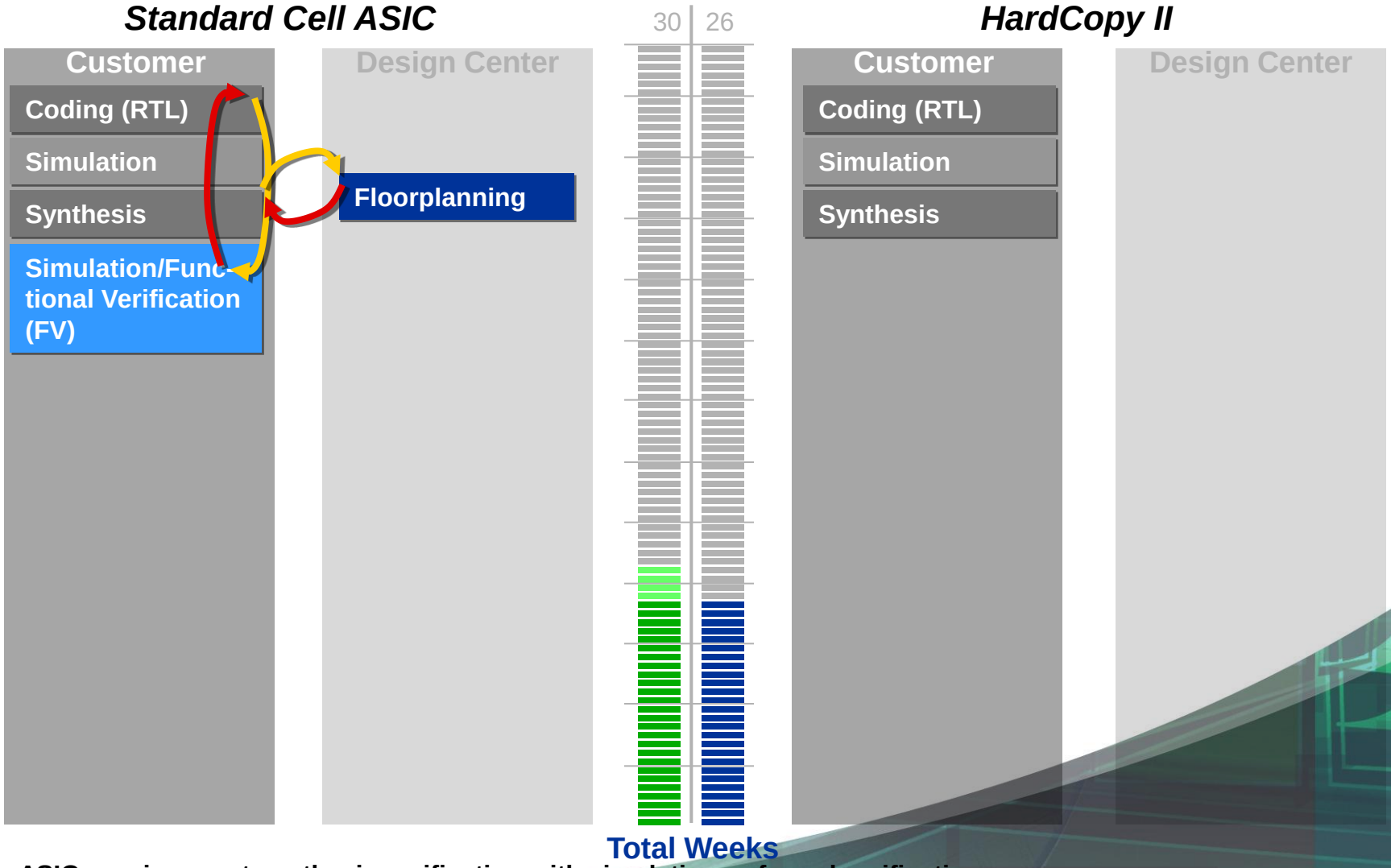
Post-Synthesis Design Verification



- ASIC requires post-synthesis verification with simulation or formal verification.
- HardCopy designs do not require post-synthesis verification.

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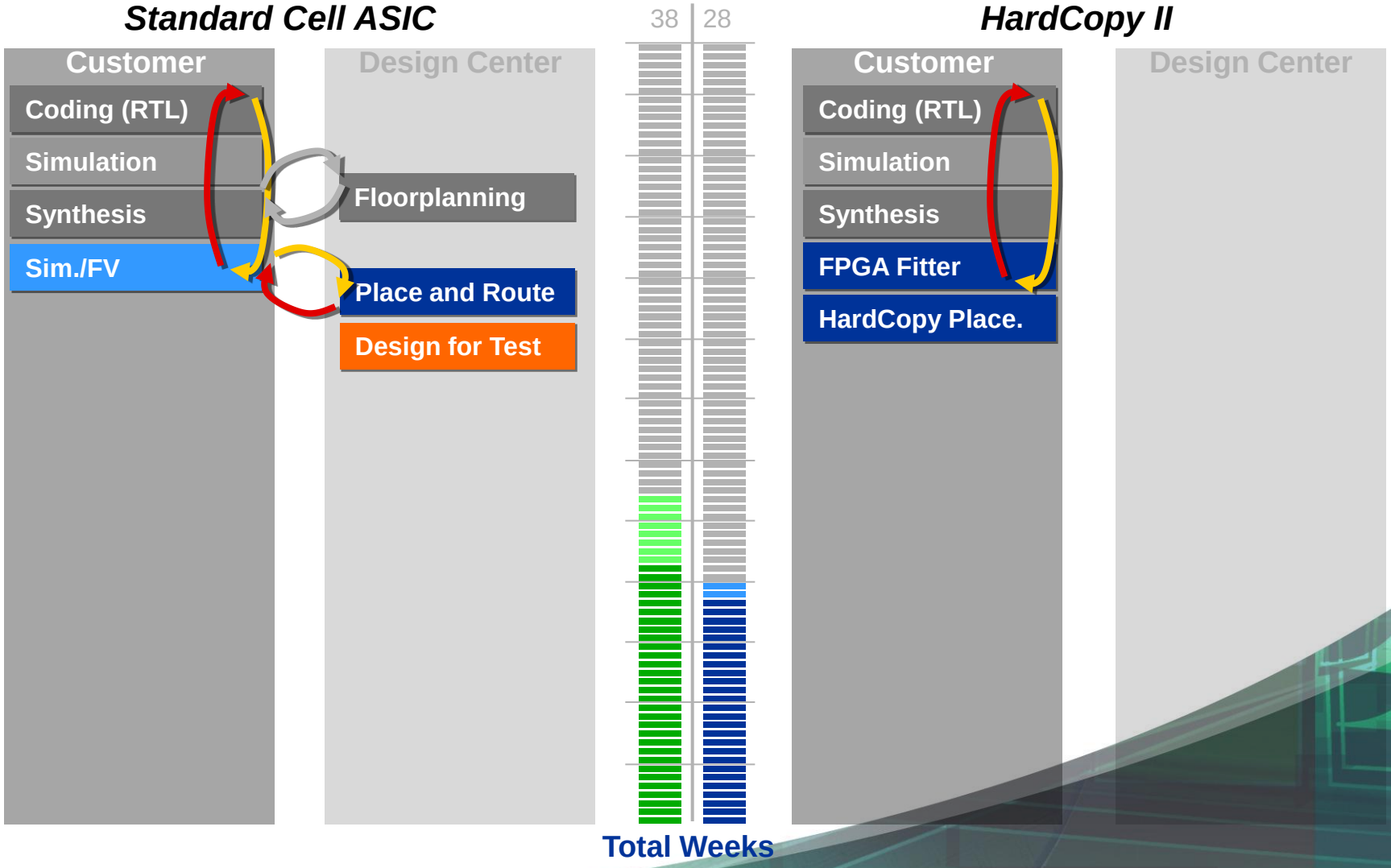
Physical Design and Timing Closure



- Place and route for ASICs requires extensive Design Center involvement.
- HardCopy placement is done by design engineer with Quartus II software.

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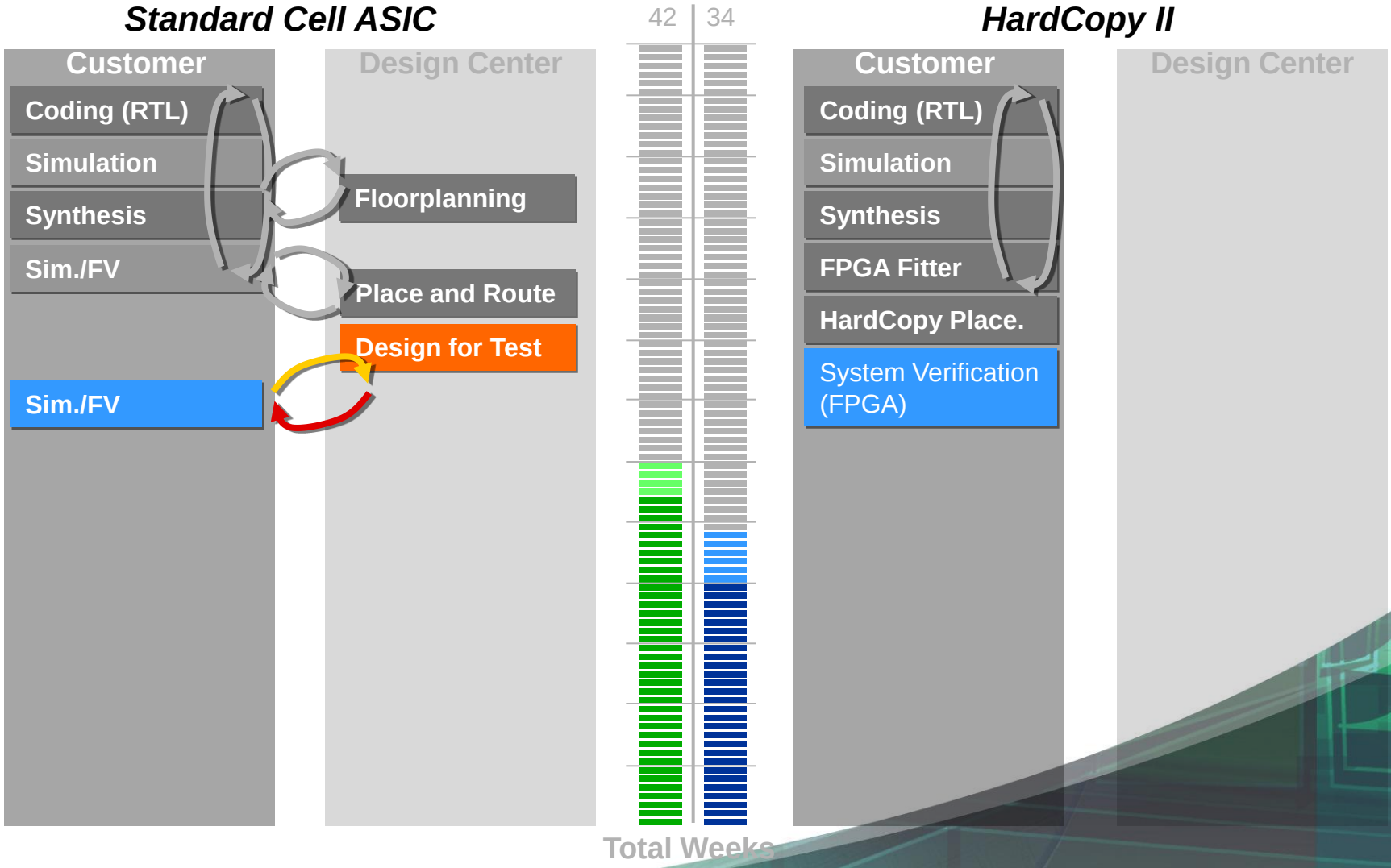
Design Verification vs. System Verification



- ASIC require post place-and-route verification before tape-out.
- HardCopy FPGA companion is used for system verification.

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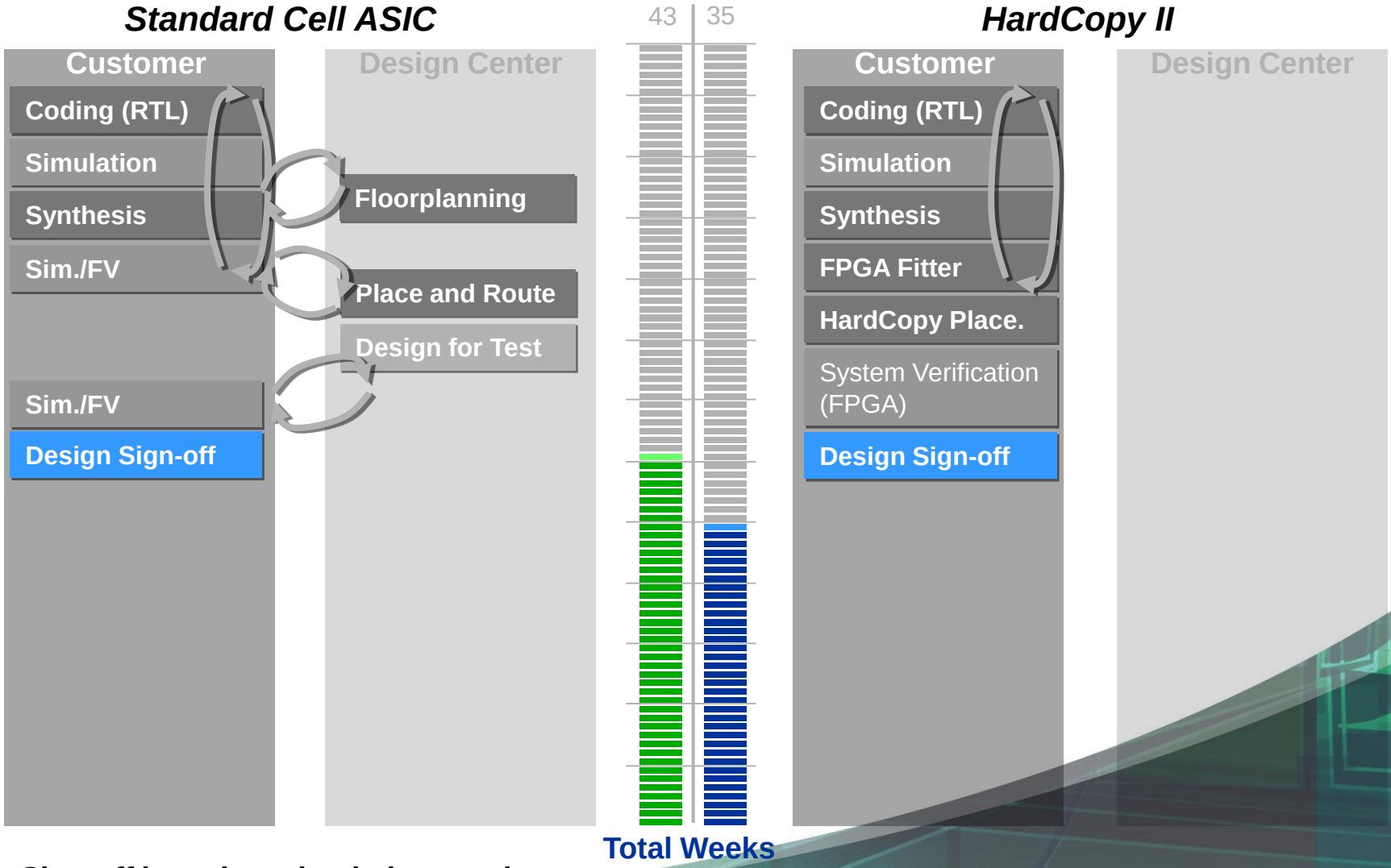
Design Sign-off



- Sign-off based on simulation results.
- Sign-off based on comprehensive in-system verification.

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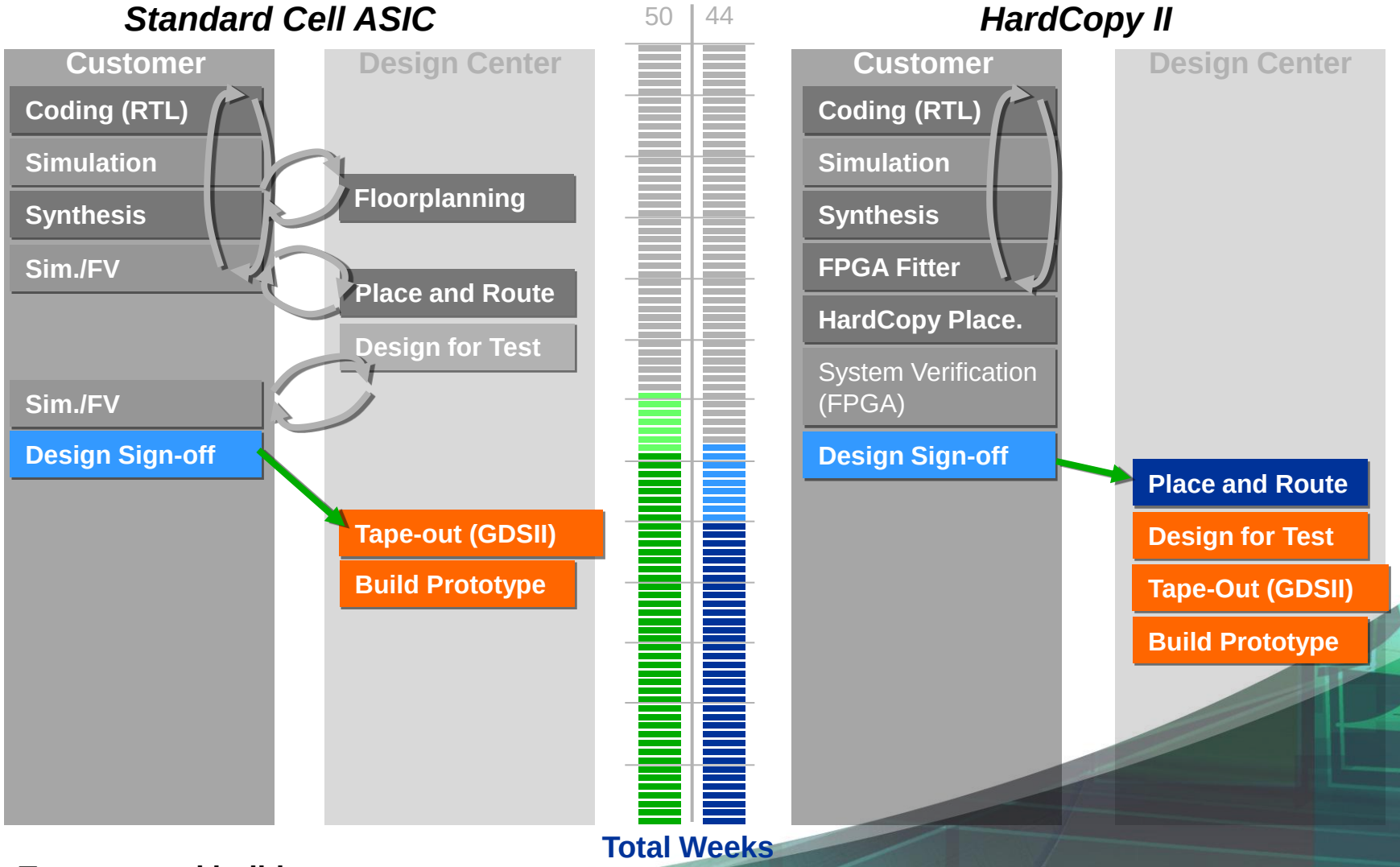
Tape-out and Prototype Build



- Tape-out and build prototypes.
- Single place and route, tape-out, and build prototypes.

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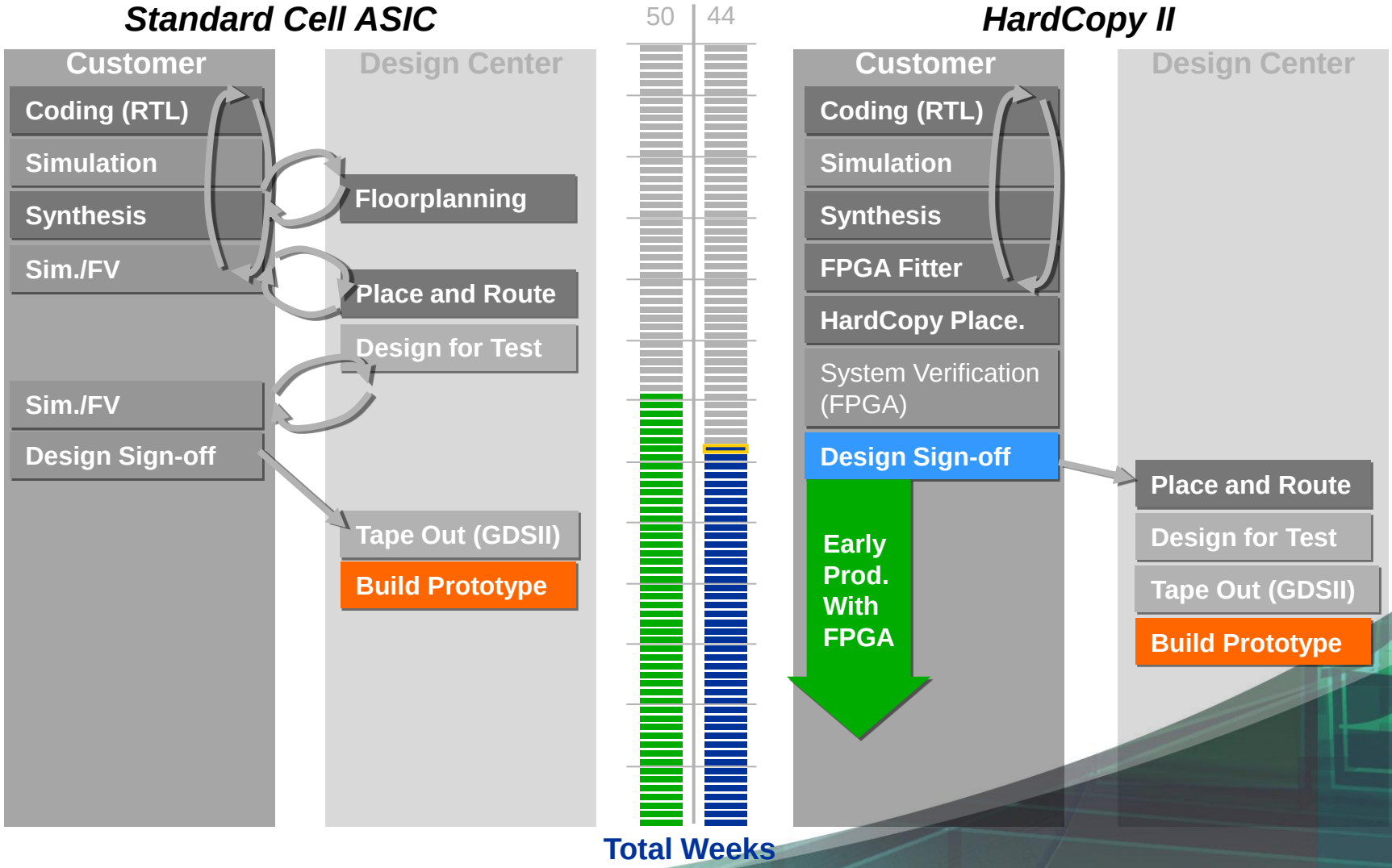
Early Production with FPGA



- Wait for prototypes. Everything on standby
- Support early production with FPGA after sign-off while prototypes are being built

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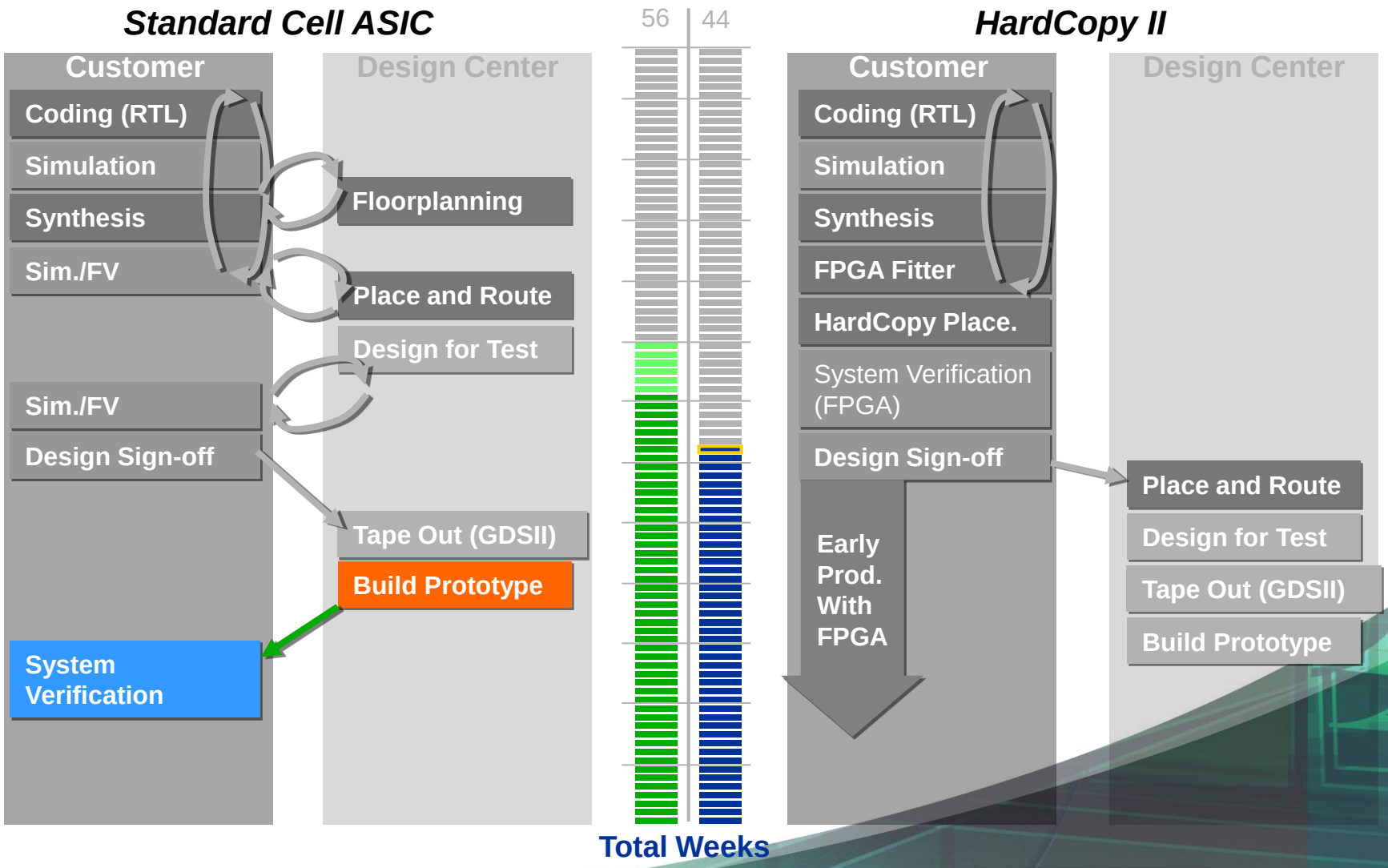
ASIC Prototypes Are Back for System Verification



- System verification begins with ASIC prototypes.
- System verification for HardCopy devices already complete.

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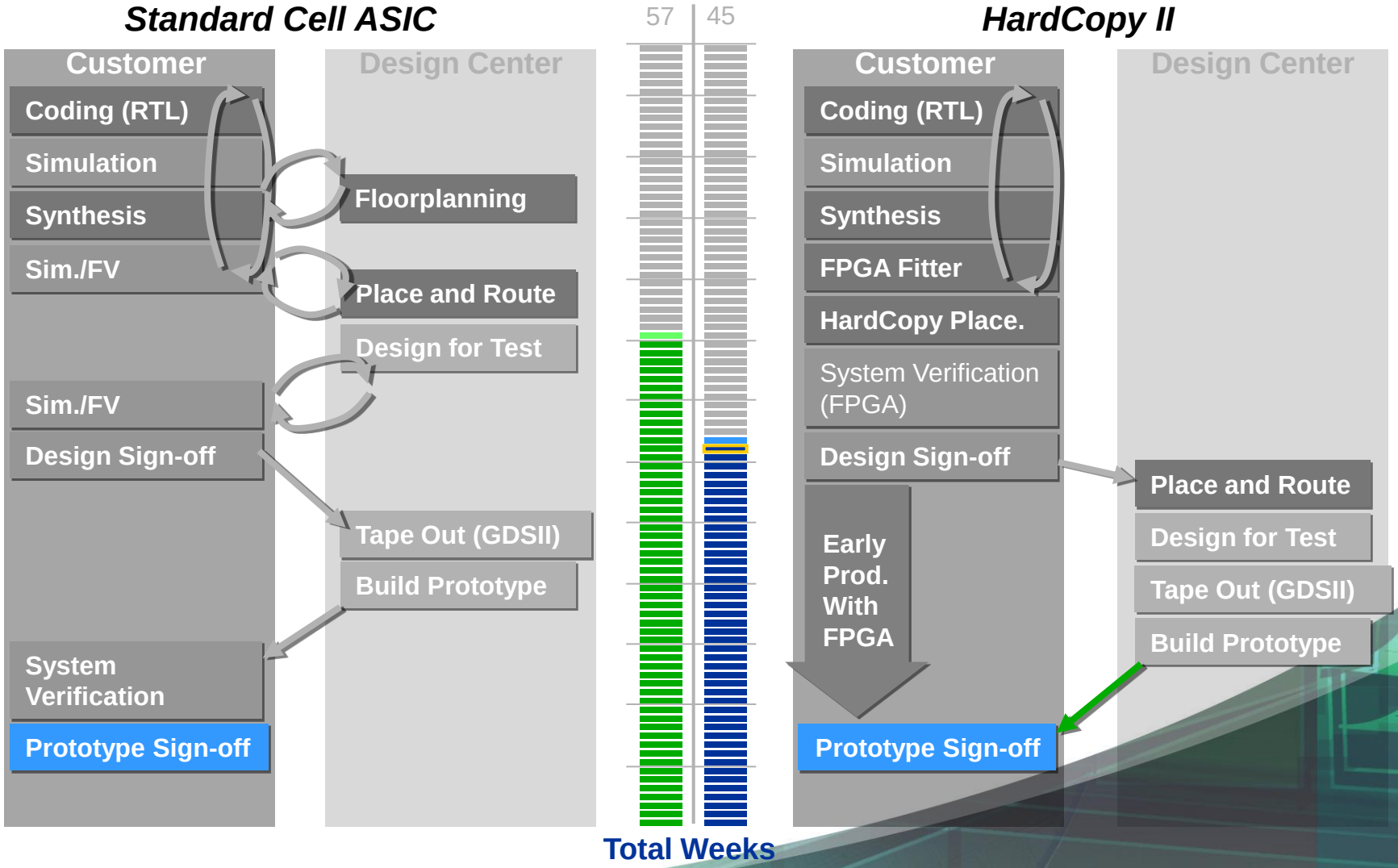
Final Prototype Signoff



- Final prototype sign-off is the same for ASIC and HardCopy devices.

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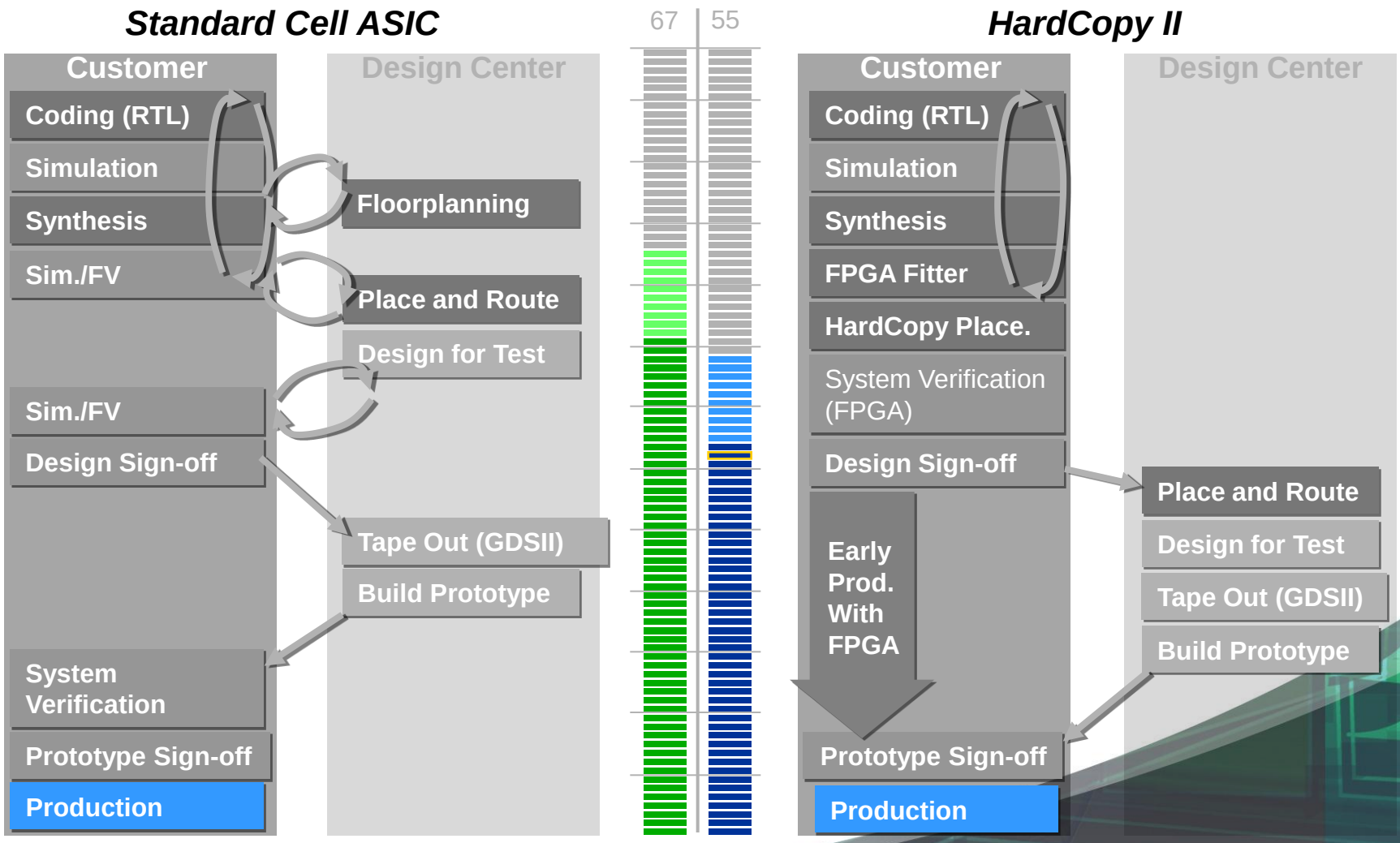
Ready for Production



- HardCopy II devices have 23-week time-to-market advantage and 12-week time-to-production advantage.

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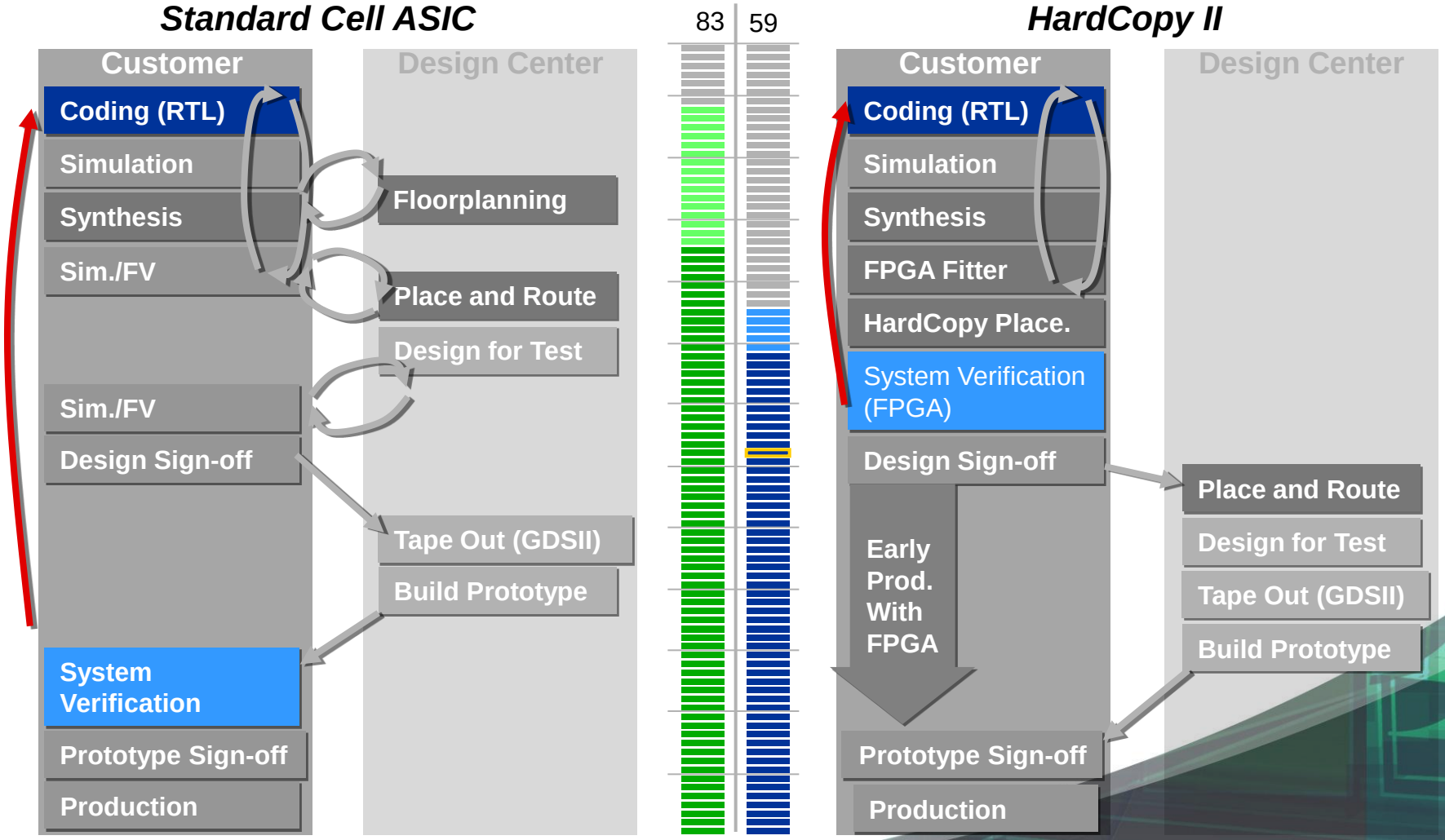
Impact of an ECO during System Verification



- Failed system verification requires an ASIC respin.
- Failed system verification requires reprogramming the FPGA

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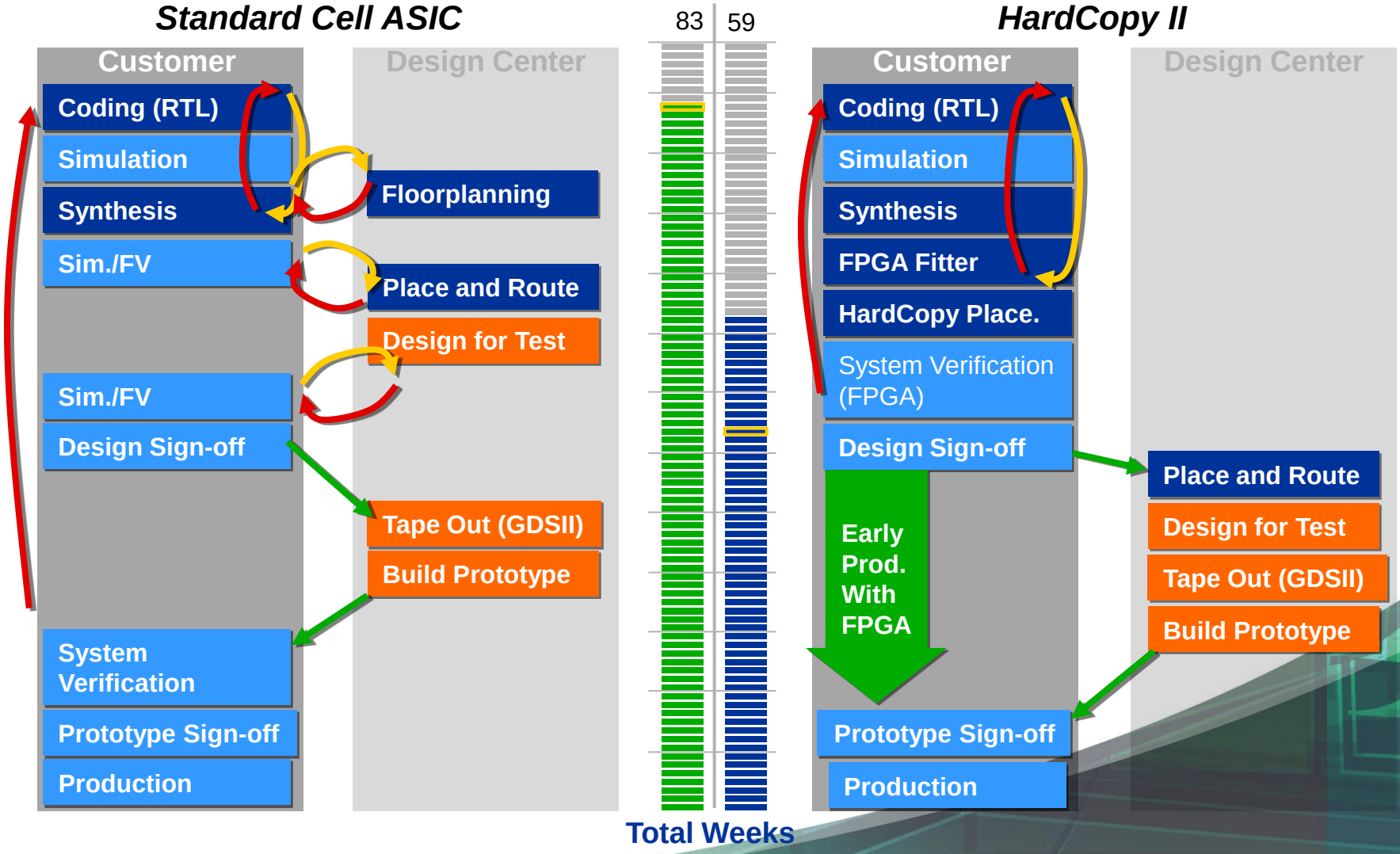
Design Methodology Comparison



- HardCopy design flow provides the most comprehensive verification process and the fastest time to market.

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ASIC vs. HardCopy Comparison

- Based on one respin
  - 83 weeks to reach ASIC production
  - 59 weeks to reach HardCopy production
  - 44 weeks for early production with FPGA
- Significant time-to-market advantage
- Altera supports traditional ASIC and FPGA design tools
- Most comprehensive pre-tape-out system verification methodology
- Highest first-time success rate in the industry

The Wave of the Future

Stratix II

FPGA Prototype

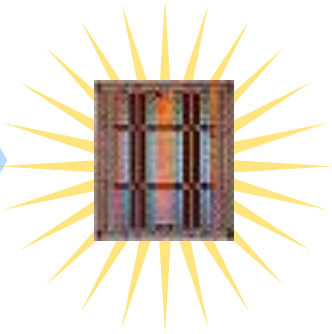
Get Low Development Costs and Maximum Flexibility With FPGAs

QUARTUS II

Design Tool

HardCopy II

Structured ASIC



Convert to HardCopy Structured ASICs When Justified and Needed

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Designed for Seamless Migration

Comparison of Stratix II FPGA and HardCopy II Structured ASIC

Process technology	Same
Soft intellectual property (IP)	Proven & embedded in design database
Hard IP functionality	Identical
User I/O characteristics	Equivalent
Design methodology	Unified for prototype FPGA & HardCopy II device
Pin-to-pin compatibility	Yes[1]
Package	Equivalent
Design revalidation	Not required

Quartus II Software Guides Designs for Seamless Migration

[1] **HardCopy II devices have fewer available I/O pins.**

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HardCopy II Family

Feature	HC210W	HC210	HC220W	HC220	HC230	HC240
ASIC Gates	1M	1M	1.6M	1.6M	2.2M	2.2M
Additional Gates for DSP Blocks	0	0	0.3M	0.3M	0.7M	1.4M
Total RAM (Millions of Bits)	0.88	0.88	3	3	6.3	8.8
Phase-Locked Loops (PLLs)	4	4	4	4	8	12
Maximum User I/O	308	334	494	494	698	951
Package	F484 Wire Bond	F484	F672 F780	F672 F780	F1020	F1020 F1508
FPGA Prototype Options	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90 EP2S130	EP2S60 EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180

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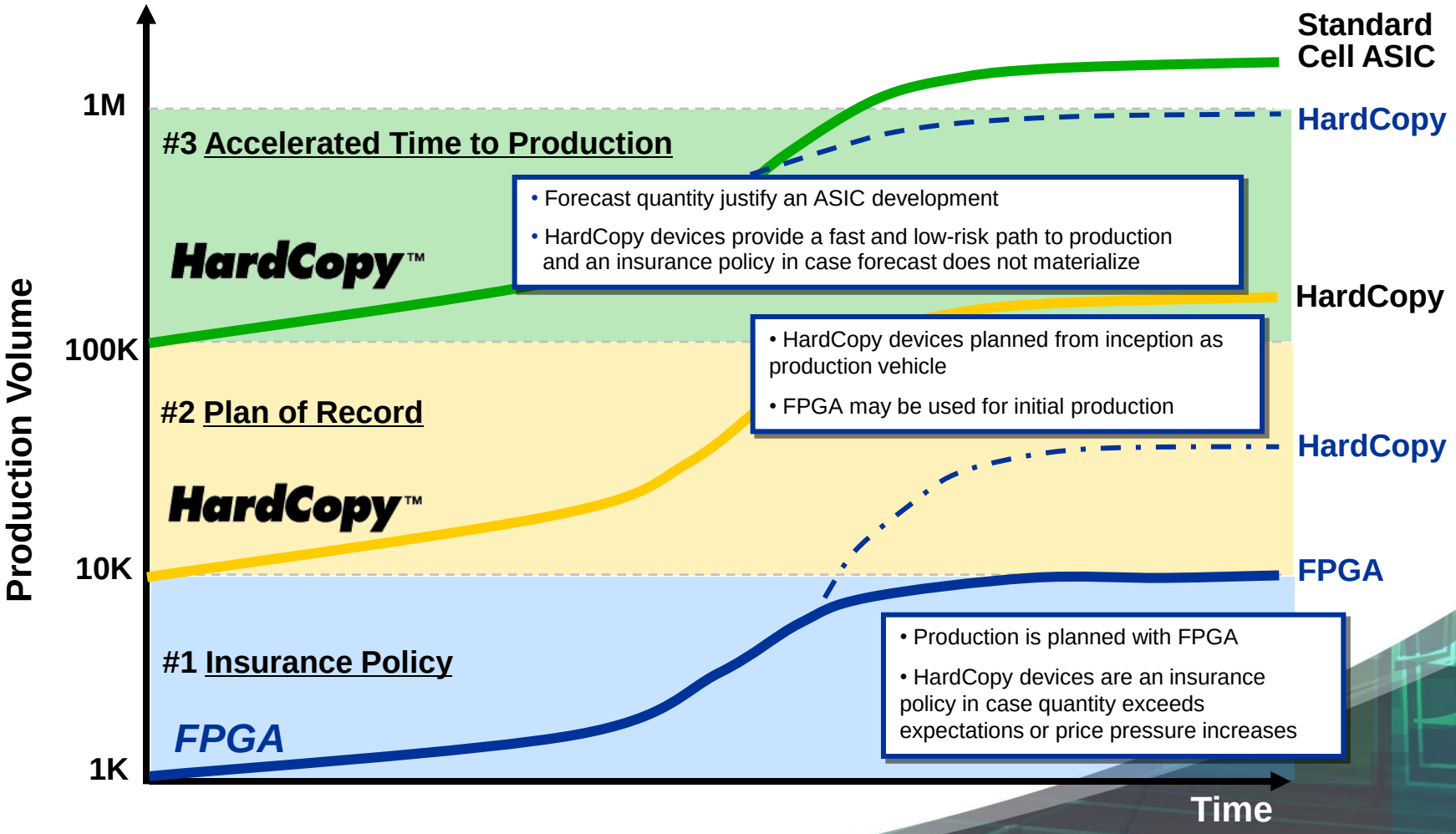
HardCopy Usage Models



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Summary

- HardCopy II structured ASICs are low-cost, drop-in replacements for Altera high-performance Stratix II FPGAs
- HardCopy II structured ASIC power and performance are comparable to standard-cell ASICs
- Quartus II software enables seamless migration from Stratix II FPGAs to HardCopy II structured ASICs
- HardCopy II structured ASICs are true alternatives to the standard-cell ASICs

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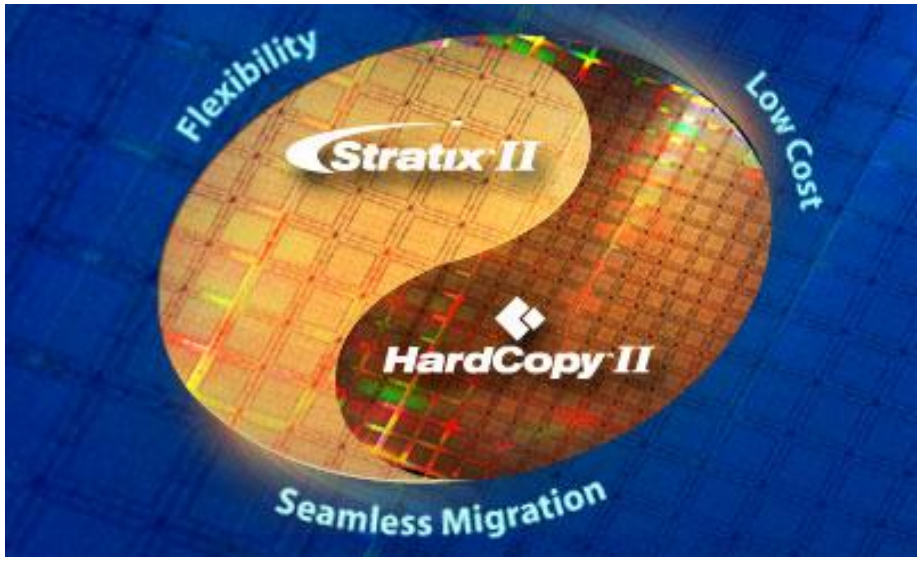
Altera Offers

The Only FPGA Company With a Structured ASIC Solution



The Only Structured ASIC Company With a Programmable Logic Front-End

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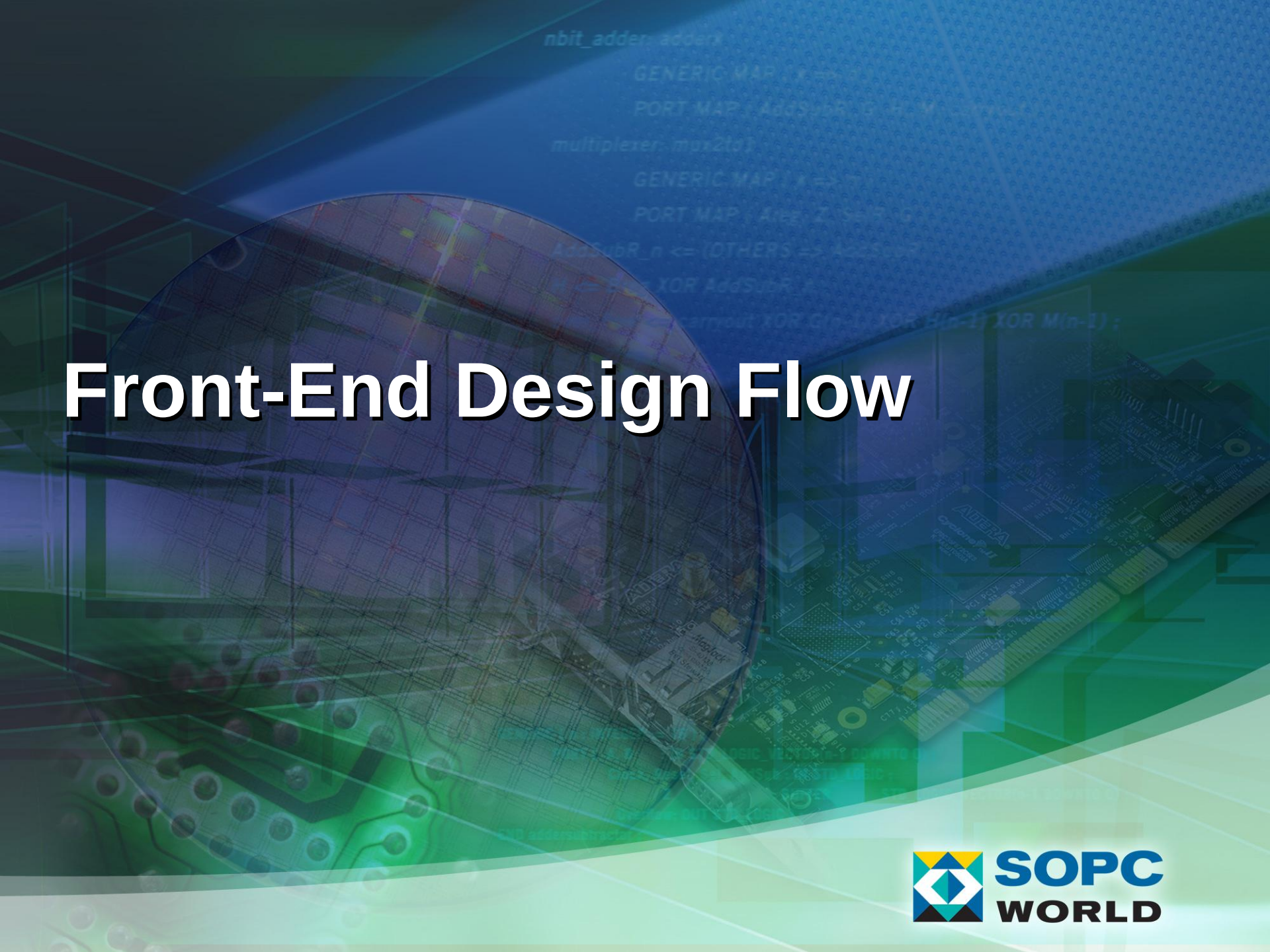
Technical Backup

Front-End Design Flow



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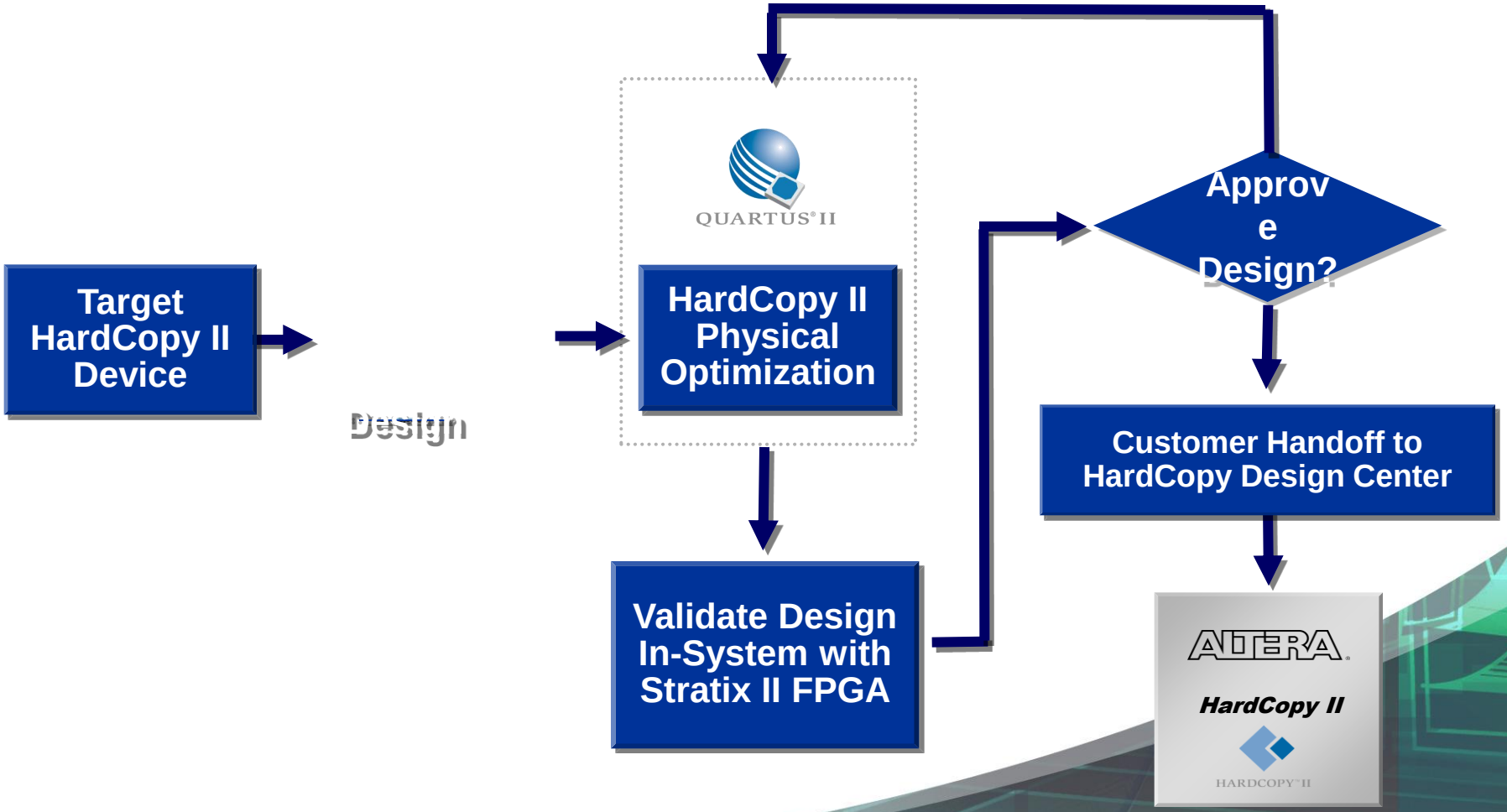
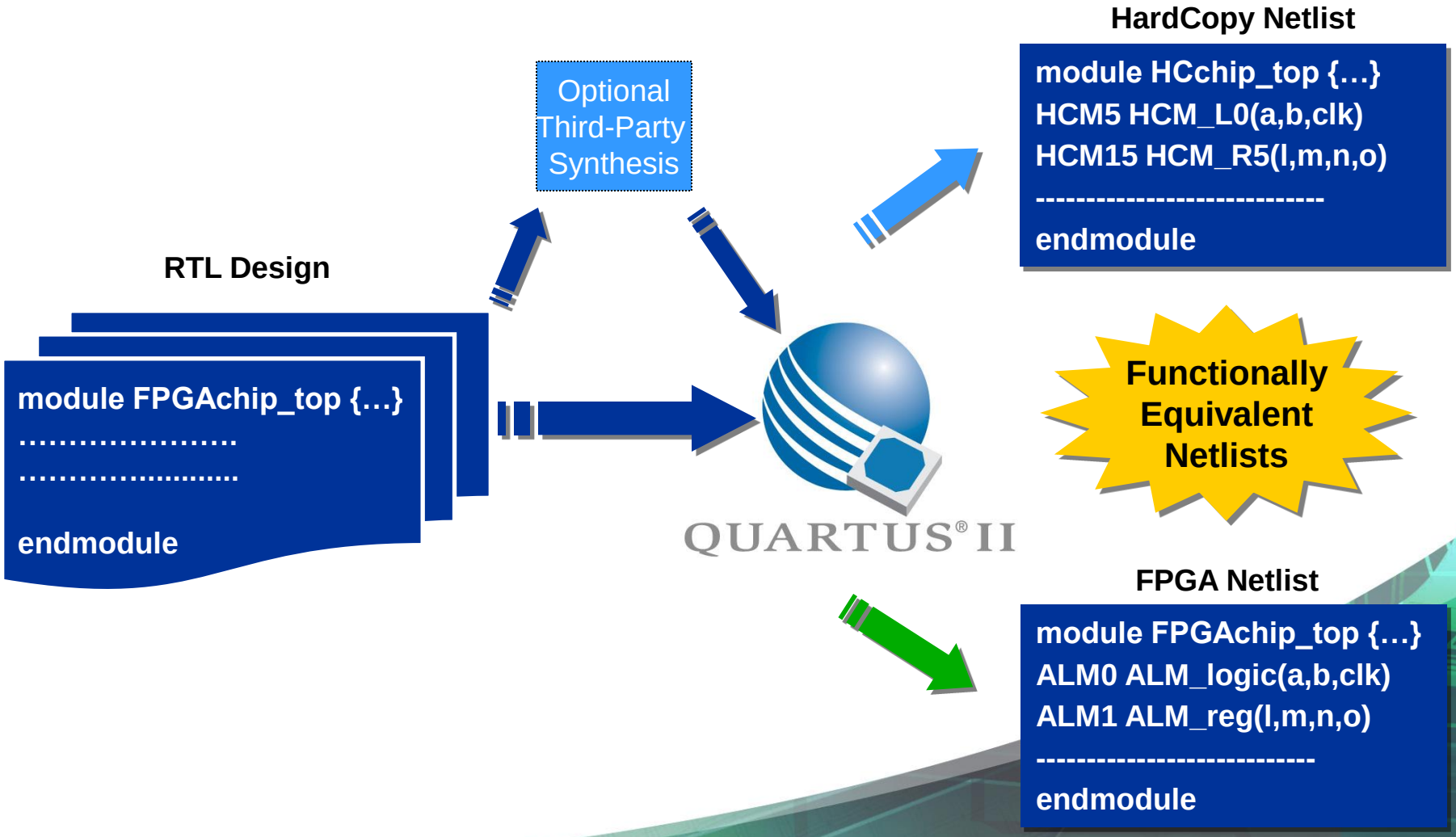
HardCopy II Design Flow



Front-End Design Flow in Quartus II Software



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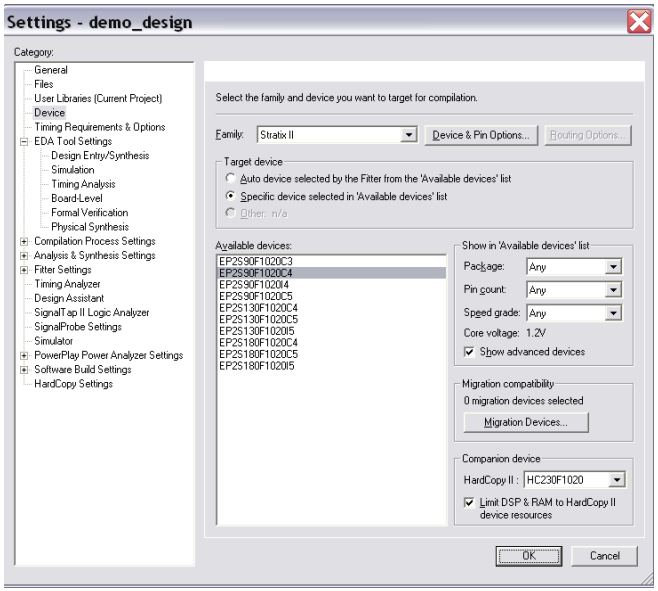
Select Companion Pair

- Chooses Stratix II FPGA and HardCopy II device
- Reports Stratix II FPGA vertical migration devices
- Guides pin-out compatibility between Stratix II and HardCopy II devices
- Constrains I/O standards, PLLs, and delay-locked loops (DLLs)
- Filters FPGA prototyping options

Device Settings Box



Recompile the design after choosing the HardCopy II device

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HardCopy II Advisor

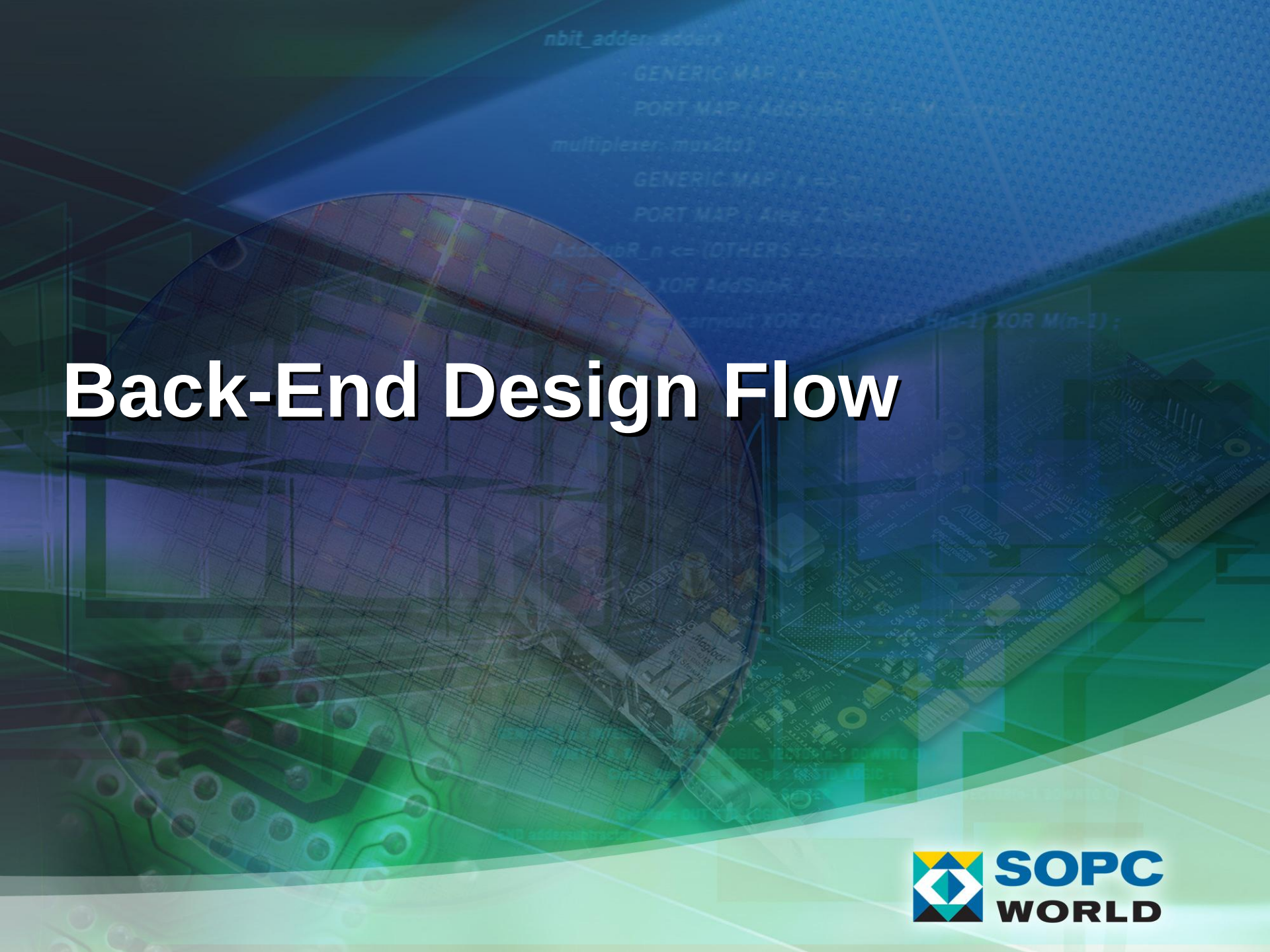
- Step-by-step guides to prepare design for a successful netlist handoff to HardCopy Design Center
- Use the advisor to review design settings in Quartus II software
- Reviews
  - Timing constraints
  - Project settings
  - HardCopy II development tasks
- Alerts any unresolved tasks

SOPC WORLD

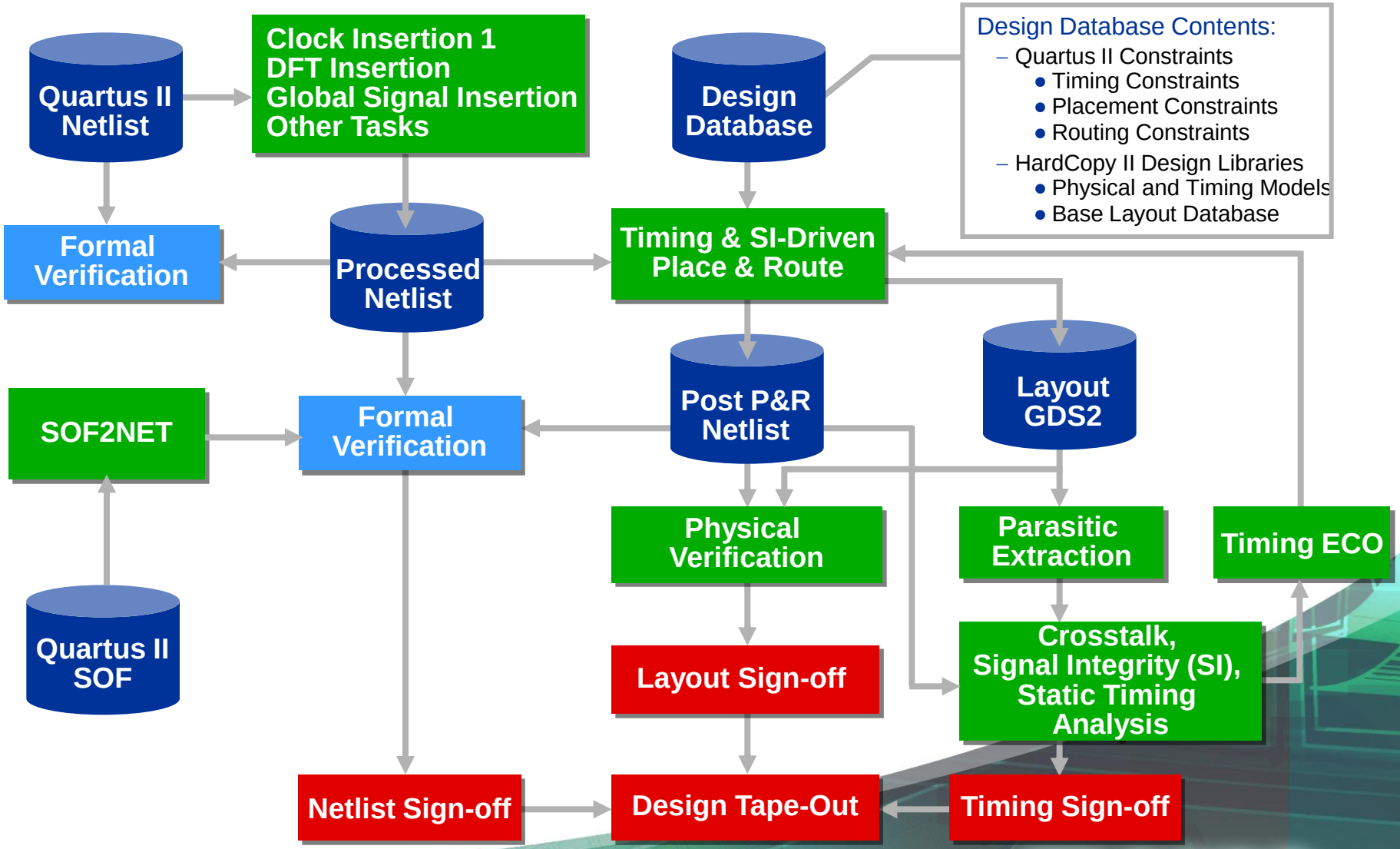
HardCopy II Advisor Checks

- ✓Chosen Stratix II/ HardCopy II devices
- ✓ Design Assistant enabled
- ✓ Assembler enabled
- ✓ Timing settings enabled
- ✓ Incompatible assignments
- ✓ Current revision compiled
- ✓ Companion revision created
- ✓ Companion revision compiled
- ✓ Comparison of revisions completed
- ✓ Handoff report created
- ✓ Archive created

Back-End Design Flow



HardCopy II Back-End Design Flow

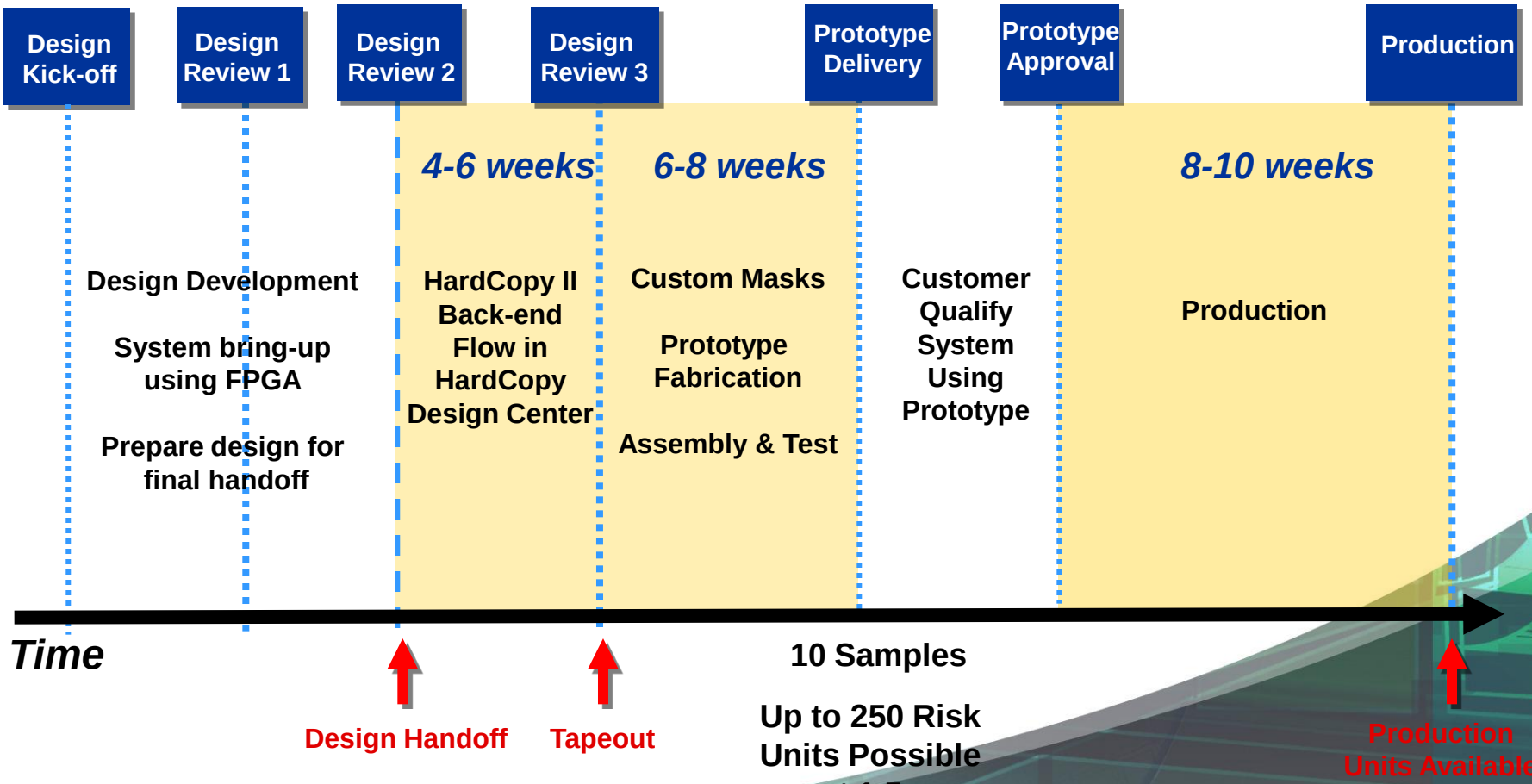


SOPC WORLD

Altera Responsible for Testing

Scan Chain Insertion	■ Route optimization ■ Manage scan flop timing overhead in Quartus II software
ATPG	97-98% stuck at fault coverage
Memory Built-in Self Test (BIST)	Includes fuse-based repair
PLL/DLL and SERDES BIST	Lock at speed
JTAG	■ I/O Connections ■ Parametric measurements
Speed Paths	Speed path and scribe line structure (ET) for determination of process factor

Chronology of HardCopy II Design Activities



Activities in color indicate Altera controls schedule

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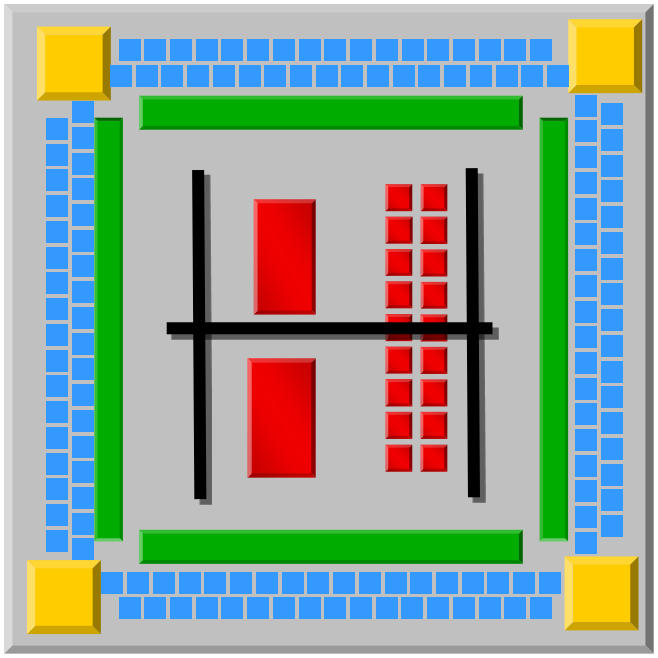
The HardCopy II Family

- Structured ASIC technology
  - Uses same base array across multiple designs for a given density with five customizable masks
- Offers true alternative to standard cell ASIC
  - Up to 2X performance improvement over FPGA
  - 50%+ power reduction vs. FPGA prototype
  - $10 volume price for 1M-gate device (HC21W)
- Eliminates high risk and cost of standard cell ASIC
  - Unified FPGA-like front-end design flow in Quartus II software
  - Full in-system design verification using Stratix II FPGA
  - Seamless migration to HardCopy II structured ASIC
    - Altera performs turn-key, back-end design flow
  - Drop-in replacement between Stratix II FPGAs and HardCopy II structured ASICs

Foundation for Low Cost and Seamless Migration

- First: defined base family members
  - I/O count
  - Packages
- Embedded equivalent Stratix II FPGA structures
  - I/O buffers
  - Clock network
  - PLL
  - Memory blocks
- Remaining area filled with logic



Result: Low-Cost Structured ASIC With Stratix II FPGA Prototype

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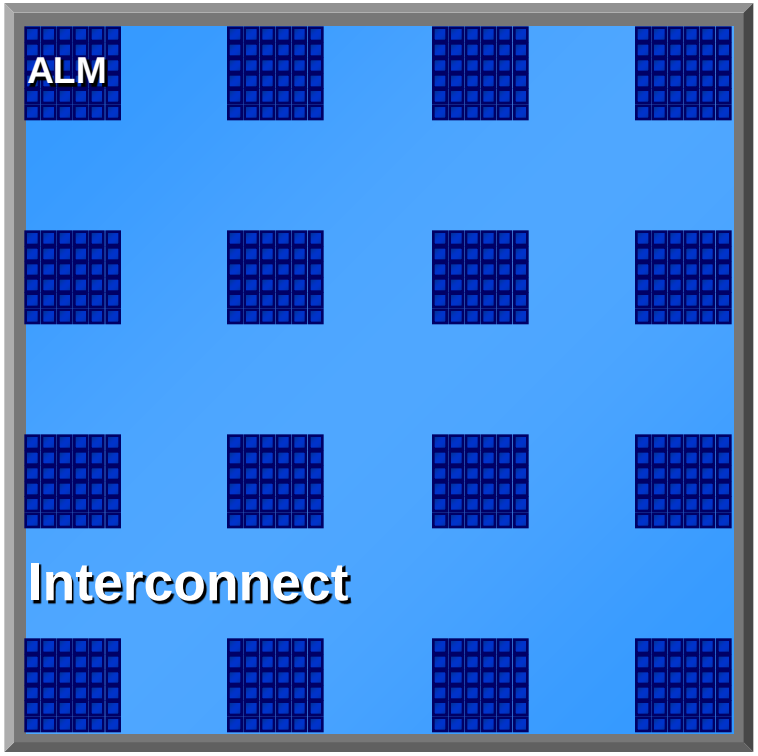
Innovative Logic Architecture

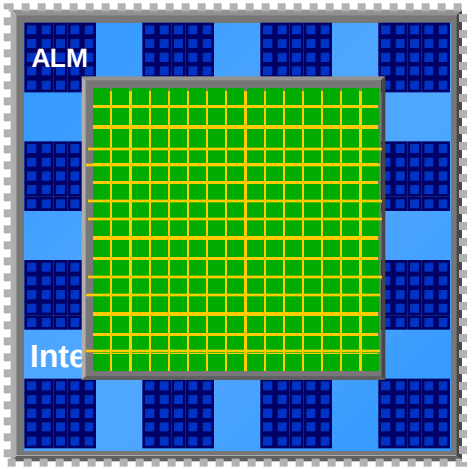
Stratix® II



Adaptive Logic Module (ALM)-Based

HardCopy™ II

~~50%~~ 80% Reduction



Same Architecture With Programmability Removed

Array of Fine-Grained HCells

Delivers High Density and Low Cost per Gate

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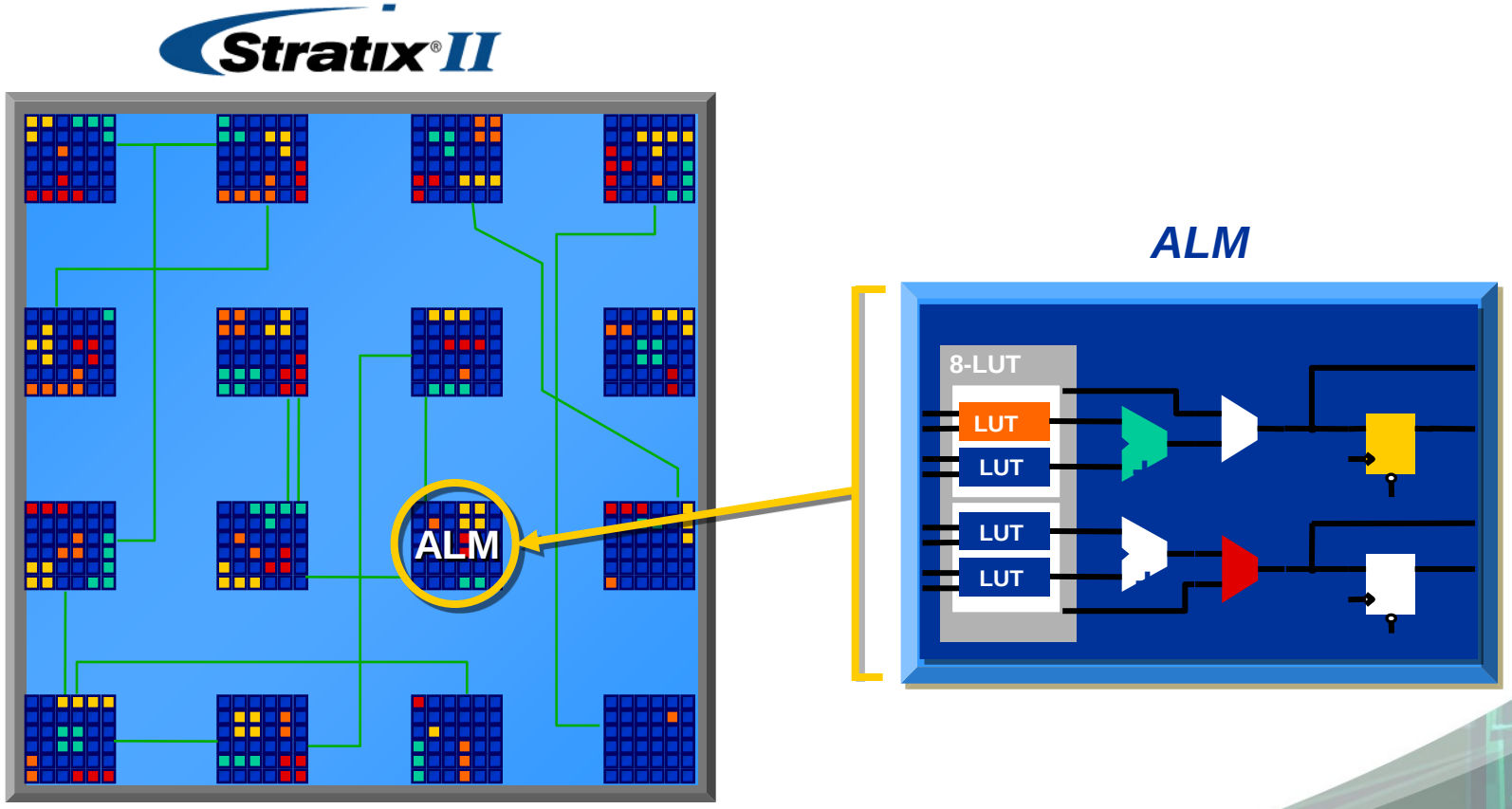
Achieving Seamless Migration



Many Different ALM Configurations

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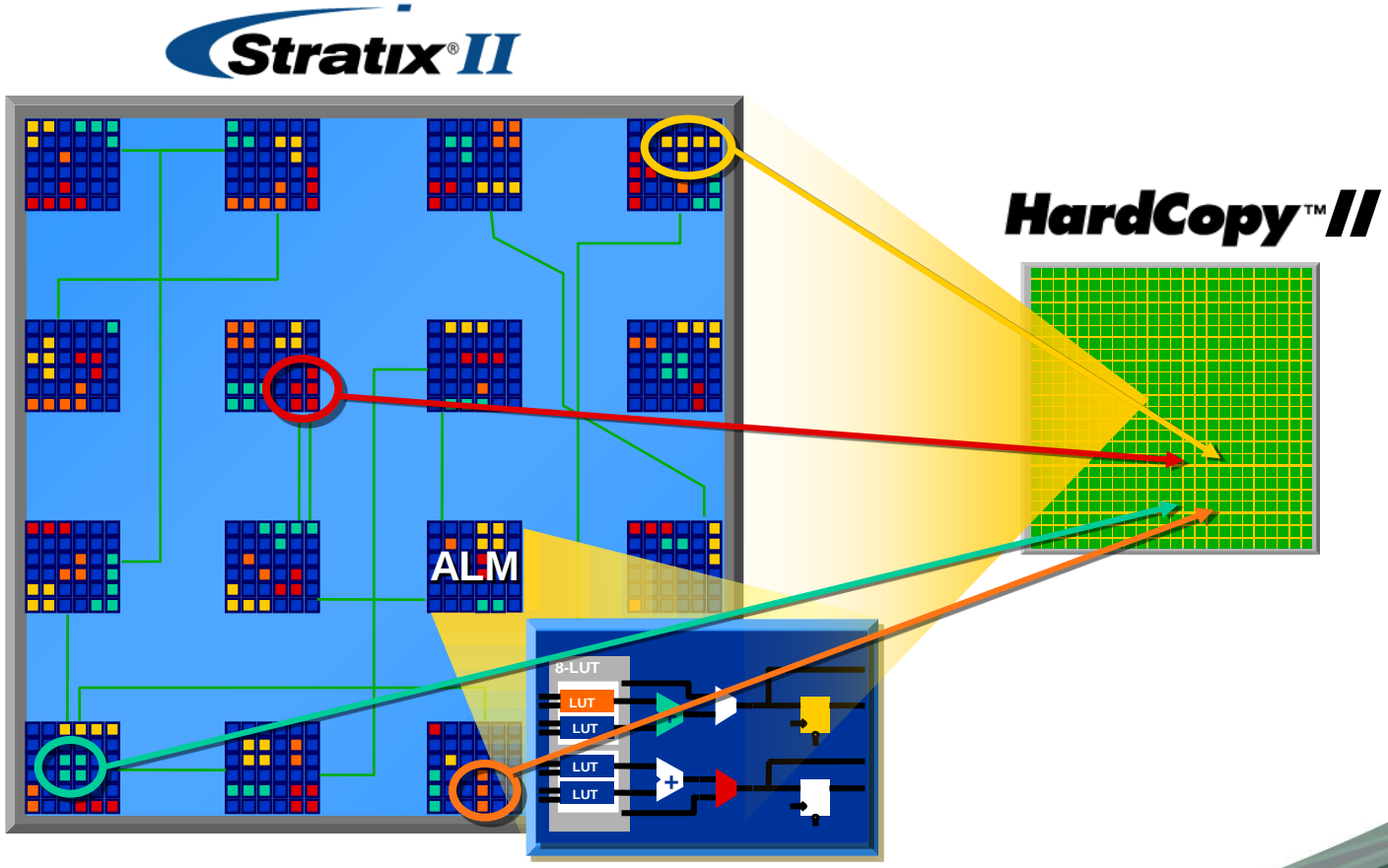
Implementing Seamless Migration

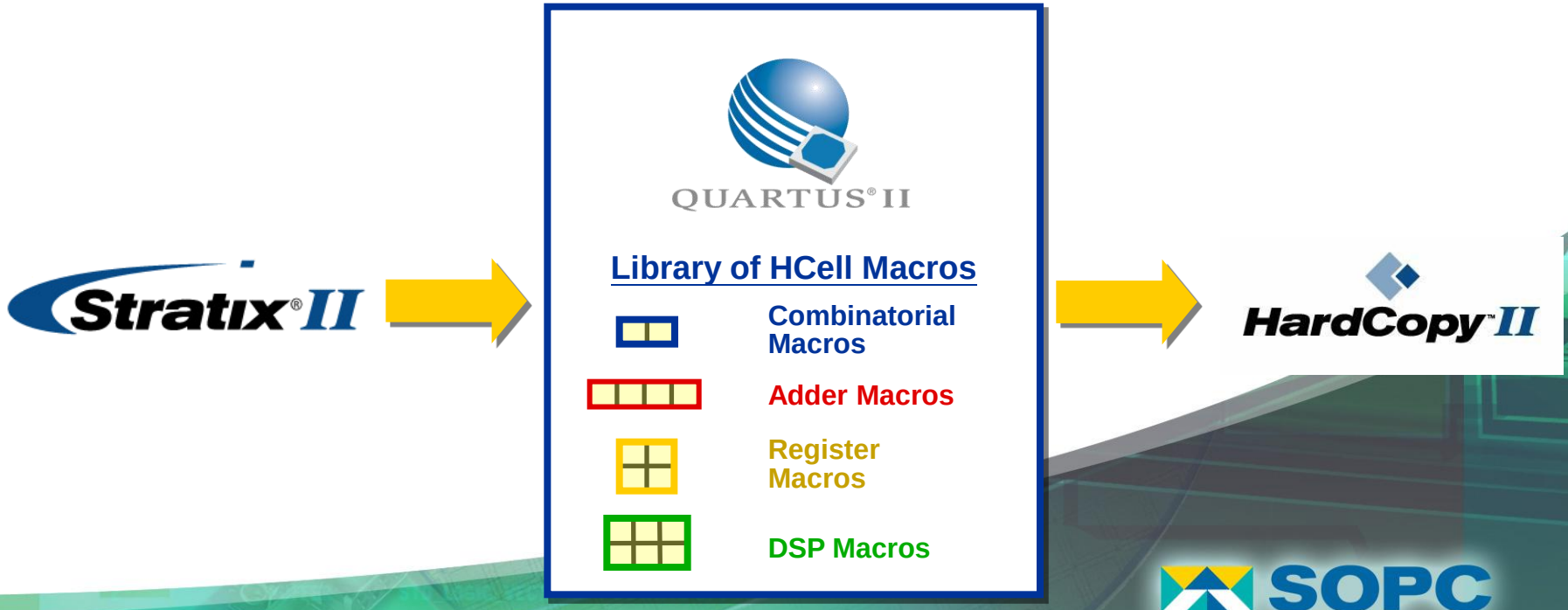


- HCell macro: collection of HCells implementing unique ALM configuration
- > 20K predefined, preverified, precharacterized macros

SOPC WORLD

Quartus II Software Performs the Mapping

- Utilizes HCell macro library
  - Predefined, precharacterized, preverified
  - Maps ALM-by-ALM
  - Maps only logic used within each ALM
- HardCopy II Advisor makes the process easy

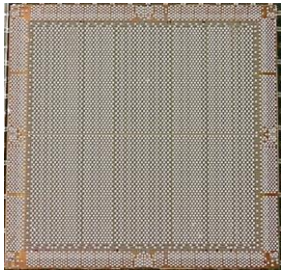


Guaranteed First-Silicon Success

The World's Biggest and Fastest FPGAs

The World's Only Seamless Migration From FPGA

Stratix™ II



EP2S130

5:1 Die Size Reduction

HardCopy™ II

HC230

- Low unit cost
- 70% lower core power
- Up to 2X the FPGA performance

EP2S90

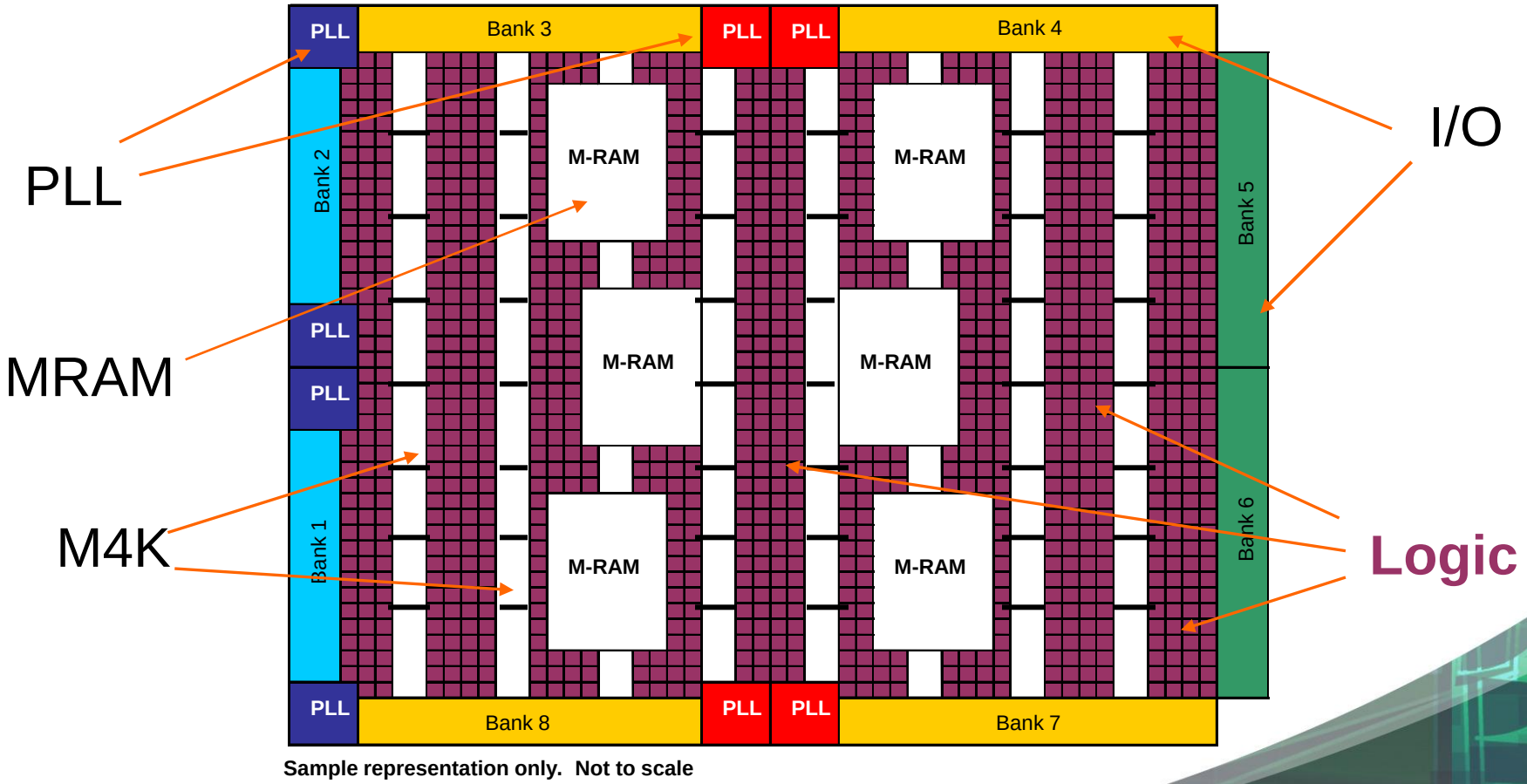
11:1 Die Size Reduction

HC210

HardCopy II Structured ASICs Linking the FPGA and ASIC Worlds

SOPC WORLD

HardCopy II Device Architecture



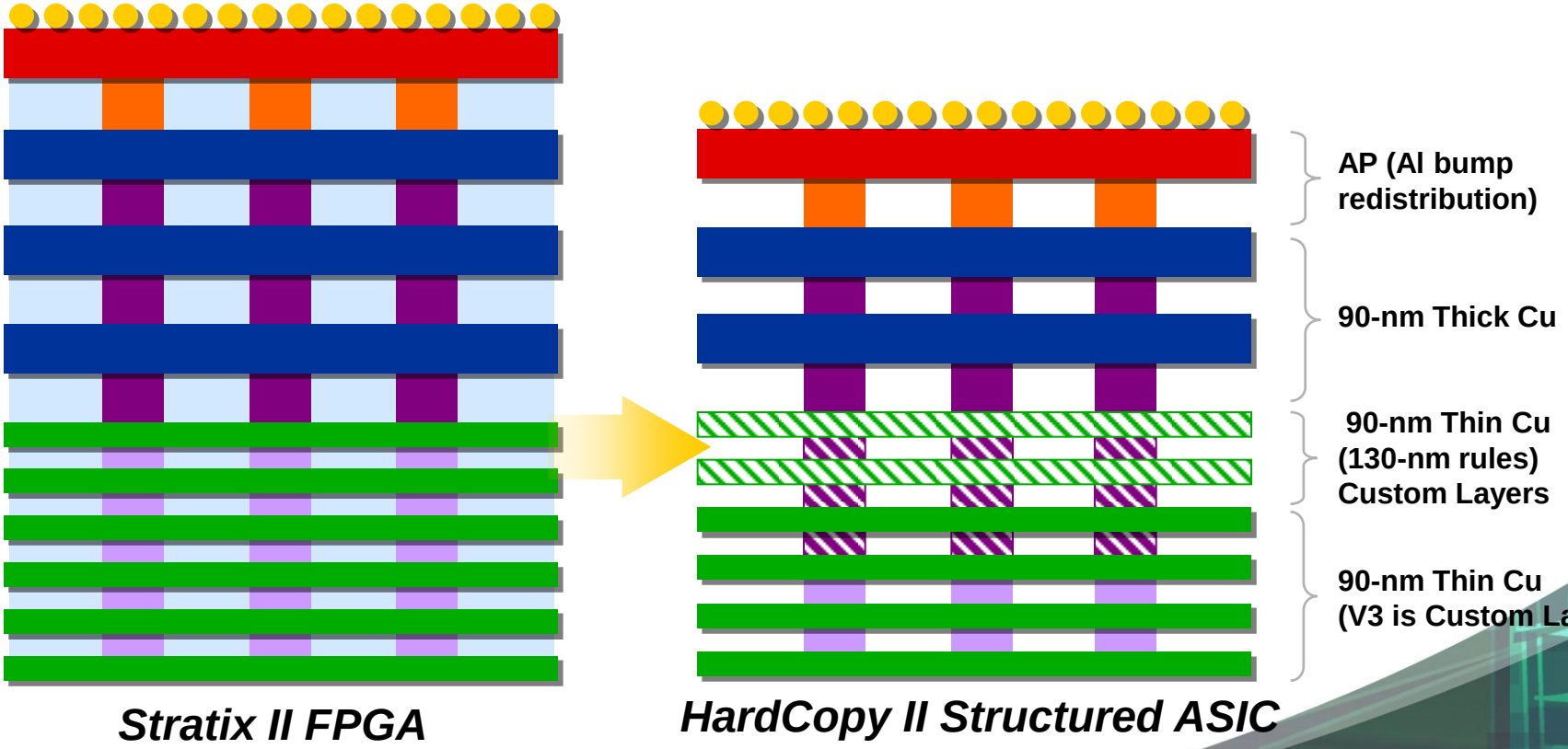
Sample representation only. Not to scale

Designed for Low Cost, High Performance, and Low Power

SOPC WORLD

Understanding HardCopy II Metal Layers

Customer Layers: V3 + V4/M5/V5/M6

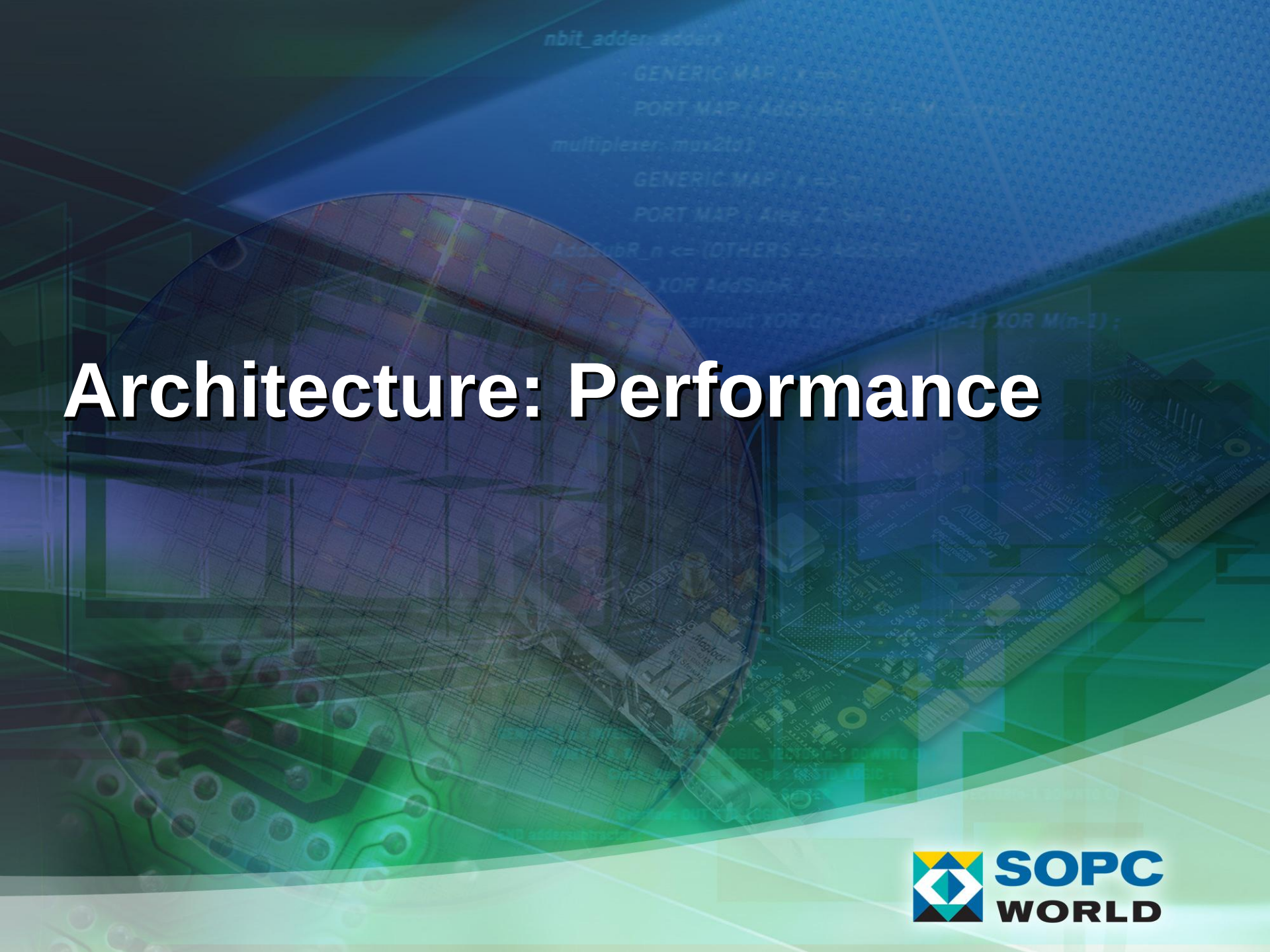


Stratix II FPGA

HardCopy II Structured ASIC

SOPC WORLD

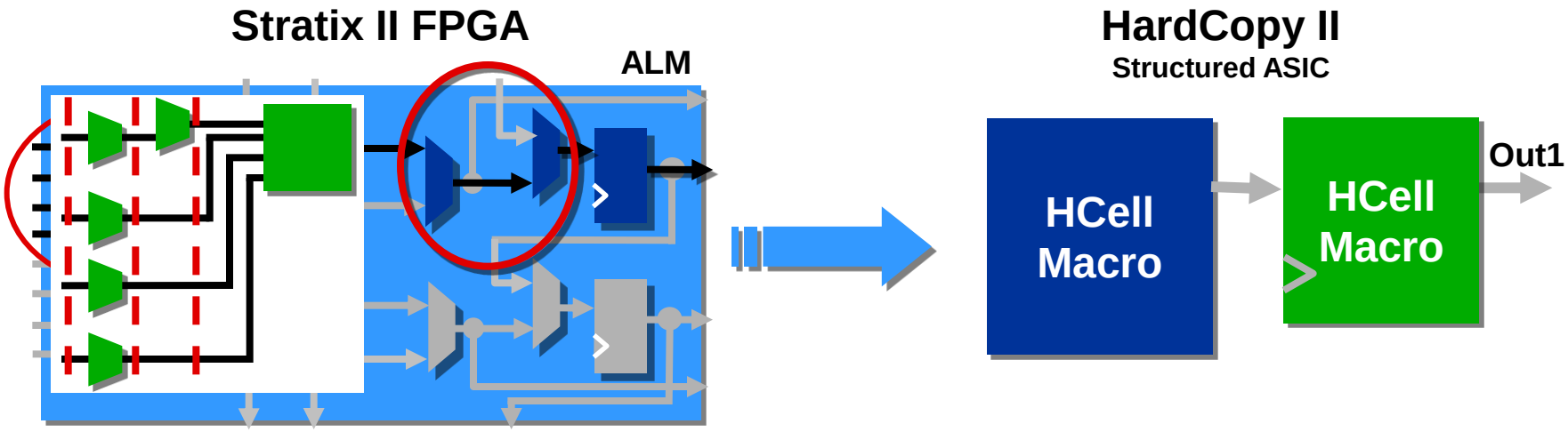
Architecture: Performance



HardCopy II Performance

- Actual design performance in HardCopy II devices can be significantly better than in Stratix II FPGAs
  - Faster routing
  - Fewer logic levels
  - Flexibility in HCell macro placement
- Design performance depends on critical path
  - Core (other than DSP and memory)
    - Up to 100% faster than Stratix II FPGAs
  - IO path, DSP, and memory
    - Minimal performance improvement over Stratix II

HCell Macros: Designed for High Performance



- Fewer levels of logic for the same combinatorial function
  - Test example: 6-input LUT translates to 6-logic levels in FPGA
  - HardCopy II implementation: 2 to 5 logic levels, design dependent
- Programmable interconnect multiplexers removed
- Much shorter routing delay between HCells

More Gates per mm², Fewer Logic Levels

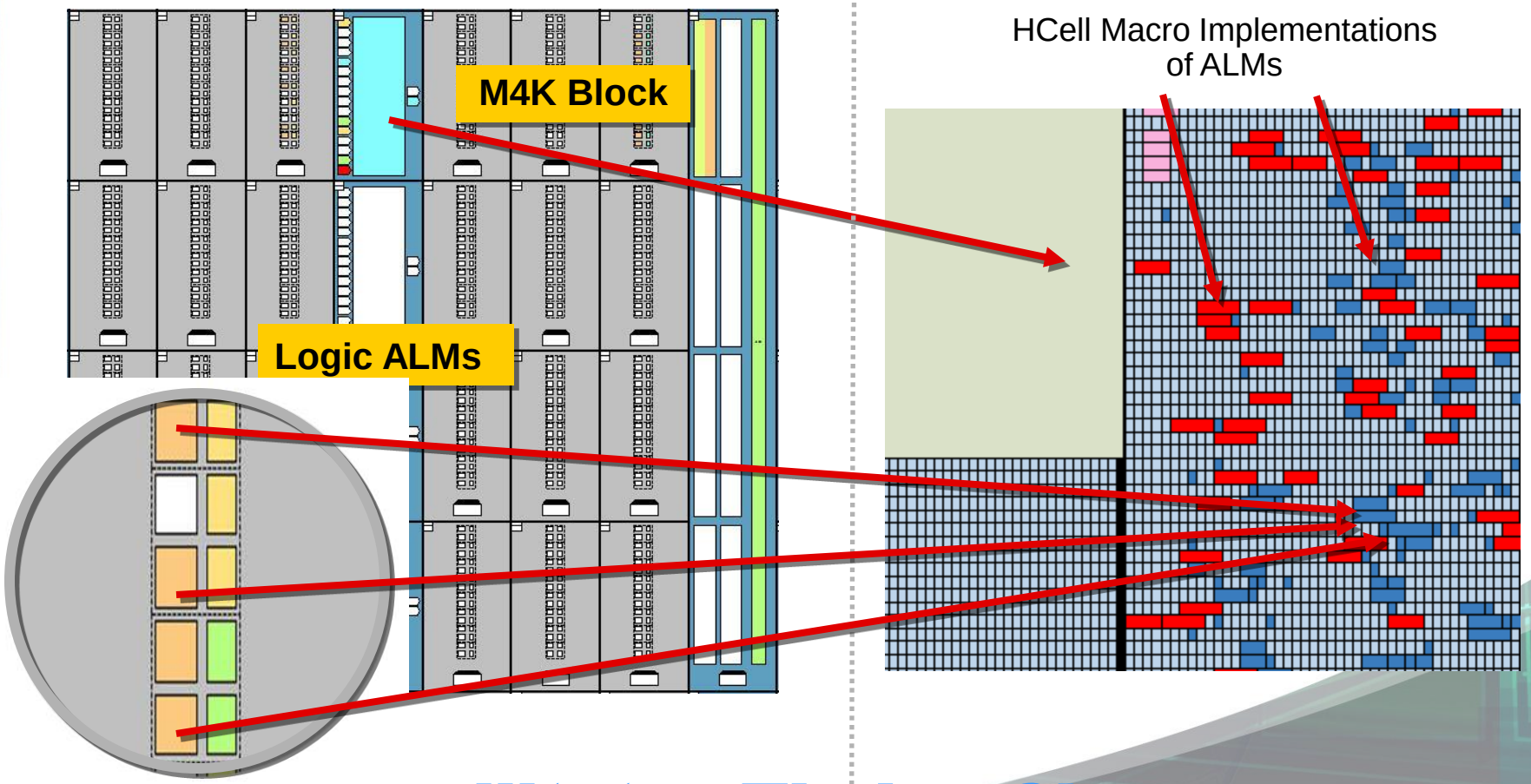
SOPC WORLD

Logic Placement Flexibility

Section of Stratix II Device Floorplan

Section of HardCopy II Floorplan

HCell Macro Implementations of ALMs

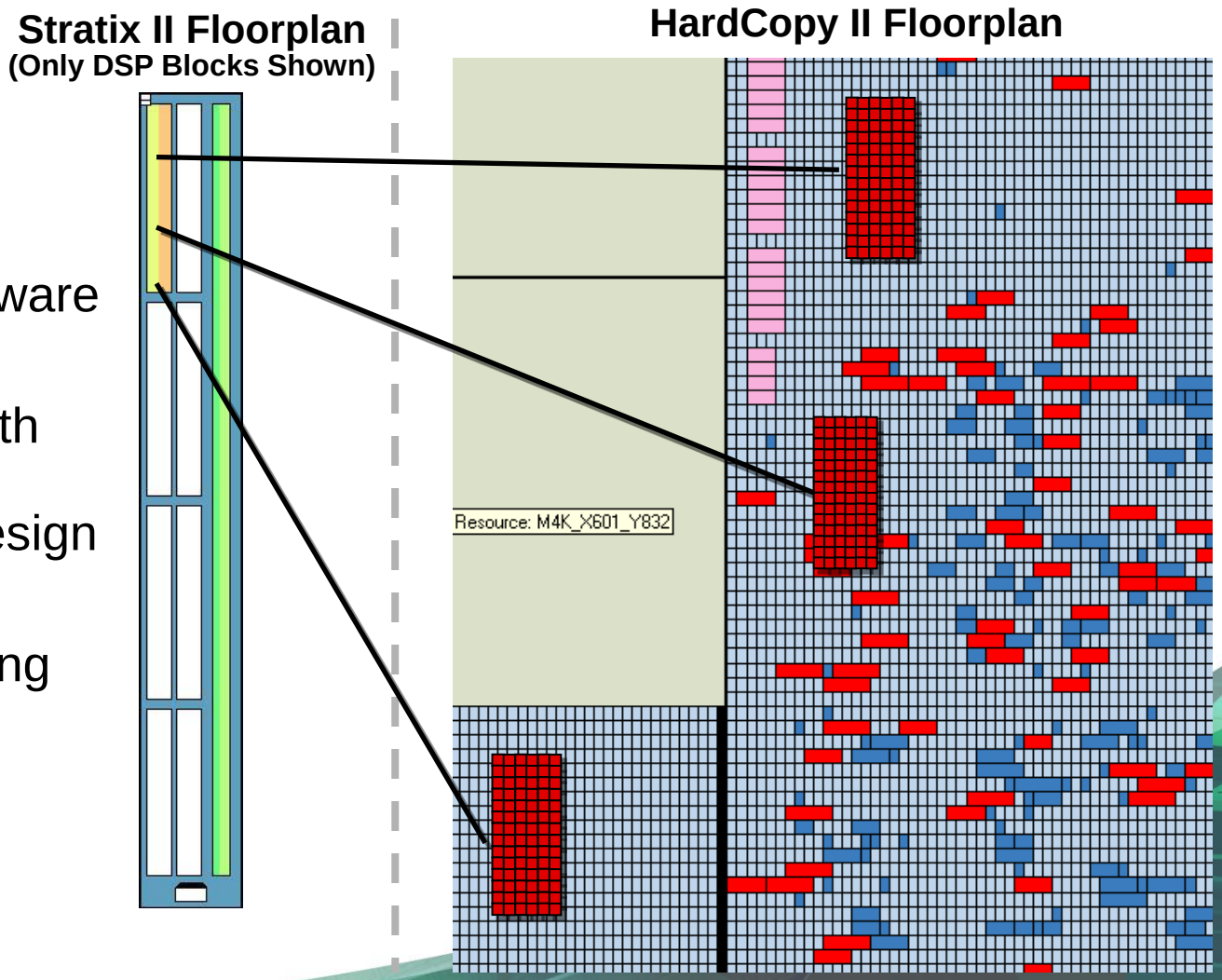


Facilitates Timing Closure

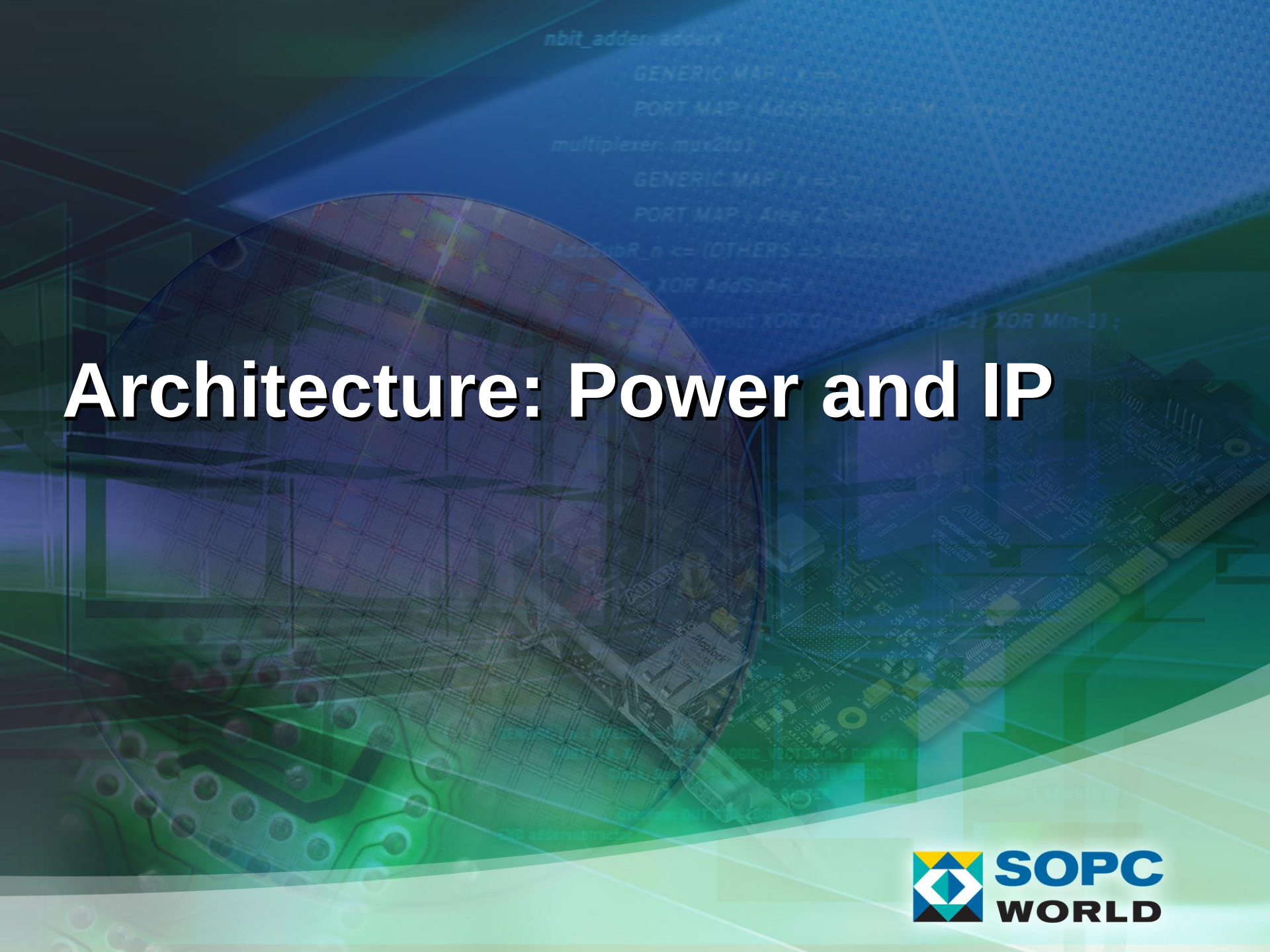
SOPC WORLD

DSP Function Placement Flexibility

- Timing-driven compilation in Quartus II software
- User-driven with LogicLock™ incremental design
- Facilitates timing closure



Architecture: Power and IP



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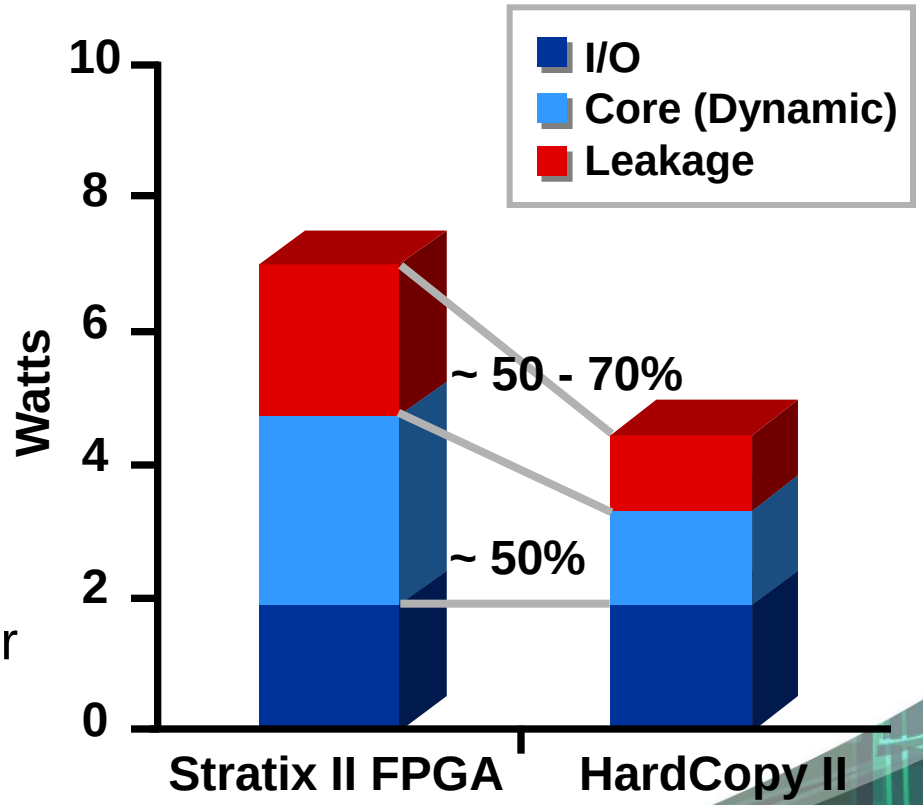
Optimized for Power Efficiency

- Unused logic, memory blocks not connected to power rail
- Unused clock trees, PLLs not powered
- Quartus II PowerPlay power analyzer tool
  - Calculates dynamic power
  - Based on simulation file



Test Case Details:
FPGA: EP2S60, 85º C, 90% utilized, 200 MHz
HardCopy II: HC210 / HC220

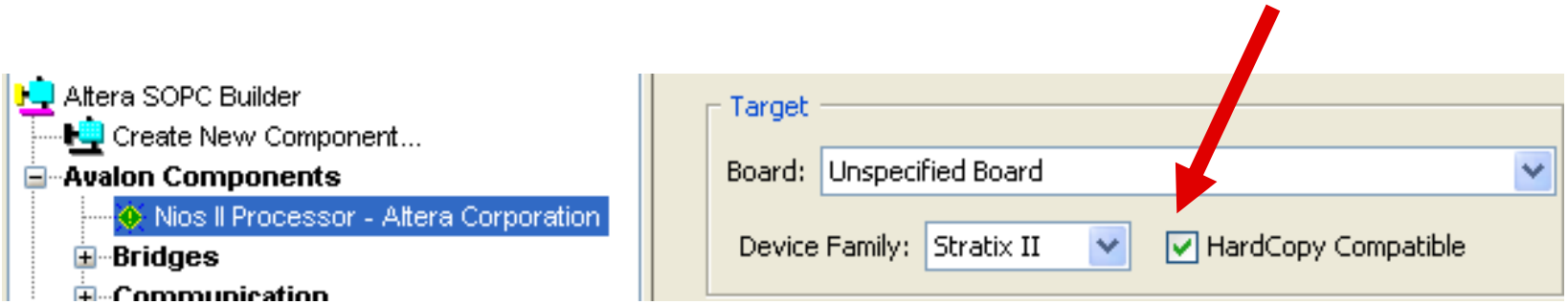
SOPC WORLD

IP Support

- IP cores for the Stratix II FPGAs map into HardCopy II structured ASICs
  - Except IP with dependency on pre-initialized RAMs
  - HardCopy II family does support ROMs
- Altera Megafunction Partners Program (AMPP^{SM}) IP
  - IP suppliers may require additional license fee

Nios II Support for HardCopy II Devices

- Set appropriate initialization settings for RAM
  - Turn on *HardCopy Compatible* check box in SOPC Builder on the system contents page



Choose the Right HardCopy II Device

- Use HardCopy II Device Resource Guide in Quartus II software
- Device Resource Guide reports
  - Compiled Stratix II device resources
  - Design's required resources
  - Resource utilization in HardCopy II devices
- Device Resource Guide helps select correct HardCopy II device
  - Vertical package migration support
  - Report Stratix II and HardCopy II devices

Device Resource Guide

Stratix II EP2S90 FPGA **HardCopy II HC230 Structured ASIC**

HardCopy II Device Resource Guide

Color Legend:
-- Green:
-- Package Resource: The HardCopy II package can be migrated from the Stratix II FPGA selected package, and the design has been fitted with the target device migration enabled.

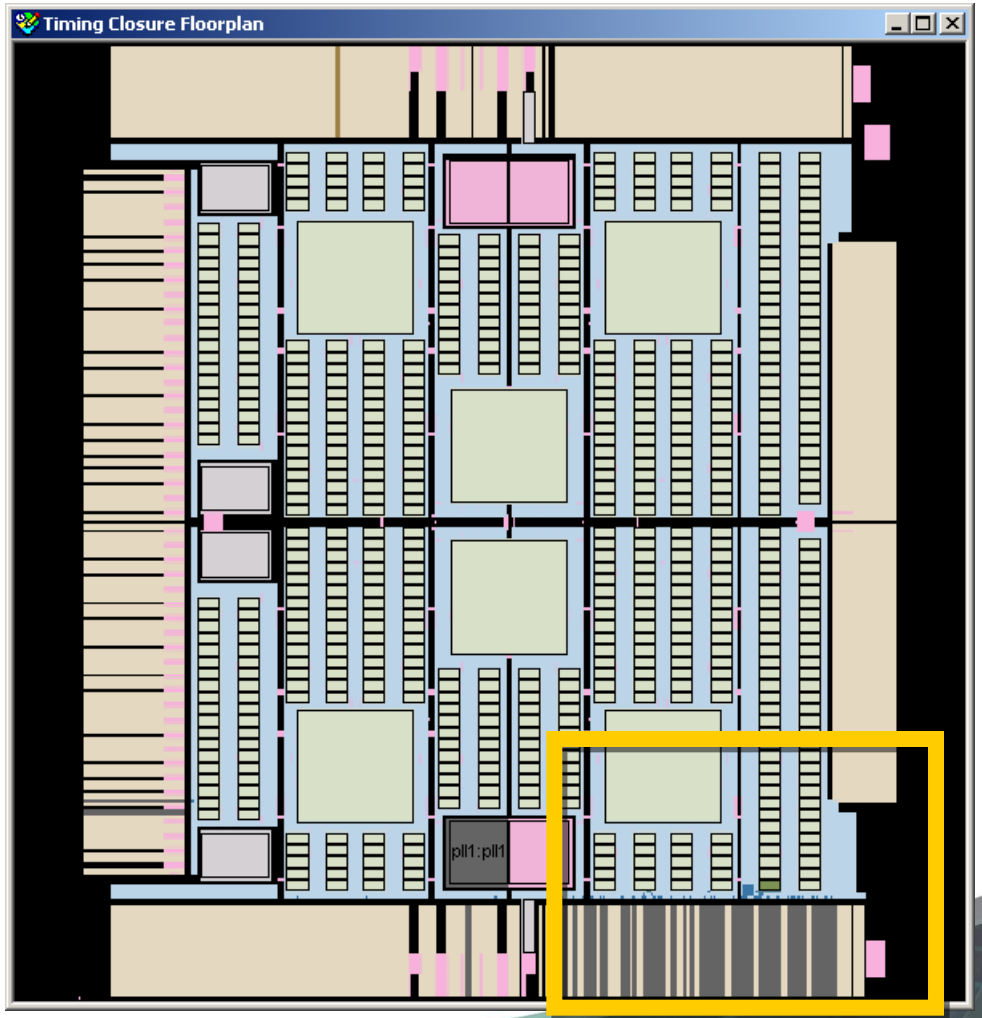
	Resource	Stratix II EP2S90	HC210W	HC210	HC220	HC220	HC230	HC240	HC240
1	Migration Compatibility		None	None	None	None	High	None	None
2	Primary Migration Constraint		Package	Package	Package	Package		Package	Package
3	Package	FBGA - 1020	FBGA - 484	FBGA - 484	FBGA - 672	FBGA - 780	FBGA - 1020	FBGA - 1020	FBGA - 1508
4	⊟ Logic	--	1%	1%	1%	1%	1%	1%	1%
5	-- Logic cells	92 ALUTs	--	--	--	--	--	--	--
6	-- DSP elements	1	--	--	--	--	--	--	--
7	⊟ Pins								
8	-- Total	51	51 / 309	51 / 335	51 / 493	51 / 495	51 / 699	51 / 743	51 / 952
9	-- Differential Input	2	2 / 66	2 / 70	2 / 90	2 / 90	2 / 128	2 / 224	2 / 272
10	-- Differential Output	0	0 / 44	0 / 50	0 / 70	0 / 70	0 / 112	0 / 200	0 / 256
11	-- PCI / PCI-X	0	0 / 159	0 / 166	0 / 244	0 / 246	0 / 358	0 / 366	0 / 471
12	-- DQ	0	0 / 20	0 / 20	0 / 50	0 / 50	0 / 204	0 / 204	0 / 204
13	-- DQS	0	0 / 8	0 / 8	0 / 18	0 / 18	0 / 72	0 / 72	0 / 72
14	⊟ Memory								
15	-- M-RAM	0	0 / 0	0 / 0	0 / 2	0 / 2	0 / 6	0 / 9	0 / 9
16	-- M4K blocks & M512 blocks	1	1 / 190	1 / 190	1 / 408	1 / 408	1 / 614	1 / 816	1 / 816
17	⊟ PLLs								
18	-- Enhanced	1	1 / 2	1 / 2	1 / 2	1 / 2	1 / 4	1 / 4	1 / 4
19	-- Fast	0	0 / 2	0 / 2	0 / 2	0 / 2	0 / 4	0 / 8	0 / 8
20	DLLs	0	0 / 1	0 / 1	0 / 1	0 / 1	0 / 2	0 / 2	0 / 2
21	⊟ SERDES								
22	-- RX	0	0 / 17	0 / 21	0 / 31	0 / 31	0 / 46	0 / 92	0 / 116
23	-- TX	0	0 / 18	0 / 19	0 / 29	0 / 29	0 / 44	0 / 88	0 / 116
24	⊟ Configuration								
25	-- CRC	0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
26	-- ASMI	0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
27	-- Remote Update	0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
28	-- JTAG	0	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1

SOPC WORLD

HardCopy II Floorplan

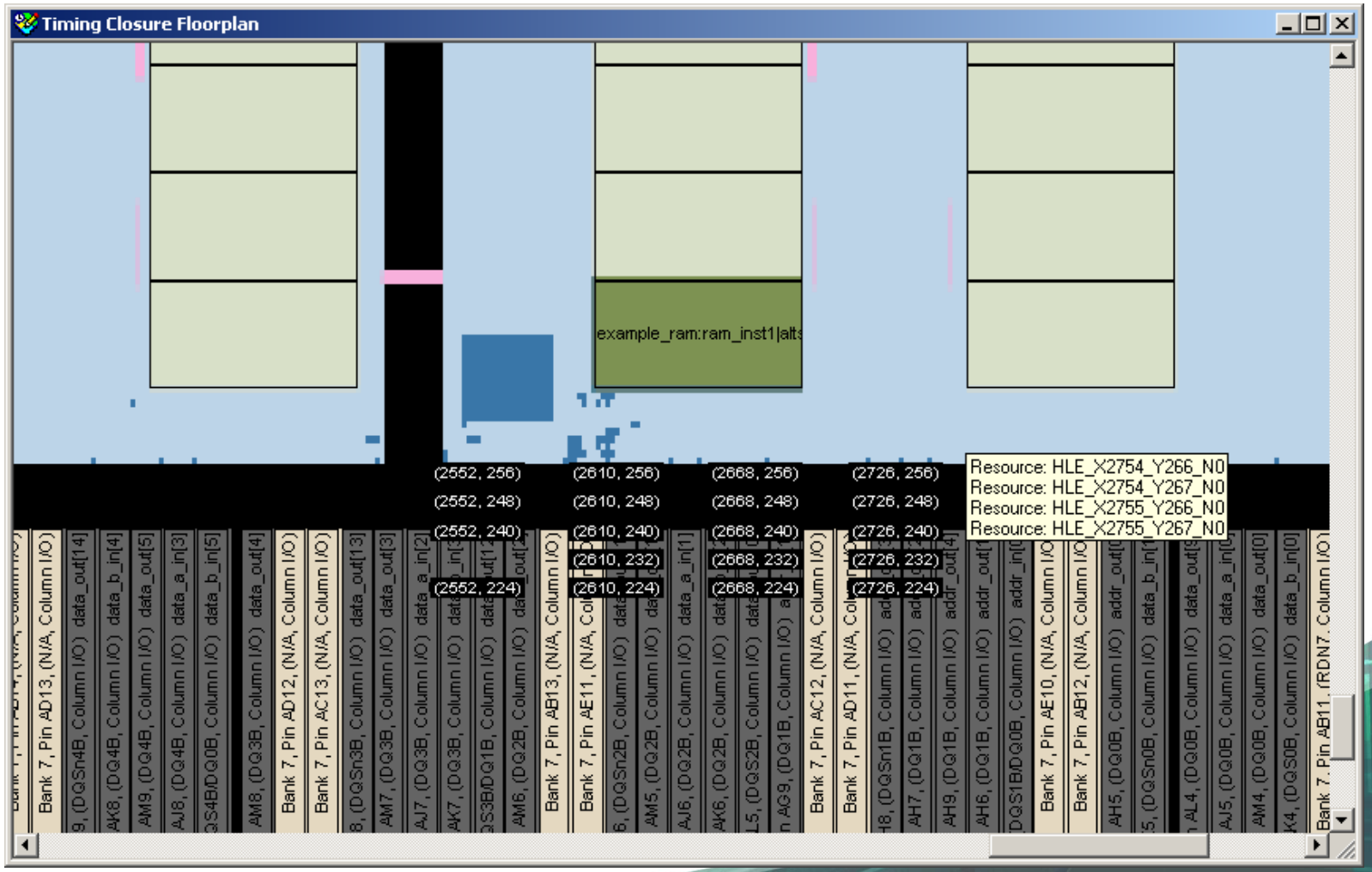
SOPC WORLD

HardCopy II Floorplan View



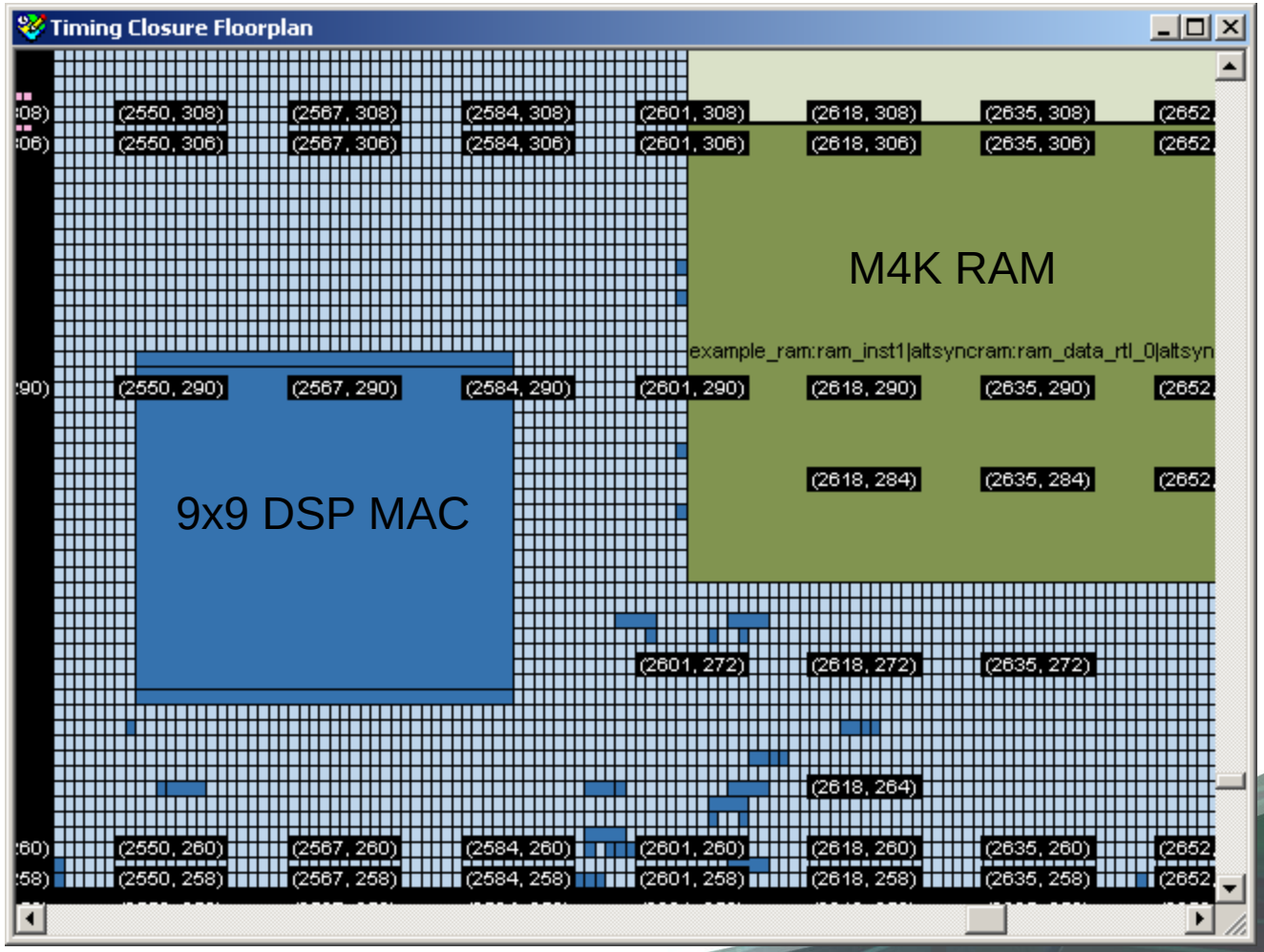
SOPC WORLD

HardCopy II Floorplan View



SOPC WORLD

HardCopy II Floorplan View



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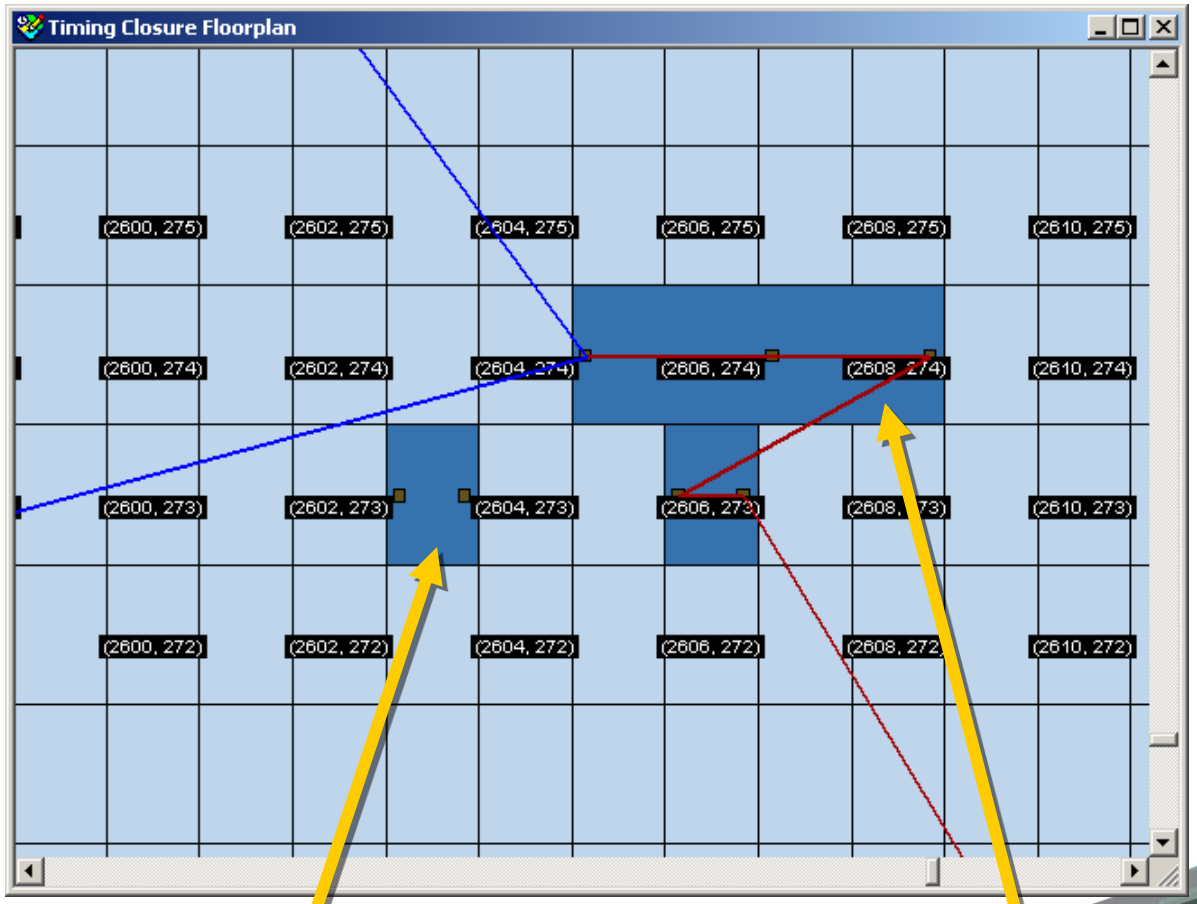
HardCopy II HCell Fabric



HCell Combinational Macro
(1 HCell Used)

HCell Register Macro
(4 HCells Used)

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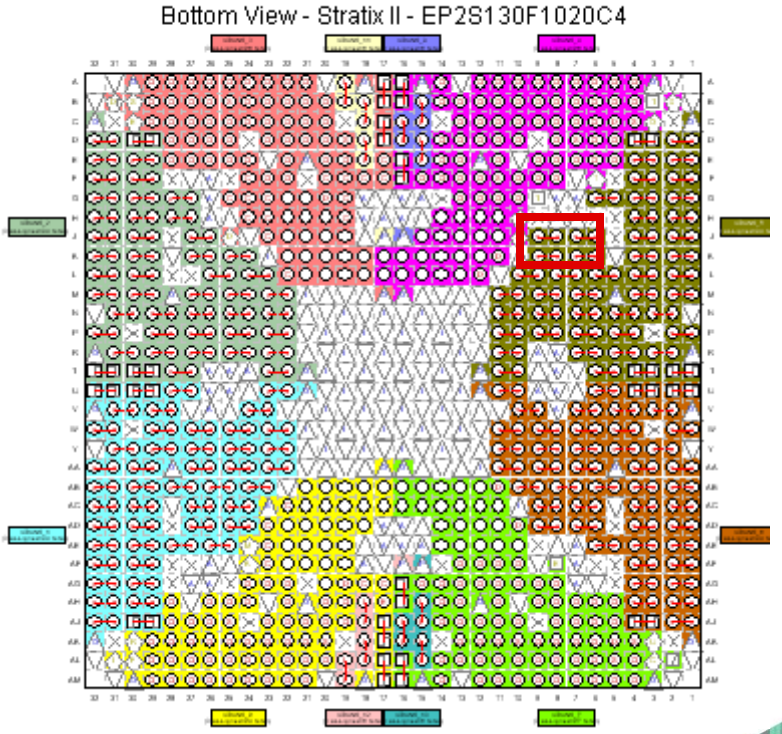
Stratix II Pin Planner View

Stratix II FPGA view without migration shows all pins are available



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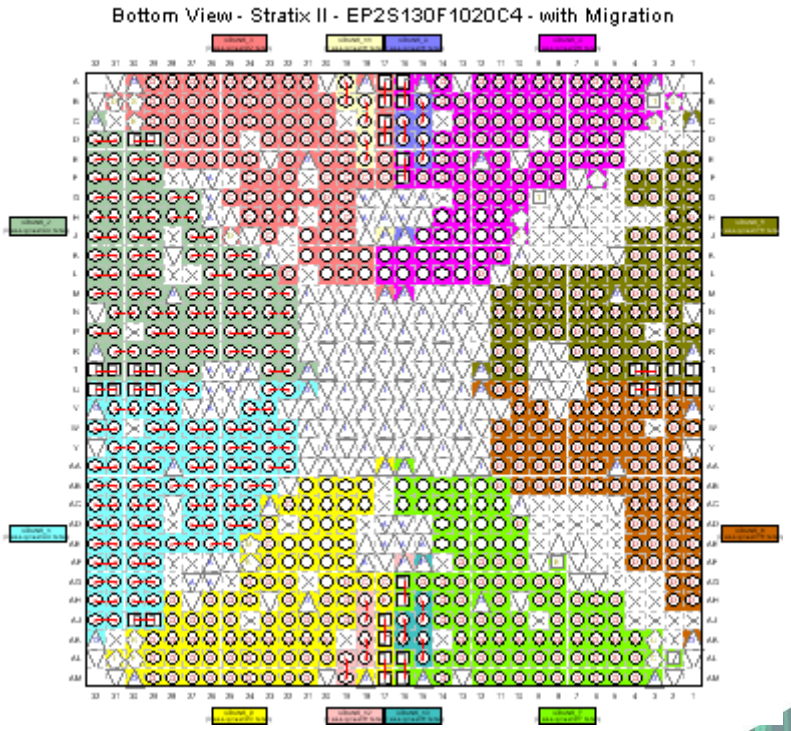
Stratix II Device With HardCopy II Migration

- With HardCopy II migration device enabled, unusable pins are hidden
- Still will show Stratix II required pins, Vcc pins, and Vss pins
- Rule checker assures simultaneous switching noise (SSN) rule compliance for both Stratix II and HardCopy II devices



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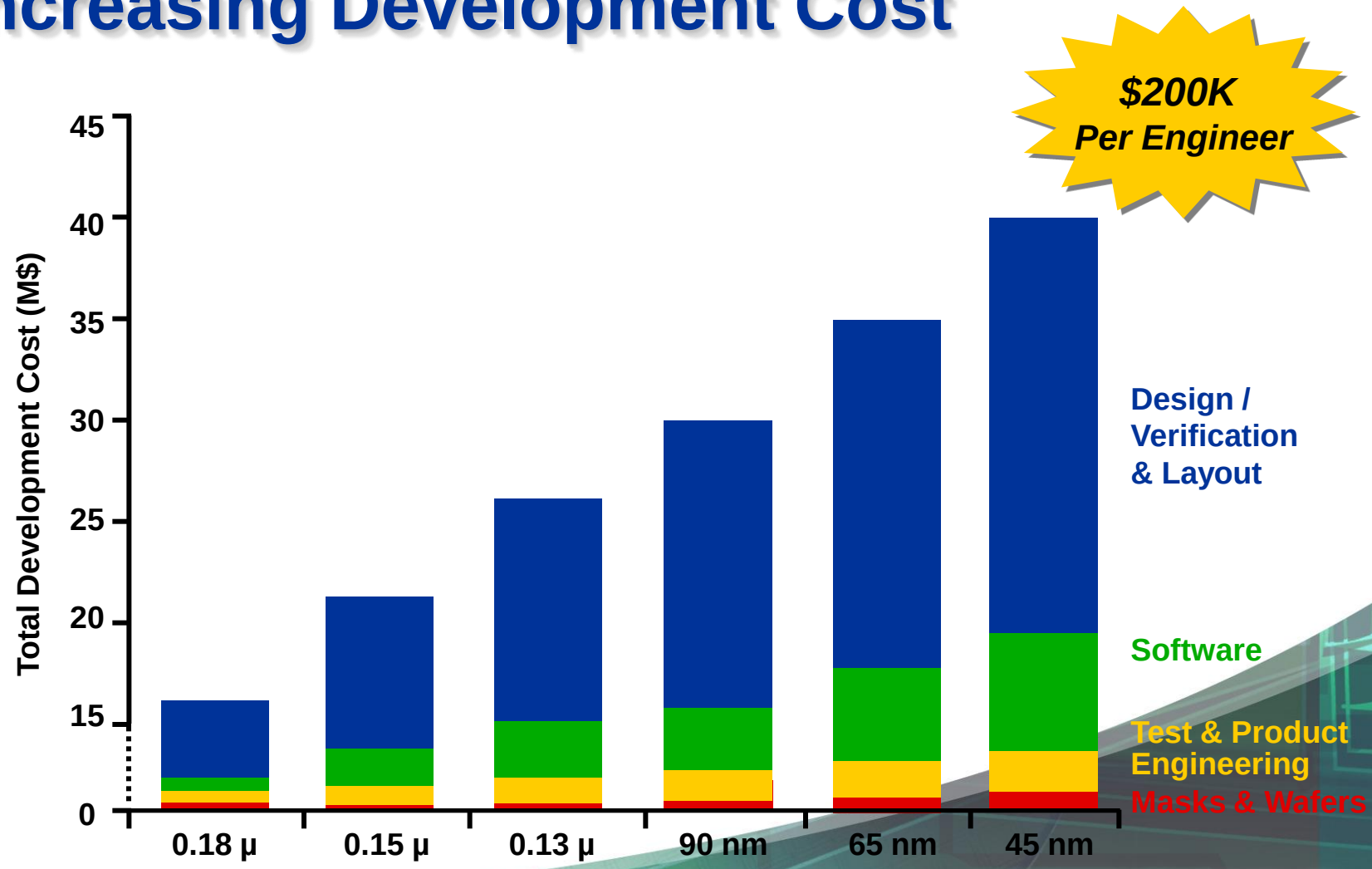
Back Up Business Slides

SOPC WORLD

Yesterday's Dilemma: Increasing Development Cost



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What If Companies Could…

- Introduce product 6-9 months earlier?
  - Implement customer feedback in silicon in real time
- Create multiple design variations?
  - Optimize the function and timing of each
- React to competitive threats and market changes instantaneously?
- Reduce development time?

Proposed Solution

Stratix II

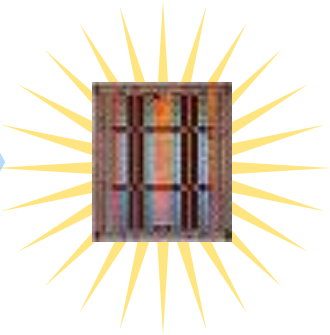
FPGA Prototype

QUARTUS II

Design Tool

HardCopy II

Structured ASIC



Get Low Development Costs & Maximum Flexibility With FPGAs

Convert to HardCopy Structured ASICs When Justified and Needed

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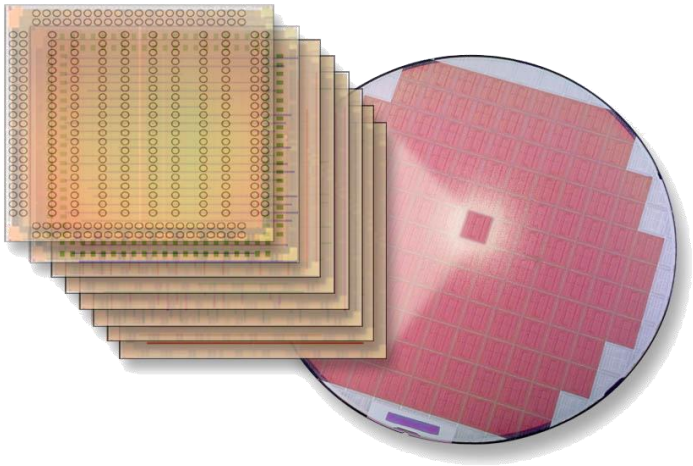
The Idea Behind HardCopy Structured ASICs

- Customers design with Altera Stratix series FPGAs
- In-house migration to a lower cost HardCopy device for higher volume applications with:
  - Same function/operation as the FPGA design
  - Same pin-out
  - Lower power
  - Higher performance
- How to make a lower cost HardCopy structured ASIC
  - Remove FPGA configuration circuitry
  - Remove FPGA programmable routing
  - Remove FPGA programmability for logic and memory
  - Add embedded testability
  - Customize with two metal layers

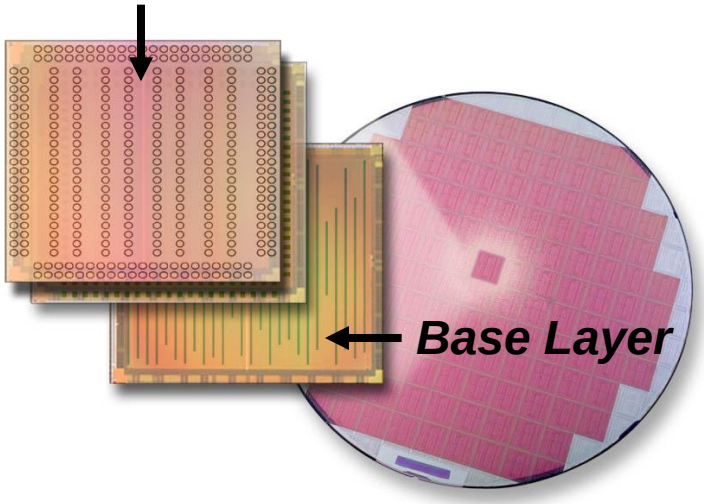
Standard Cell vs. Structured ASIC

All Layers are Custom



Full Set of Masks for Standard Cell ASIC

Pre-Fabricated Common Layers



Top Layers Customize Structured ASIC

Structured ASICs Deliver Low NRE Costs and Quick Turnaround Times

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Unique HardCopy Value

- Only Altera offers FPGAs **AND** structured ASICs
  - Leverage FPGA technology to build structured ASIC
- FPGA front-end design process
  - Design with Quartus II software
  - Test design in-system with FPGAs
  - Turnkey migration to drop-in replacement
- Significant benefits
  - Much lower risk of ASIC re-spin
  - Lower initial investment than standard cell
  - Use FPGA in early production
  - Smooth transition to HardCopy device
  - Transition back to FPGA at end of system life

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Additional Benefit: One Vendor

- Common tool flow: FPGA and HardCopy Devices
- Consistent technical support
- Transition logistics managed
- Clear accountability throughout
- FPGA use always an option

Only With HardCopy Structured ASICS

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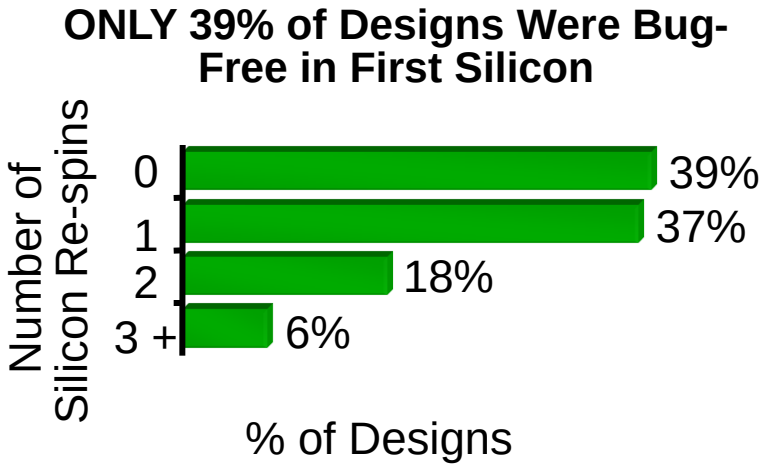
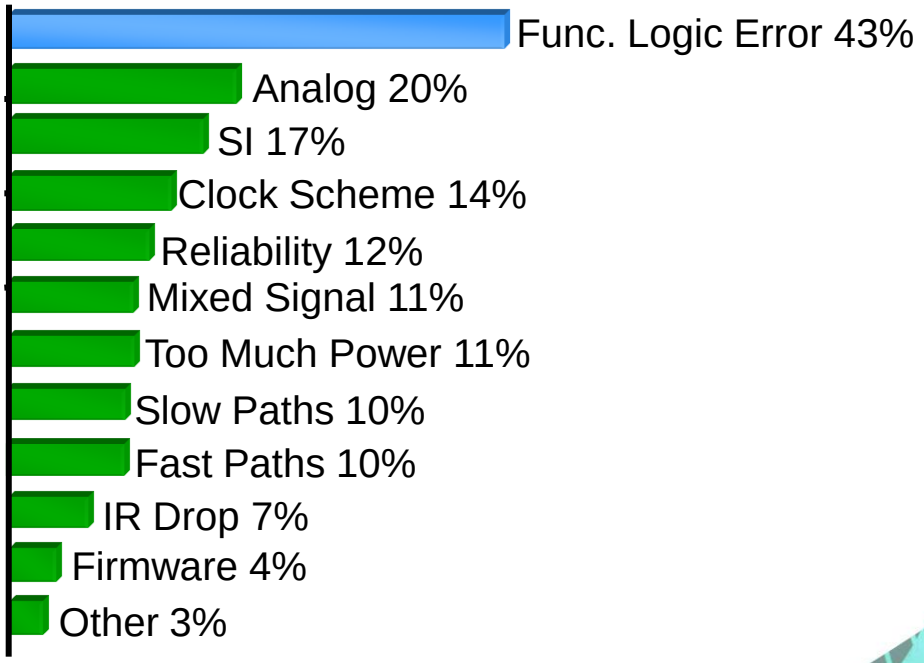
Solving The ASIC Re-Spin Problem



SOURCE: COLLETT INTERNATIONAL RESEARCH INC.



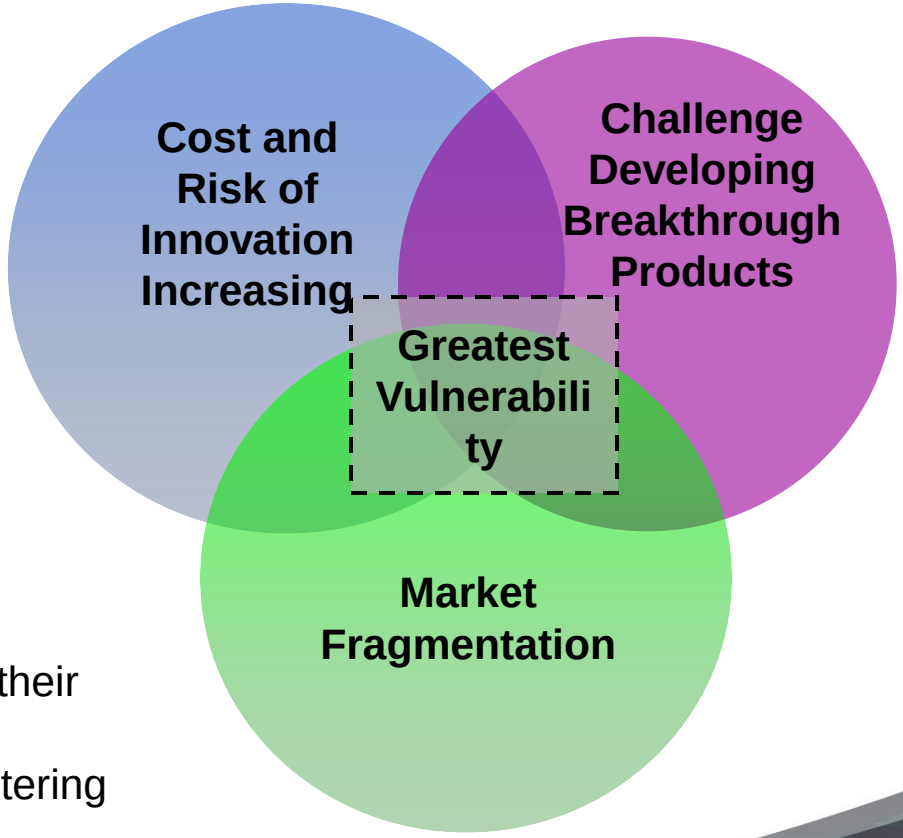
Aart de Geus, Chairman & CEO of Synopsys,
Boston SNUG Keynote Address, Sept. 2003

Prototyping With FPGAs Removes Functional Logic Errors

SOPC WORLD

Facing Multiple Challenges

- ASIC designs take 18-24 months
- Market can shift faster than planning and development
- New product may not impact market (but R&D already spent!)



- R&D budgets under pressure
- Design complexity increasing
- Companies react with minor product improvements (creeping incrementalism)

- End users demand products aligned to their specific needs
- New competitors entering to support market fragments

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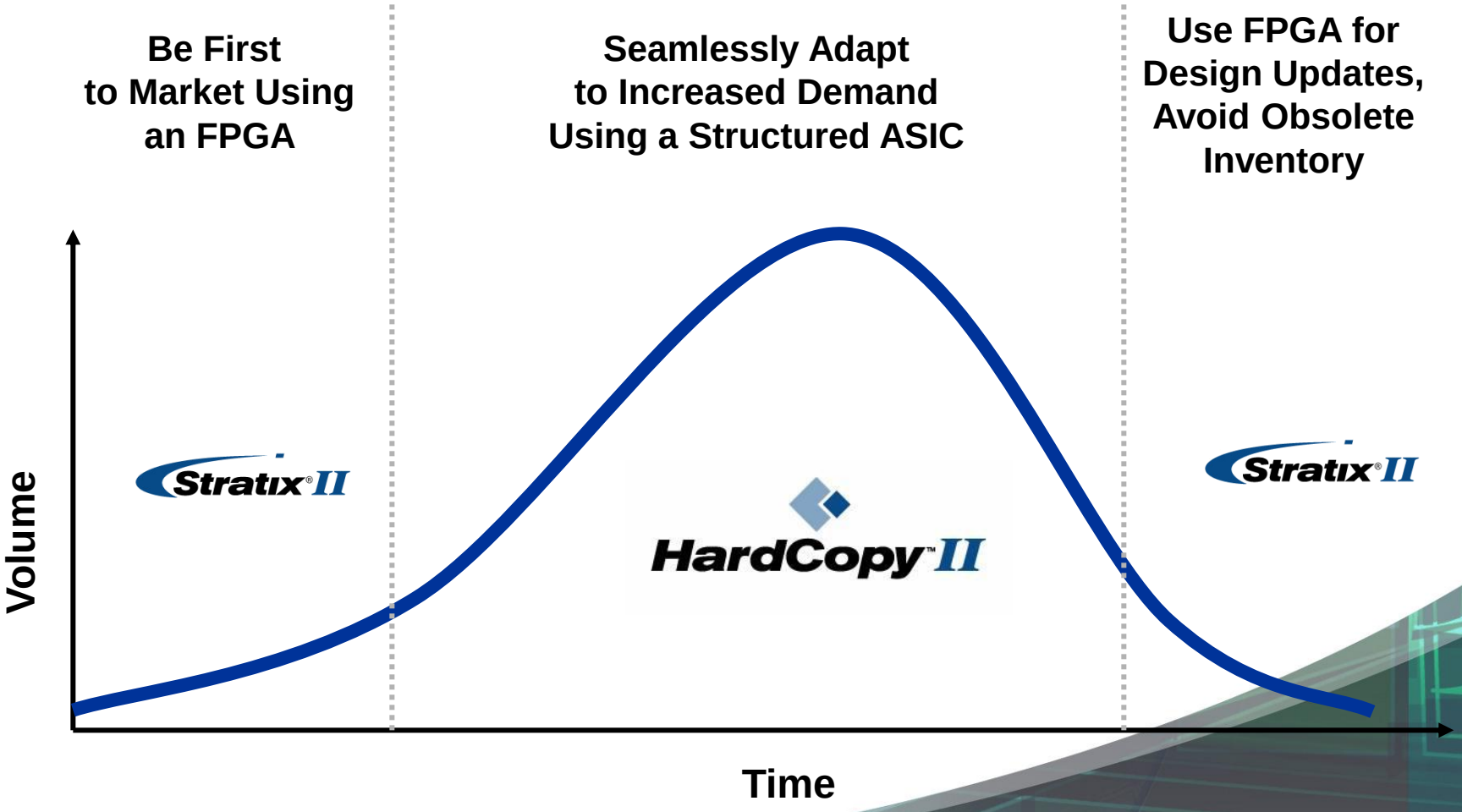
Solution for the Entire Product Life



Altera: Ideas-to-Production Partner

	Altera
Did I build the right product?	Design flexibility enables rapid changes and efficient test marketing
Did I build the product right?	In-system, at-speed testing throughout design cycle
Did I build the market demand?	Test market and build market plan during development
Can I build enough product to meet demand?	Use FPGAs or structured ASICs depending on volume and bill of materials (BOM) budget

Enabling Vision, Creativity, and Production

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