What You Need to Know About High-Speed Design

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Agenda

- Introduction
- High-speed design challenges
  - Optimizing signal integrity
    - Transceiver quality
    - Compliance to protocols
    - Pre-emphasis, equalization, and simultaneous switching noise (SSN)
  - Protocol implementation
- Conclusion

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Optimizing Signal Integrity

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What Is Signal Integrity (SI)?

- Signal quality
  - What is the signal condition at the receiver? Can it interpret the data correctly?
  - Measurement metrics: voltage margin, reflection noise, SSN
- Timing margin
  - Does the signal reach its destination when it is supposed to? Does the receiver have a good window for data recovery?
  - Measurement metrics: timing window, edge rates, jitter

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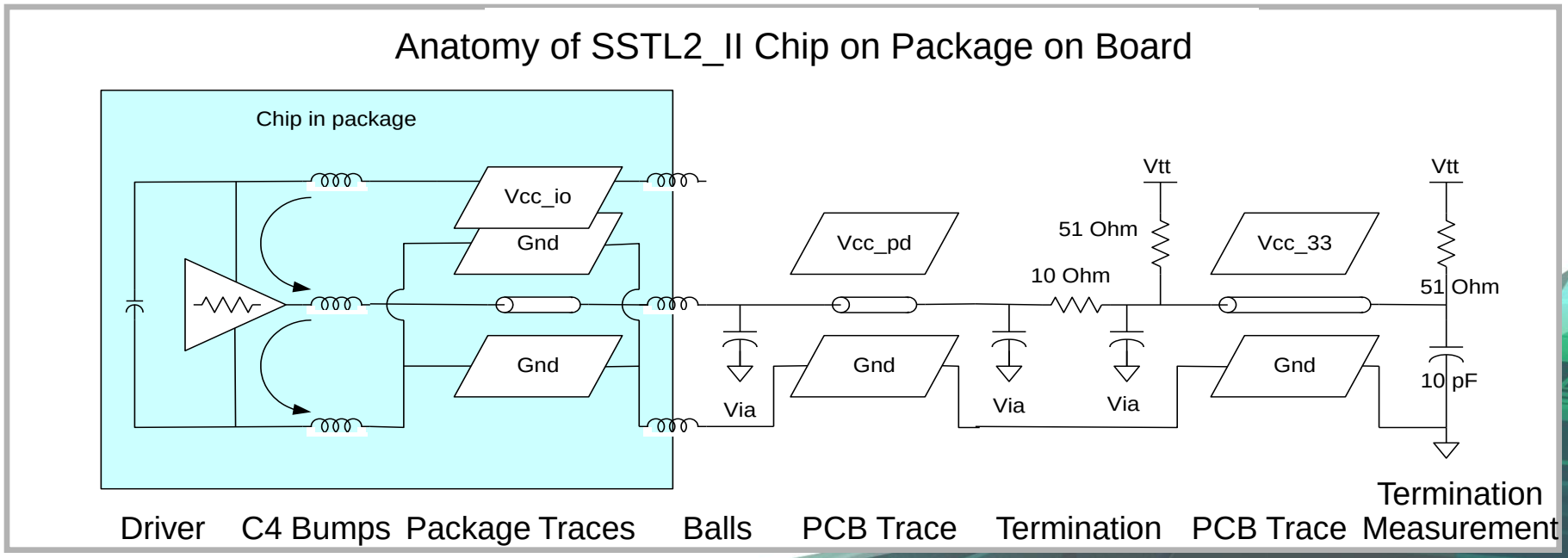
SI Concerns at the System Level

- Customer data at far end (eye opening)
- Coupled noise at near and far end (SSN)
- Power integrity
  - Ground and power nodes are references for signals



Costs of Poor Signal Integrity

- Delayed product releases
- Lost opportunities and revenues
- Field failures
- Poor reliability
- Degraded performance
- Expensive board re-spins

Factors Affecting Signal Integrity

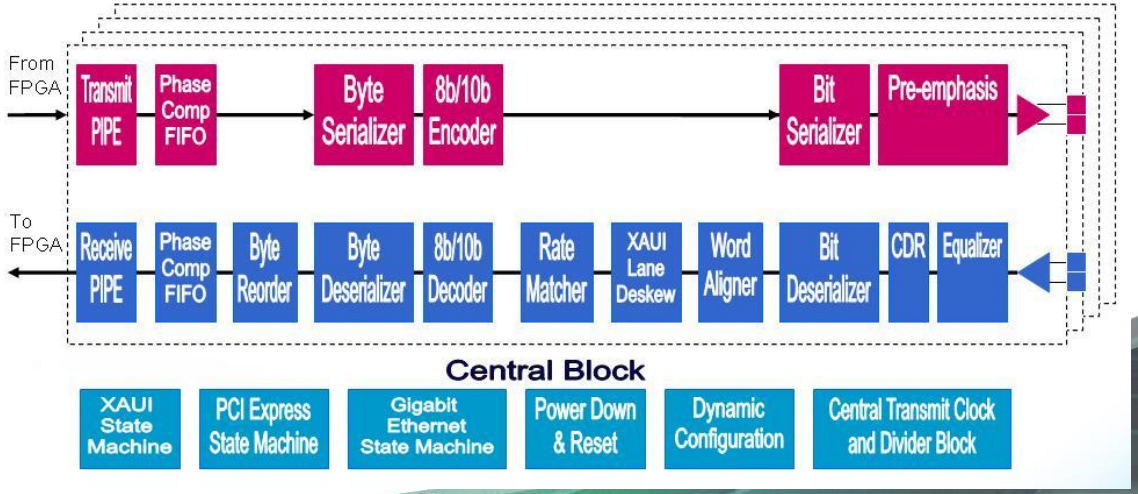
- Transmission line effects
- Impedance mismatch
- Signal attenuation
- Cross-talk
- Simultaneous switching outputs
- Related links
- Signal attenuation

Transceiver Considerations

- Transceiver selection criteria
  - Electrical compliance to protocol standards
  - Features to optimize signal integrity
  - Ease of use
- Protocol implementation criteria
  - Proven built-in personal communications system (PCS) hard intellectual property (IP)
  - Proven higher layer protocol stacks
  - Availability of development boards
- Other system considerations
  - Low-power transceivers with accurate power estimator tools
  - Board power distribution network (PDN), layout, and debugging guidelines

Complete Transceiver Building Blocks

- 622 Mbps – 6.375 Gbps
- Pre-emphasis and equalization
- Generic (basic) transceiver functionality
  - 8b/10b ENDEC
  - Rate matcher
  - Phase compensation FIFO buffer
  - 8-,10-,16-, 20-, 32-, 40-bit interface to core
- PCI Express state machine
  - Power state sequencing
  - Electrical idle, receive detect, and others
  - Physical interface for PCI Express (PIPE) interface to core
- PCI Express state machine
  - Power state sequencing
  - Electrical Idle, receive detect, and others
  - PIPE interface to core
- Gigabit Ethernet (GbE) state machine
  - Comma character insertion/deletion
  - Gigabit medium independent interface (GMII)-like interface to core
- XAUI state machine
  - Channel deskew, alignment, and bonding
  - XGMII-like interface to core



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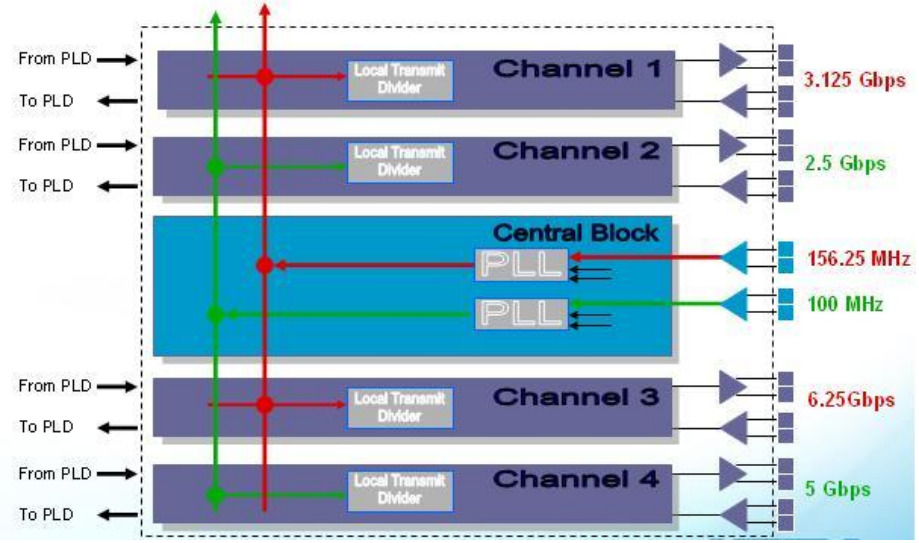
Efficient Quad Architecture with Channel Flexibility

- Supports 2 clock domains
- Supports up to 4 distinct rates from 622 Mbps to 6.375 Gbps
- Clock lines connected to adjacent quad minimize skew between channels
- Dynamic reconfiguration of transceiver data rates and modes supported in Quartus® II software ver. 6.1 (November 2006)



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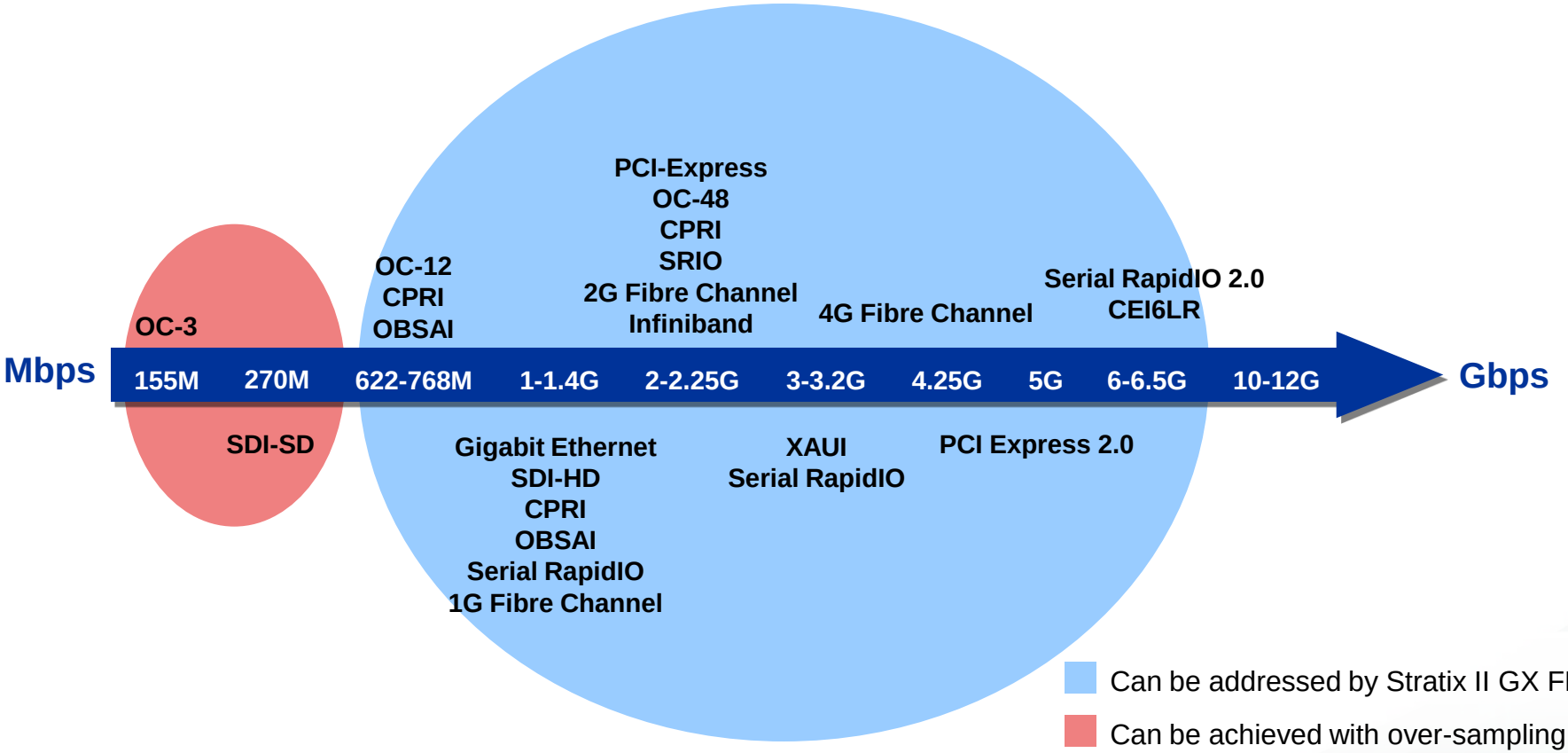
Stratix® II GX Protocols & Rates



Optimized Performance for Applications Between 622 Mbps and 6.375 Gbps

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Standards Supported

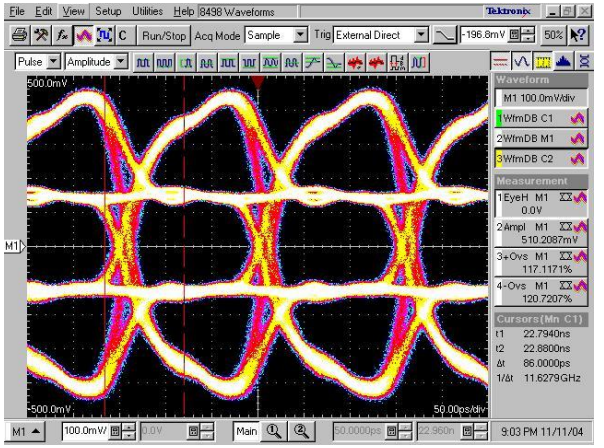
Standards	Data Rate	Built-in PCS blocks
PCI Express 1.1	2.5 Gbps	PIPE-compliant
OIF CEI 6G	6.25 Gbps	8B/10B
Gigabit Ethernet	1.25 Gbps	IEEE gigabit Ethernet PCS
Serial Rapid I/O	1.25, 2.5, 3.125	8B/10B
XAUI	3.125 Gbps	IEEE XAUI PCS
SD-SDI	270 Mbps	No special blocks for SDI
HD-SDI	1.488 Gbps	No special blocks for SDI
SONET OC-12	622 Mbps	A1A2 pattern detector and aligner
SONET OC-48	2.488 Gbps	A1A2 or A1A1A2A2 pattern detector and aligner
3G Basic	622 Mbps to 3.1875 Gbps	For proprietary protocols: 8B/10B
6G Basic	3.1875 Gbps to 6.375 Gbps	For proprietary protocols: 8B/10B

Stratix II GX Features for SI

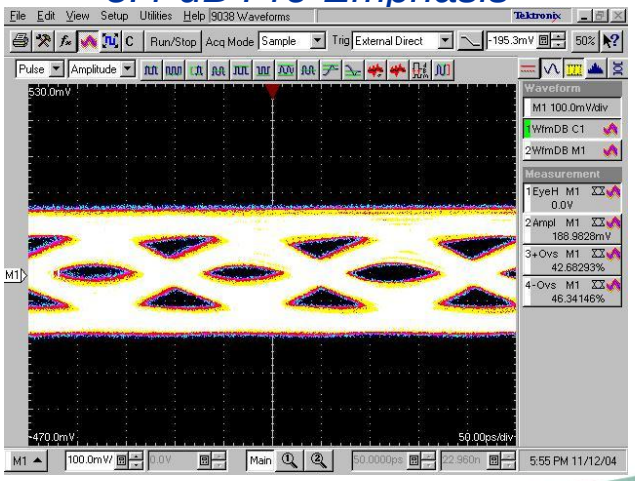
- **On-chip termination**
  - Simplifies board layout
  - Removes need for additional PCB trace stubs
- **Programmable V_{OD} settings in I/O buffers**
  - Enables user to select level for system design or to meet protocol standard
- **Pre-emphasis**
  - Delivers improved signal integrity, allowing 6.375 Gbps across 40 inches of FR-4 PCB material
  - Enables legacy systems to run faster
- **Receiver equalization**
  - Delivers improved signal integrity, allowing 6.375 Gbps across 20 inches of FR-4 PCB material
  - Enables legacy systems to run faster
  - Detects correct level automatically, reducing PCB design risk

Stratix II GX: Pre-Emphasis

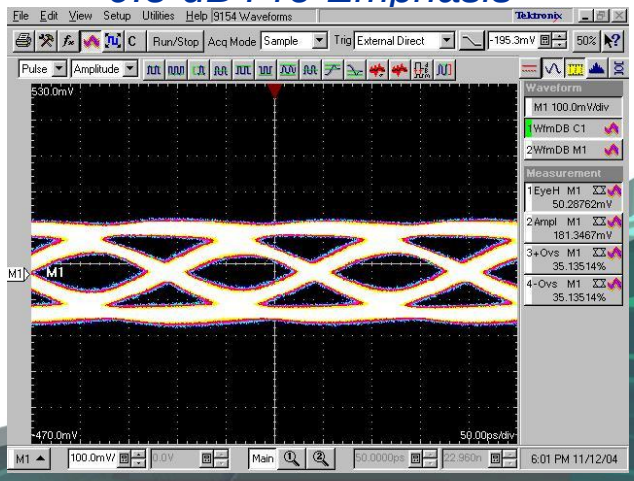
- Boosting initial voltage level of each edge to compensate for high-frequency loss
- Magnitude of pre-emphasis needed depends on cumulative interconnect loss (e.g., trace length)



5.4-dB Pre-Emphasis

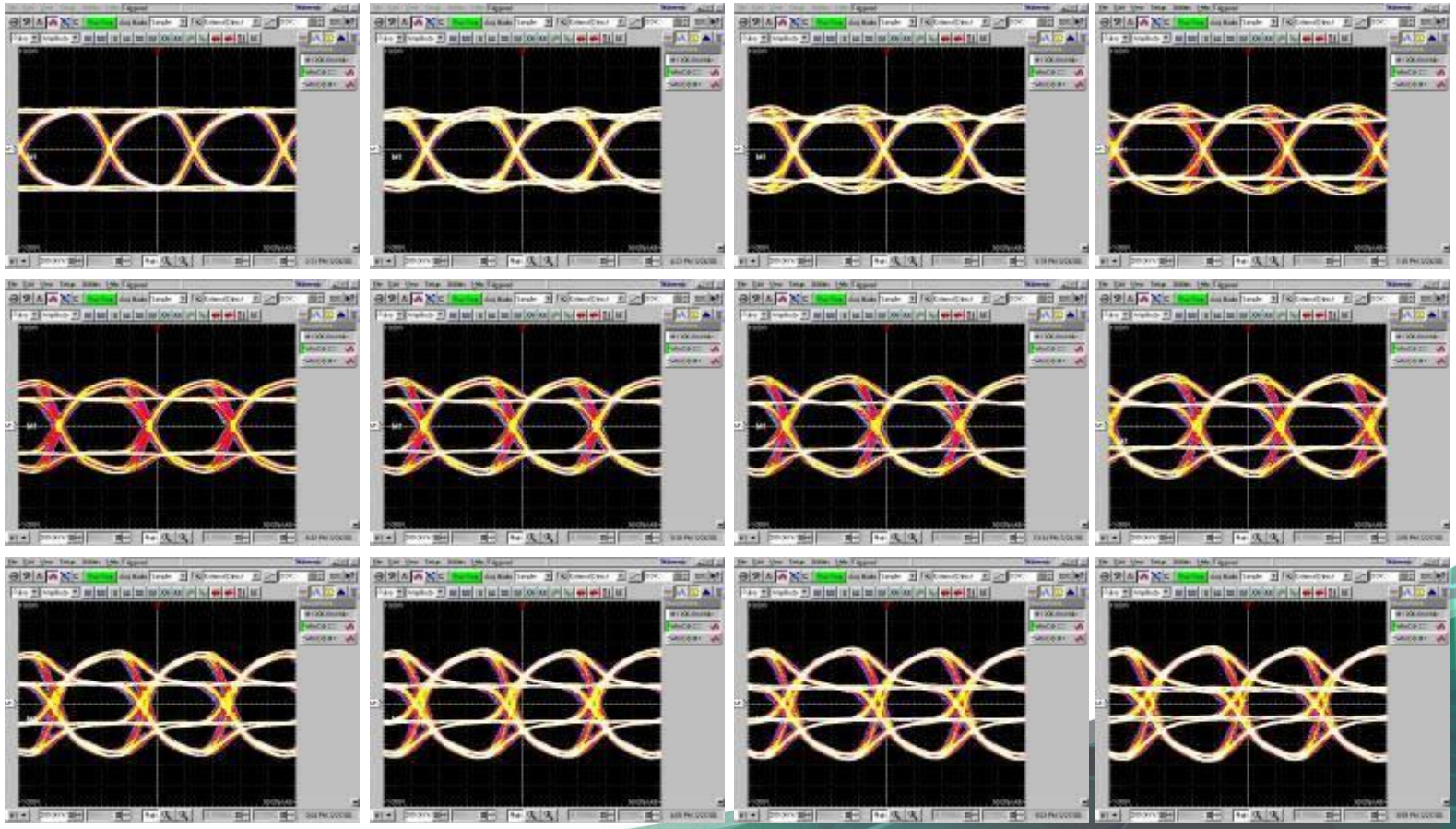


9.5-dB Pre-Emphasis



Stratix II GX Pre-Emphasis: 6.375 Gbps

- Dynamically configurable pre-emphasis (3 taps) plus V_{OD}
- Example: 800-mV V_{OD} with different first-post tap settings



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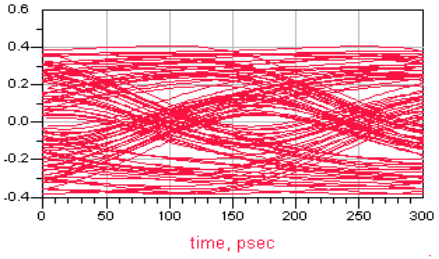
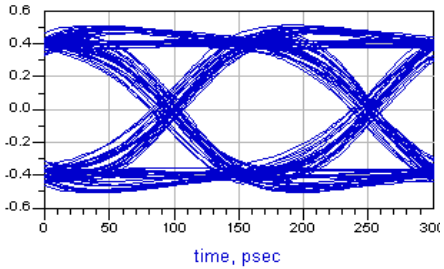
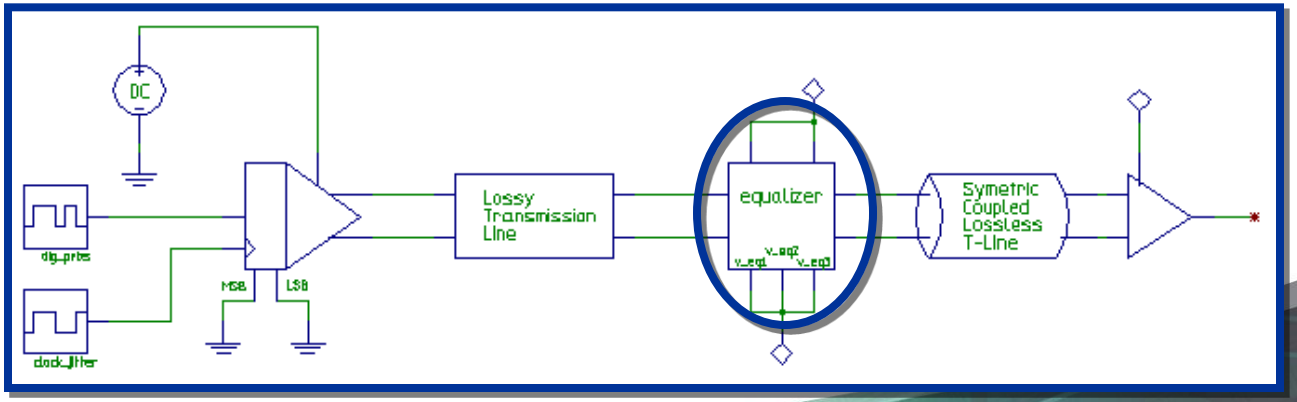
Stratix II GX: Equalization

- Receiver accounts for signal loss
- Passive equalization
  - Lower-frequency harmonics are attenuated to match attenuation at higher frequencies
- Active equalization
  - Higher-frequency harmonics are boosted to compensate for interconnect attenuation



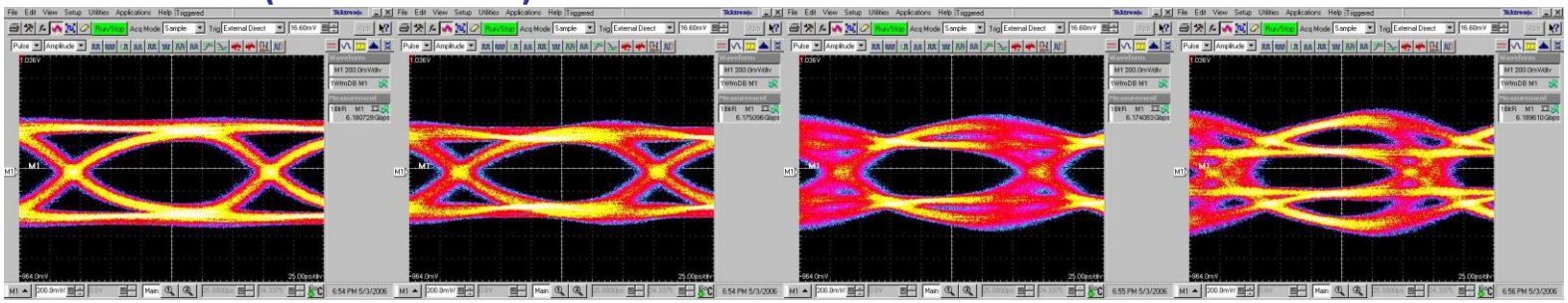




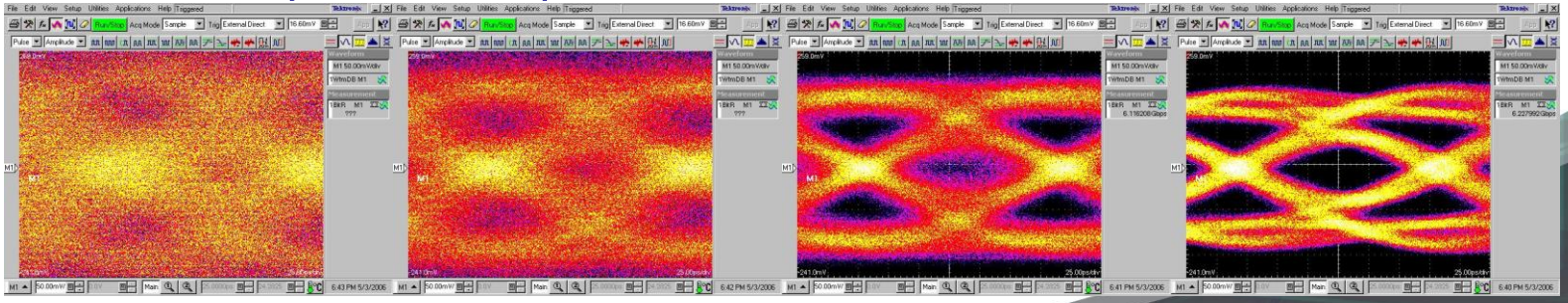
Pre-Emphasis and/or Equalization Compensates for PCB Degradation

Increasing pre-emphasis levels

3" PCB Trace (FR-4 Material)



40" PCB Trace (FR-4 Material)



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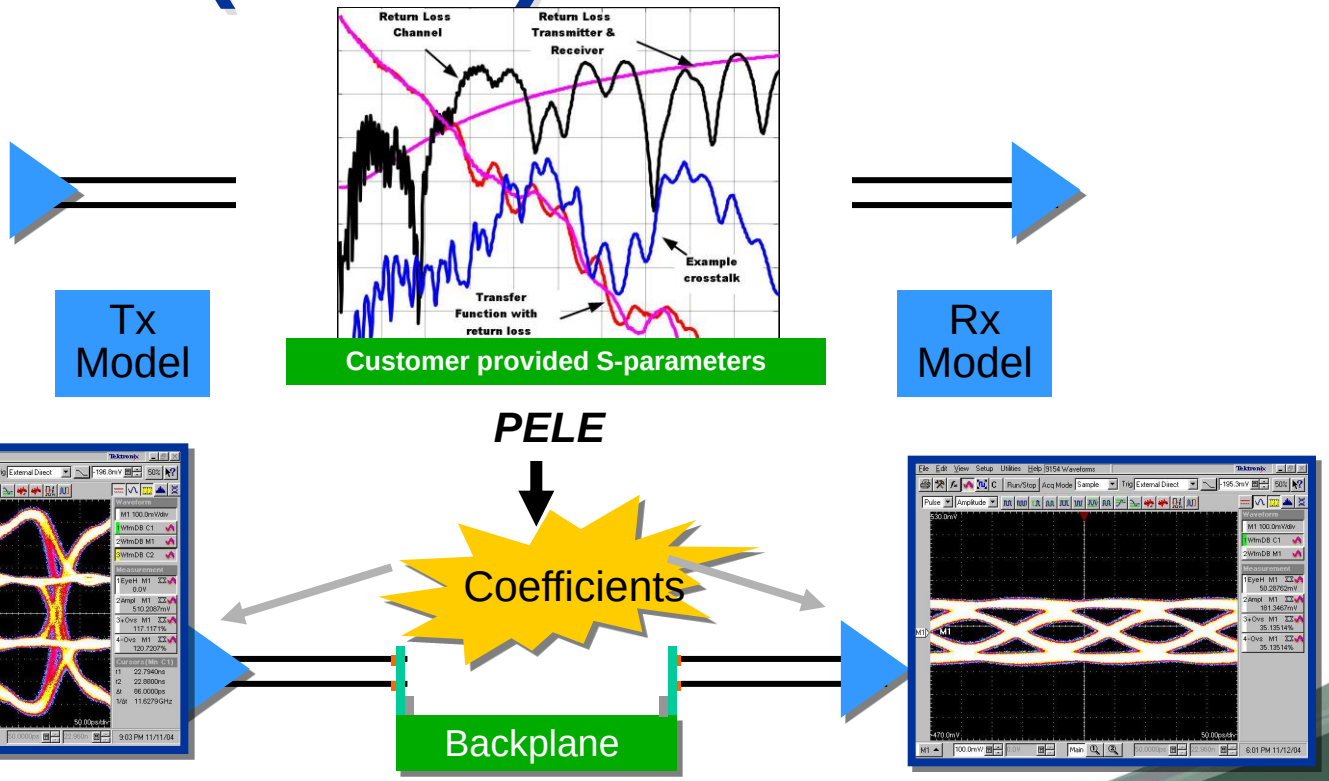
Altera's Pre-Emphasis and Link Estimator (PELE)



- Proprietary EDA tool for determining pre-emphasis and equalization coefficients

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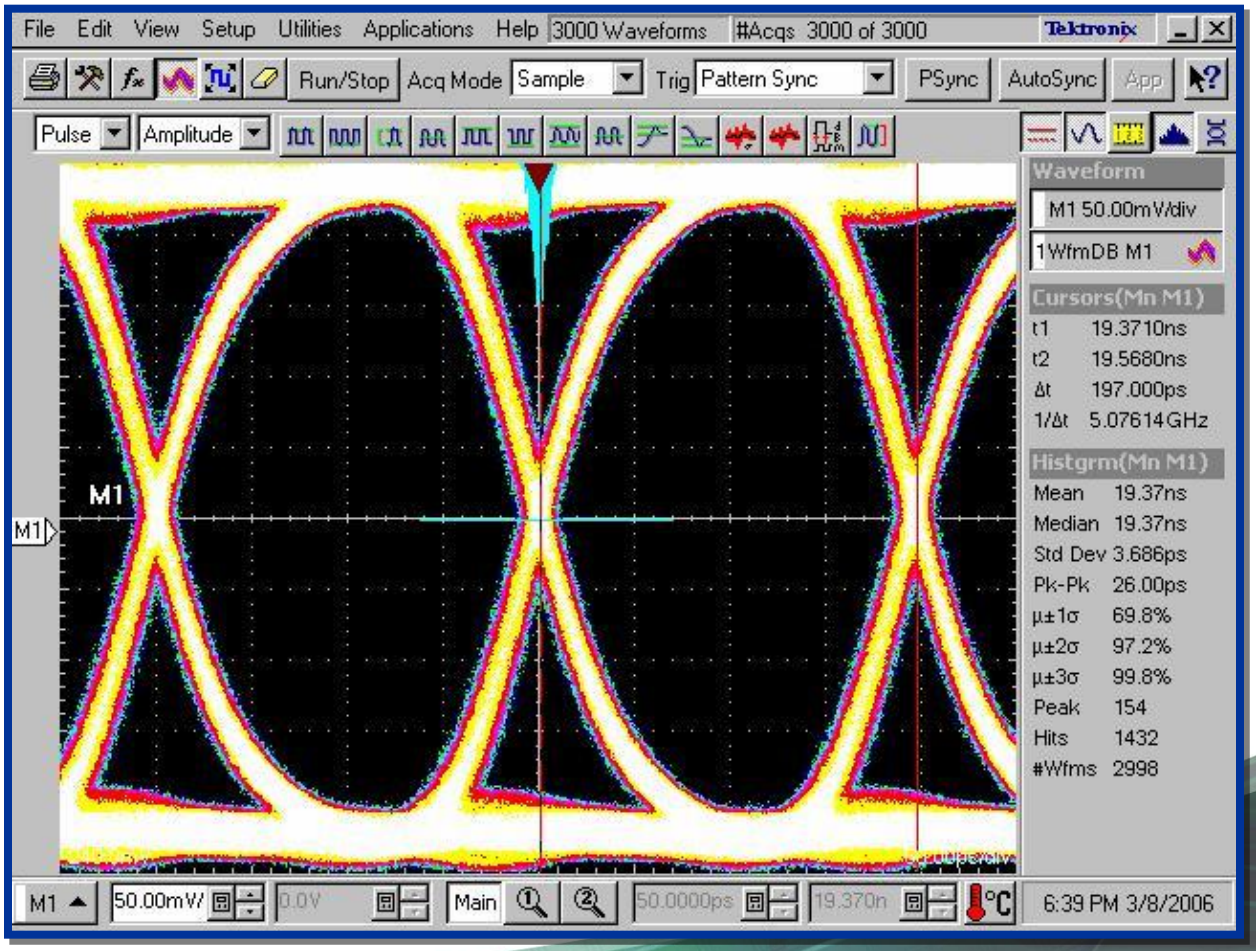
Stratix II GX Eye Diagram: 6.375 Gbps

- Wide-open eye indicates cleaner data transfers



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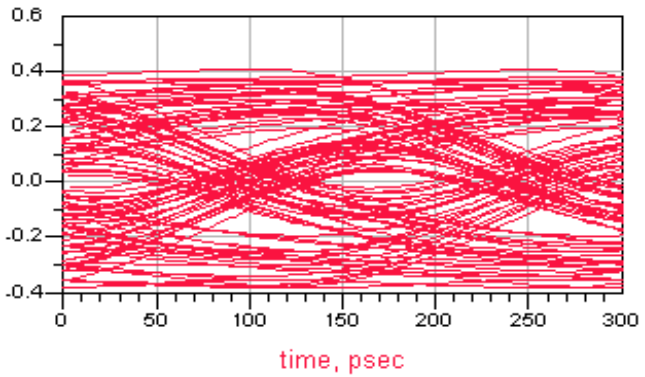
Best-in-Class Signal Integrity

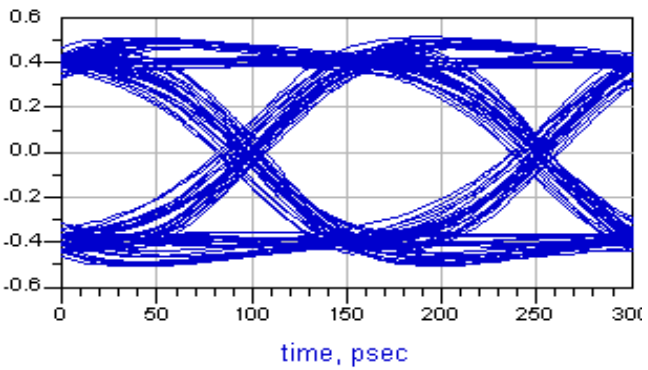
Receive

6.375 Gbps

Simulated Receive Eye, With No Equalizer



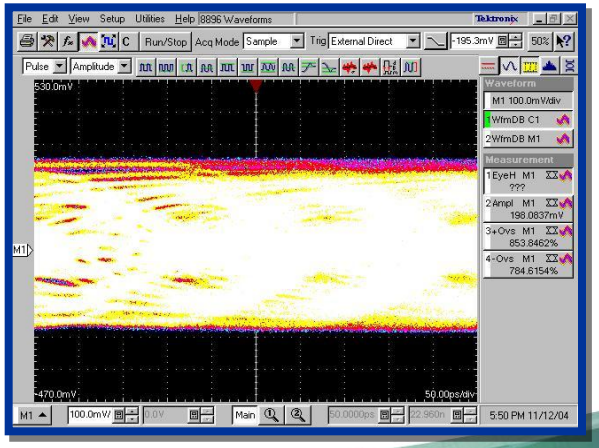
Simulated Receive Eye, With Equalizer



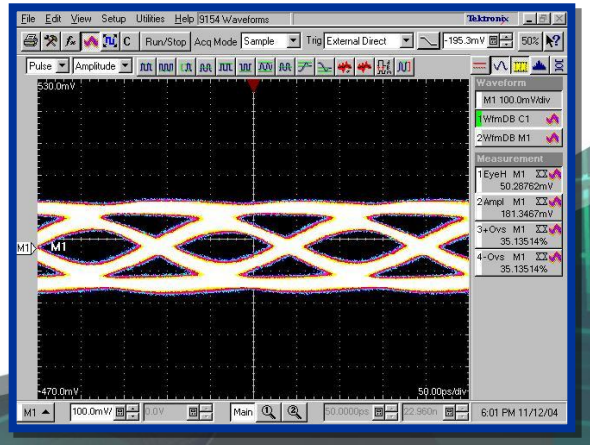
Transmit

6.375 Gbps

Eye Opening After 34” Tyco Backplane



Eye Opening After 34” Tyco Backplane and 9.5-dB Pre-Emphasis



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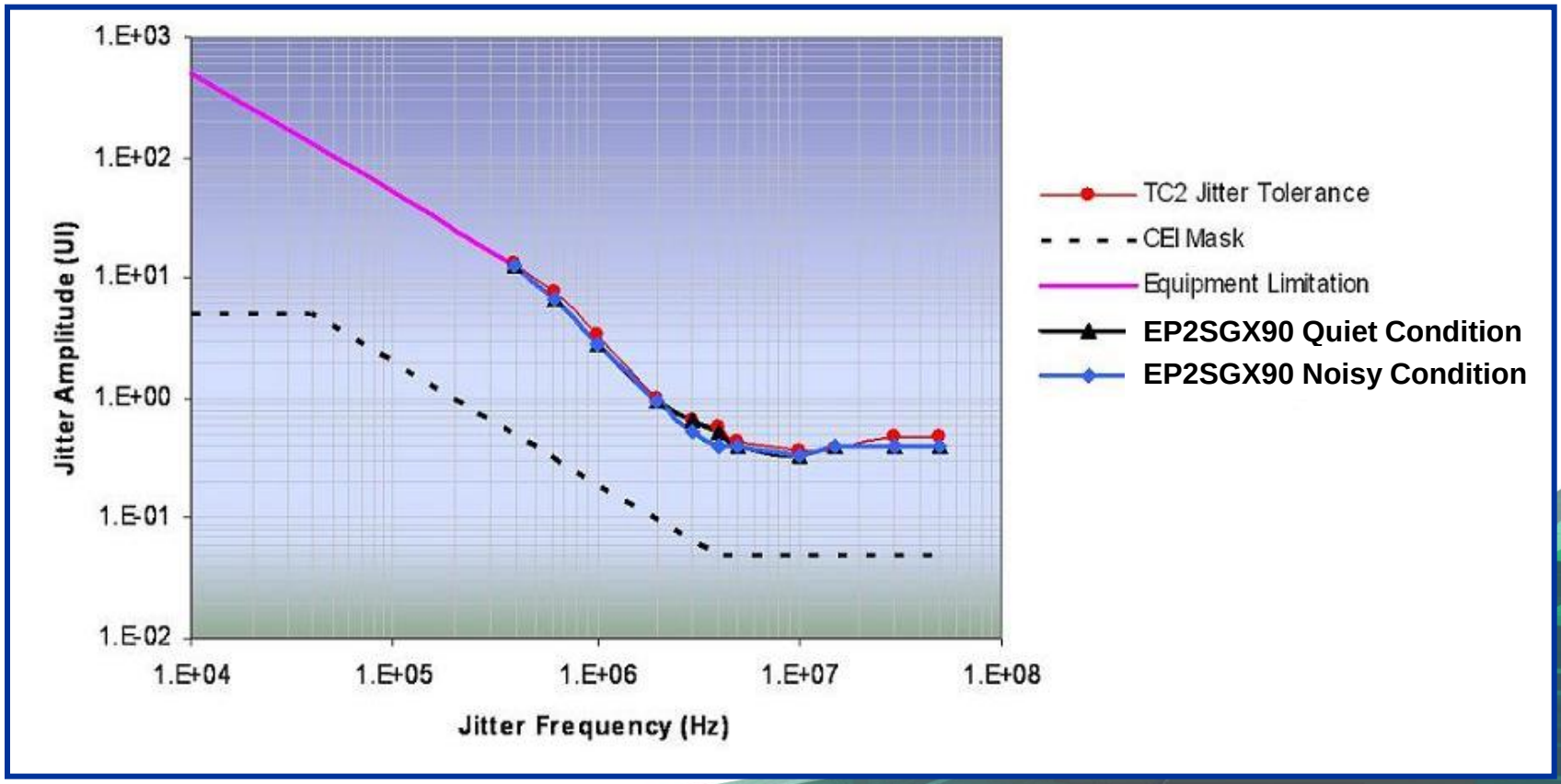
Stratix II GX RX Jitter Tolerance: 6.375 Gbps

- Excellent jitter tolerance with 80% core noise and 80% I/O switching



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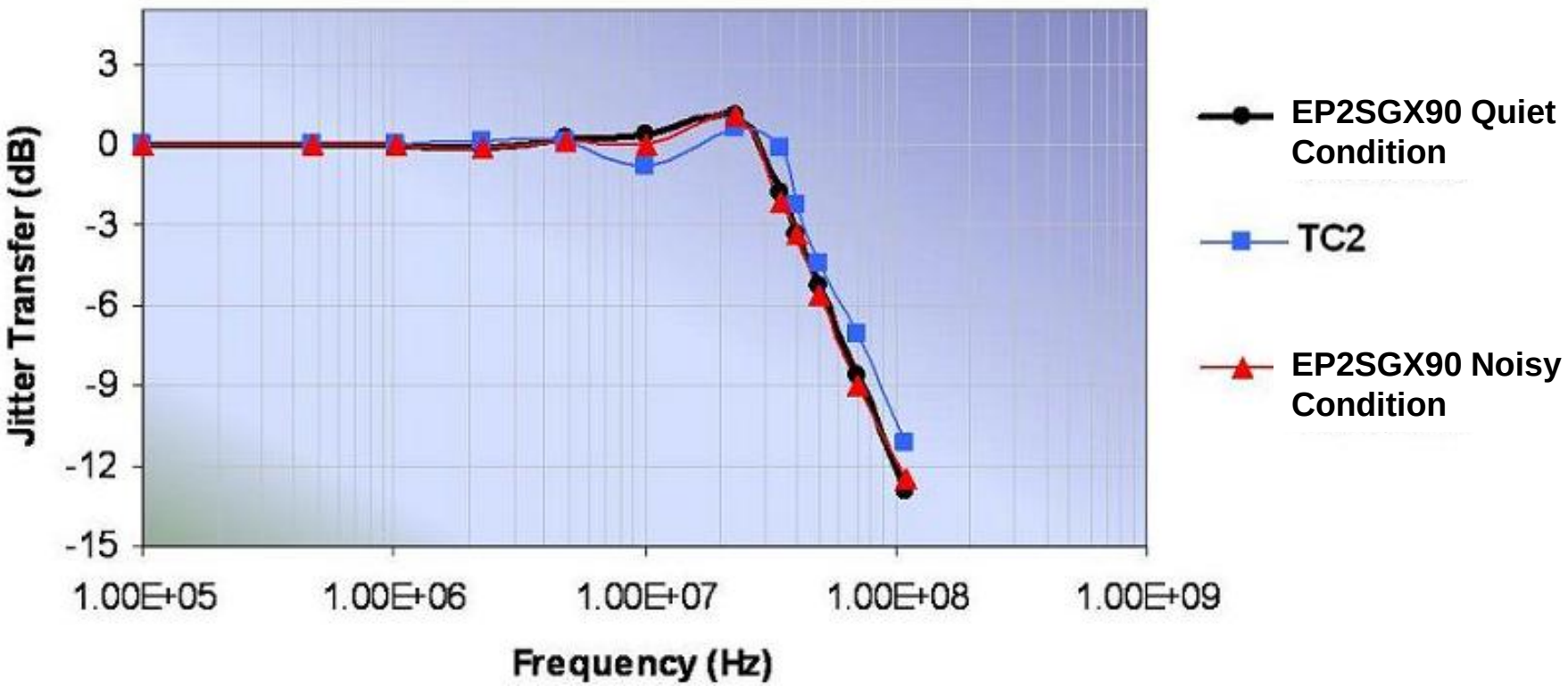
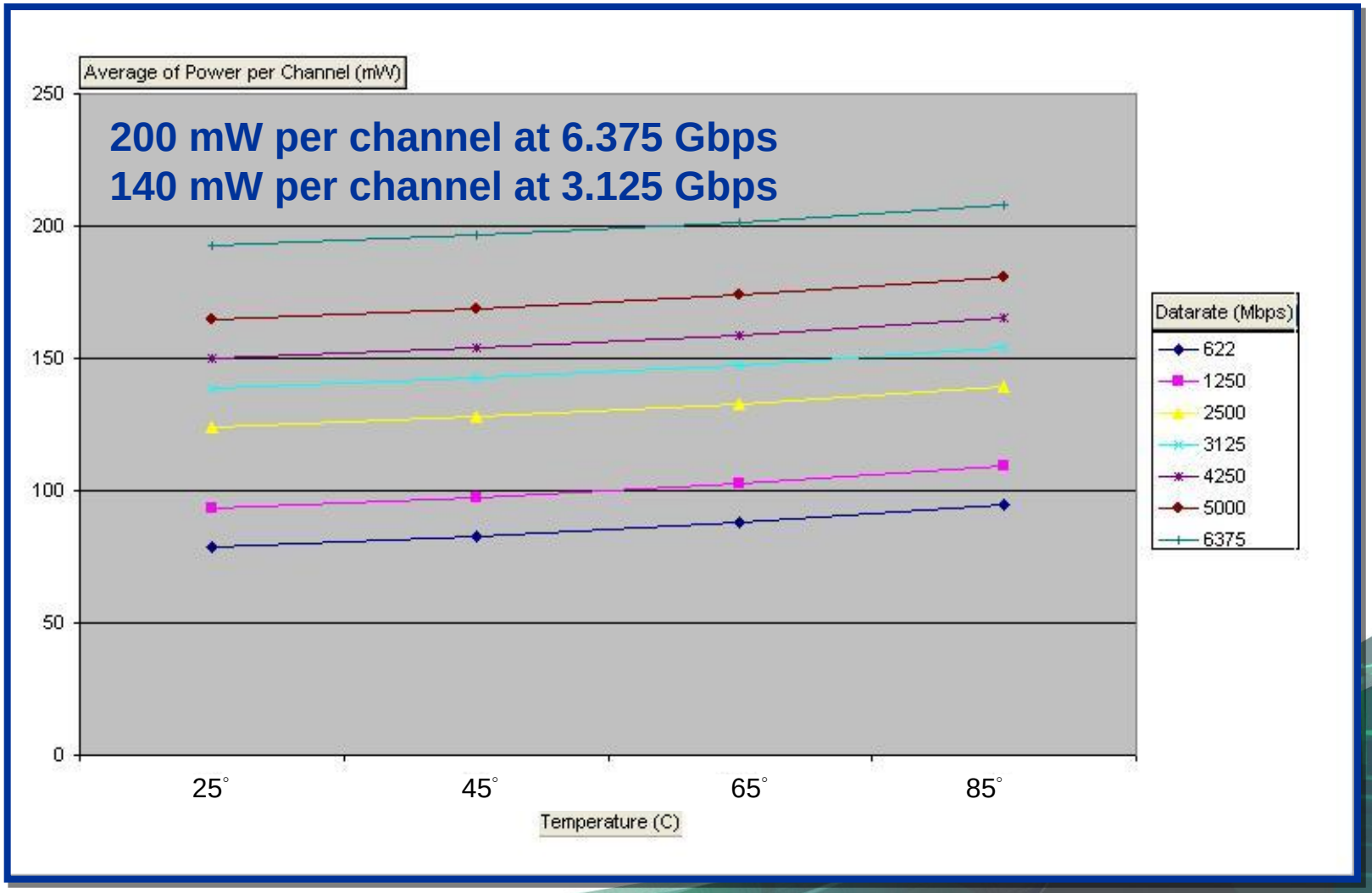
Stratix II GX RX Jitter Transfer: 6.375 Gbps

- Excellent jitter transfer with 80% core noise and 80% I/O switching



Low-Power Transceivers



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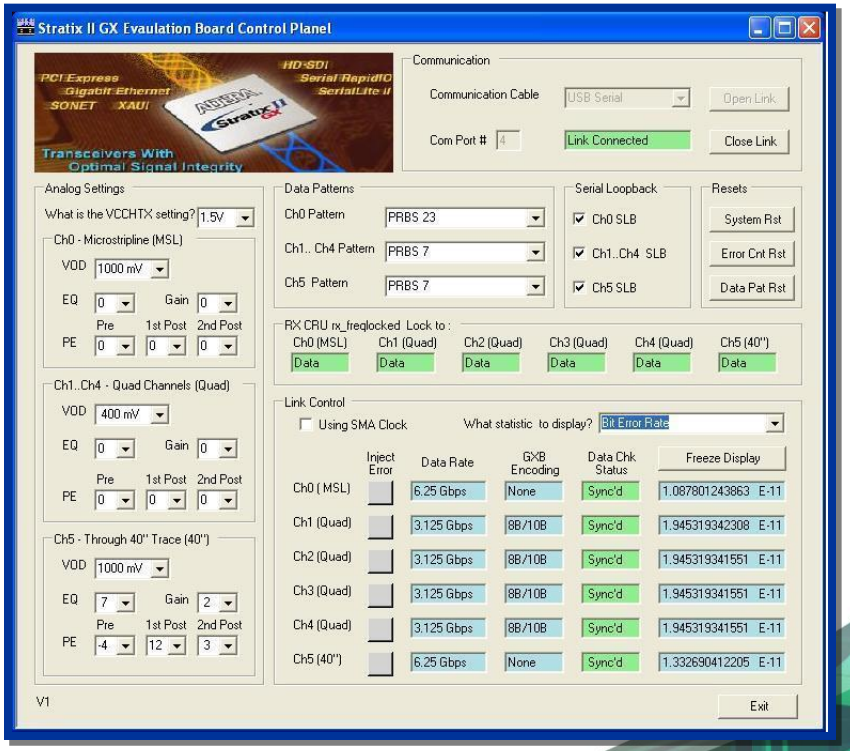
Channel Optimization Tools

- Optimize signal integrity by dynamically controlling
  - Differential output voltage
  - Transmit pre-emphasis
  - Receive equalization and gain
- Select pattern based on encoding scheme
  - PRBS 7, 15, 23
  - 0101 pattern
- Monitor errors
  - Number of errors and bit error rates
- Supply external clock for jitter generation and tolerance measurements
- Quantify transceiver power by powering down channels



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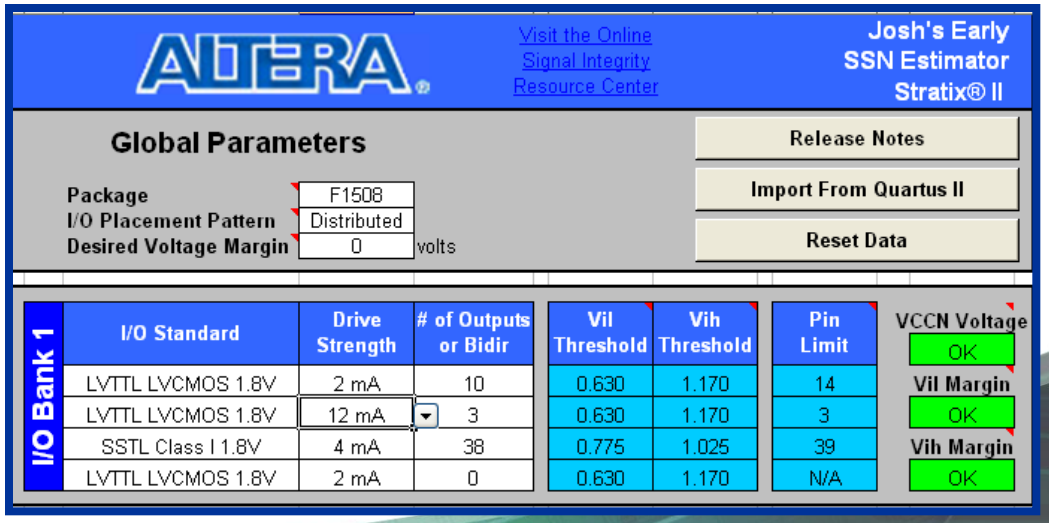
Signal Integrity Tools

- Focus on minimizing SSN
  - Early SSN Estimator (Excel-based)
  - Quartus II SSN Estimator
- Focus on overall system-level signal integrity analysis
  - Third-party EDA tool support
  - Quartus II SI Analyzer

Early SSN Estimator (Excel-based)

Early SSN Estimator (Excel-based Spreadsheet) Goal: Provide pre-design SSN evaluation	
Analysis Input	■ Early in the design cycle (partial or no design) ■ Enter I/O properties (e.g., I/O standard, current strength, etc.) ■ Enter board parameters (e.g., number of layers, board stack-up, etc.)
Analysis Output	■ Report and warn if VCC sag and ground bounce limits are exceeded



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Quartus II SSN Estimator

Quartus II SSN Estimator Goal: Assist in SSN management during design phase	
Analysis Input	▪ Enter I/O properties (e.g., I/O standard, current strength, etc.) ▪ Enter board parameters (e.g., number of layers, board stack-up, etc.)
Analysis Output	■ Report and warn if VCC sag and ground bounce limits are exceed ■ Highlight areas of high SSN and advise on alternative pin placement – Integrate with Quartus II Pin Planner ■ Report timing push-out/push-in – Integrate with Quartus II TimeQuest Timing Analyzer

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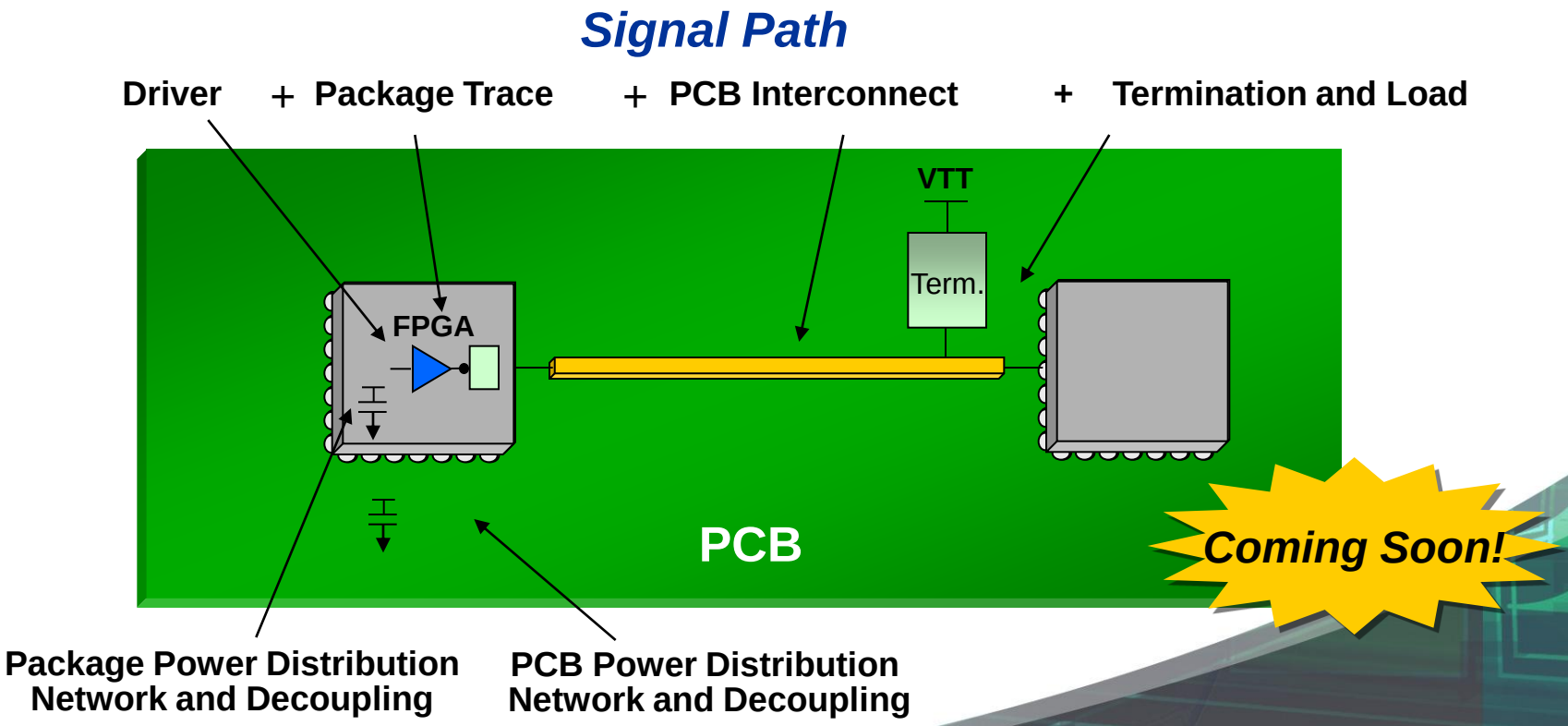
Quartus II SI Analyzer

- Goal: Detailed modeling of entire I/O signal path and power distribution network

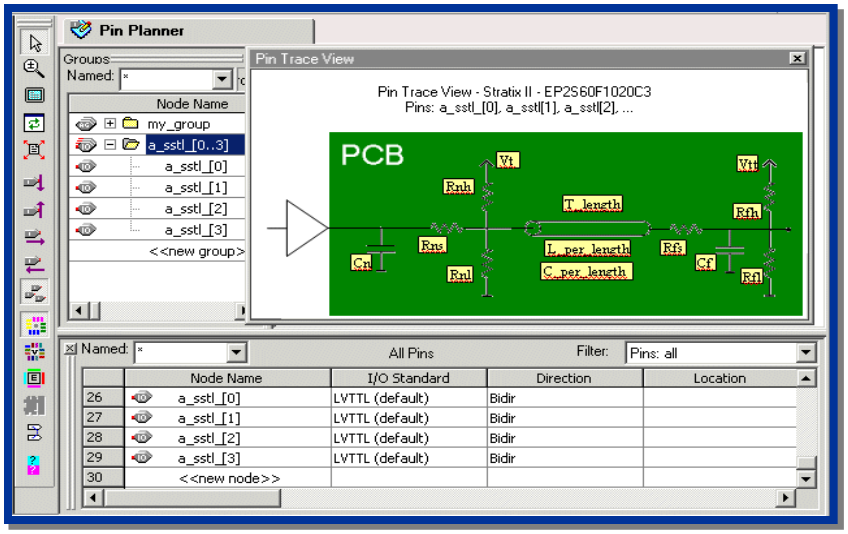


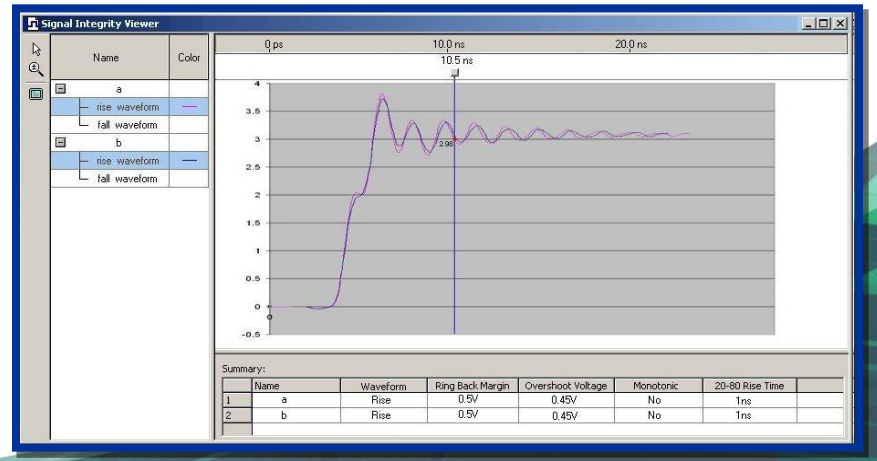
Quartus II SI Analyzer

Quartus II SI Analyzer Goal: Provide system-level signal integrity analysis using internal circuit simulation engine	
Analysis Input	Based on Quartus II design and device database: ■ Exact I/O configuration of design (I/O buffer model) ■ Package model User-entered: ■ Board trace and load on each I/O (simplified board model) ■ Relevant PCB power plane parameters and decoupling caps
Analysis Output	■ Delay for each I/O ■ Analog voltage vs. timing waveform for each I/O ■ Incorporate Quartus II SSN Estimator to include SSN effects

Quartus II SI Analyzer Tools

- Enter board characteristics
  - Signal path terminations (I/O load capacitance + board trace)
  - Integrate with Quartus II Pin Planner
- Signal integrity report panel will be added under Fitter report
  - Locate to Quartus II Waveform Viewer
- Quartus II Waveform Viewer
  - Analog voltage vs. time waveform
  - Delay to FPGA pin and destination pin
  - Signal quality metrics (e.g., overshoot, etc.)





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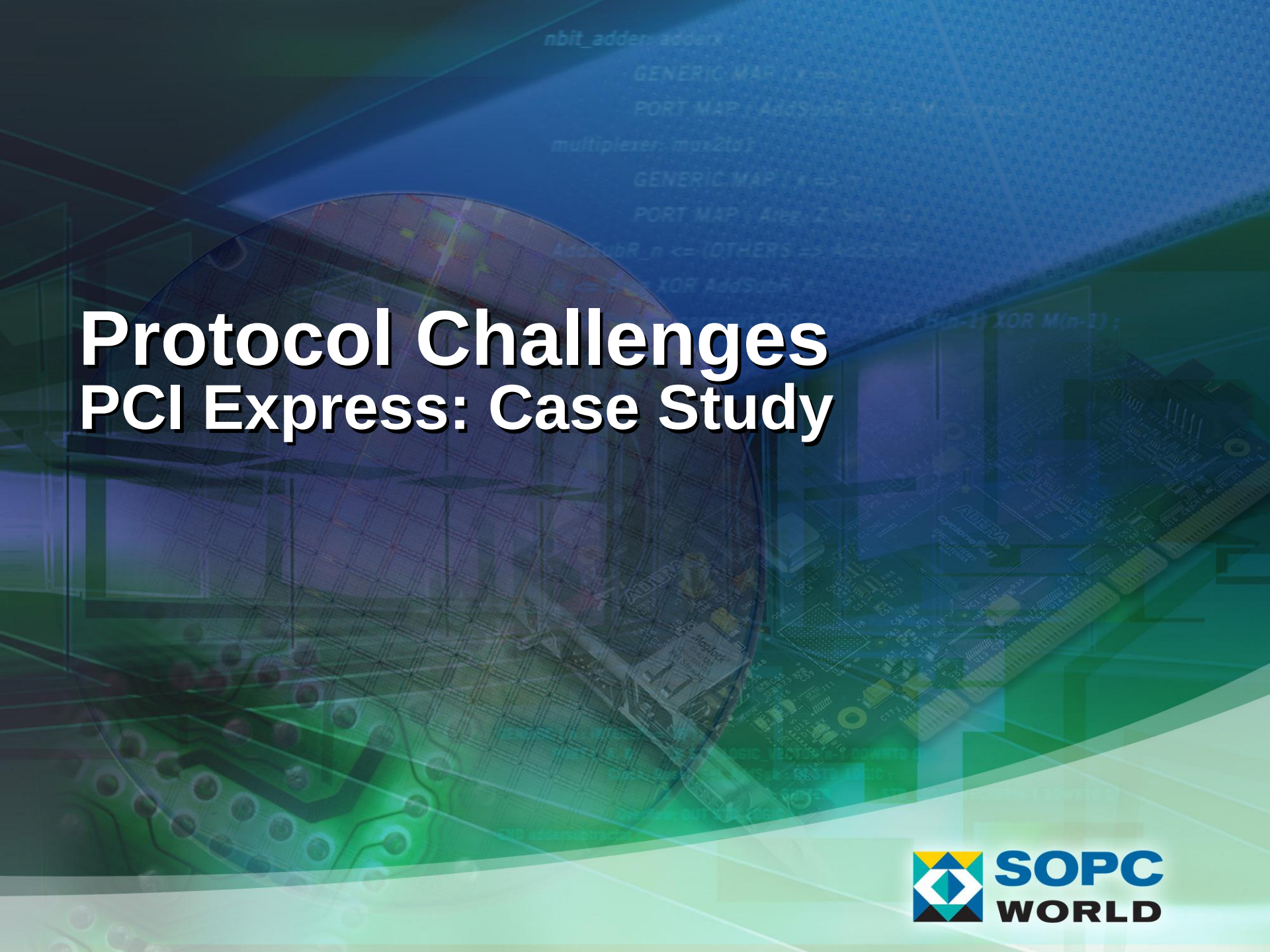
PCB Design

- Quartus II interface to PCB layout tools
  - Mentor Graphics
    - I/O Designer
    - DxDesigner
  - Cadence
    - Allegro PCB Librarian Part Developer
    - Allegro Design Entry HDL 610
    - Allegro Design Entry CIS 210 (OrCAD Capture)
- Board design guidelines
  - Application Note AN:

Protocol Challenges
PCI Express: Case Study



Protocol: Proprietary vs. Standard

- Standard protocol
  - Standard interface to DSP, Processors and external Busses now common
  - Simplified interface to 3rd party solutions
  - Access to low cost ASSP
    - Many low cost solutions with PCI Express
  - Reduction design effort for new users
  - Increasing ecosystem to support standard interfaces
- Proprietary protocol
  - Dramatically simplifies interface to legacy systems
  - Customized solution deliver lighter weight protocols
    - Exact requirements application
    - Reducing logic
    - Less protocol overheads in data flow

Benefits Standard Protocols Beginning to Outweigh Drawbacks

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Need Adaptable Hardware

- Protocol standards continue to advance in performance and function
  - Need for solution able to adapt as protocol evolve
- Protocol does not always provide exact fit to application
  - Need to provide protocol extensions in hardware
- Data rates rising doubling every few years
  - Need for solution capable of supporting multiple data rates
  - Need a solution to support next generation data rate to future proof application
- Hardware flexibility can increase application life
  - Ability to change protocol allows same hardware to be used in multiple applications, particularly in line card applications
  - Ability to bridge between protocols also advantageous

Consideration When Selecting Solution

- Need for robust protocol solution
  - Is the solution aligned to hardware resource?
    - Solution should integrate hard transceiver building blocks
    - Well designed Silicon can significantly aid protocol implementation
  - Does the solution provide seamless implementation?
    - IP must fit silicon without additional engineering effort (this effort should be handled by IP provider)
- Solution must meet protocol electrical standard
  - Is solution characterized against protocol?
  - Has device interoperated with other solution?
- Solution must meet system performance needs
  - Need proof of system validation?

Development cost and integration challenges reduce value of internal design

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PCI-Express

Case Study

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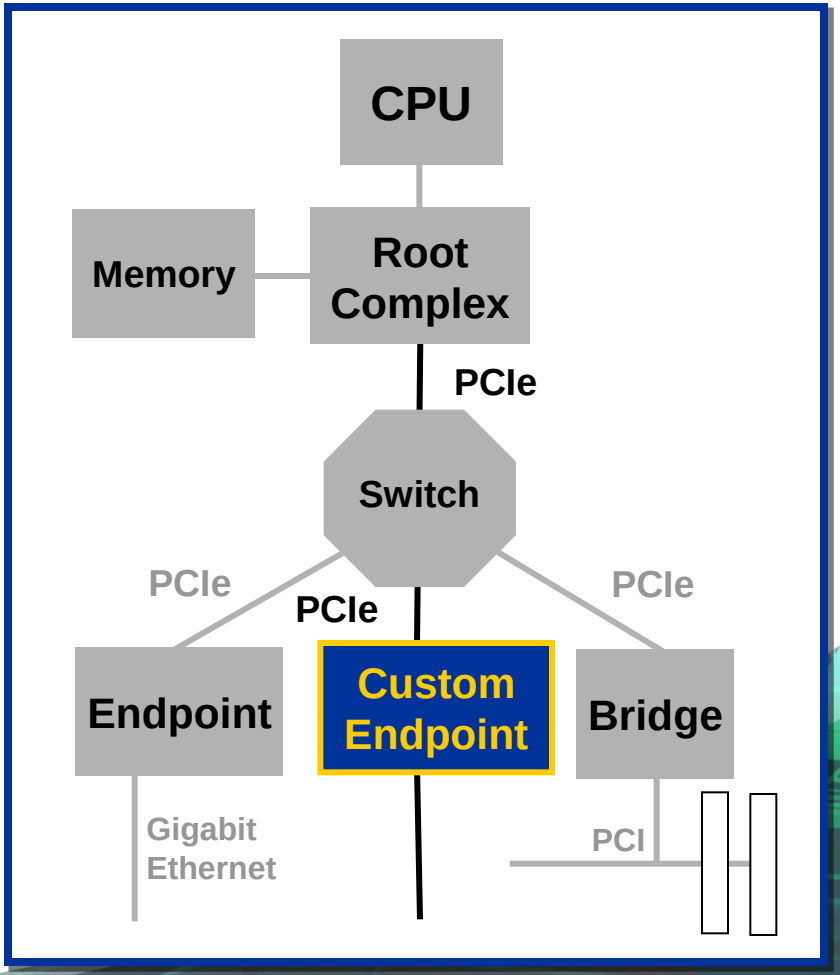
PCI Express Implementation Challenges

- Availability
  - Production silicon
  - Complete protocol stack
    - Proven transceivers
    - Protocol layer IP with right feature set
- Usability
  - Ability to accommodate evolving protocols
  - Ease of use
  - Development platforms
  - Reference designs
  - Performance
- Reliability
  - History and knowledge of transceiver design
  - Solution interoperability

Altera PCI Express Focus

Ensuring customer success by:

- Targeting endpoint applications
  - Switch, root complex, transparent bridging support using partner IP
- Complete product portfolio
  - Low cost/high-volume designs to high-performance FPGA/structured ASIC device families
- Providing complete PCI Express solutions
  - A solid commitment to hardware validation
  - With a focus on ease of use



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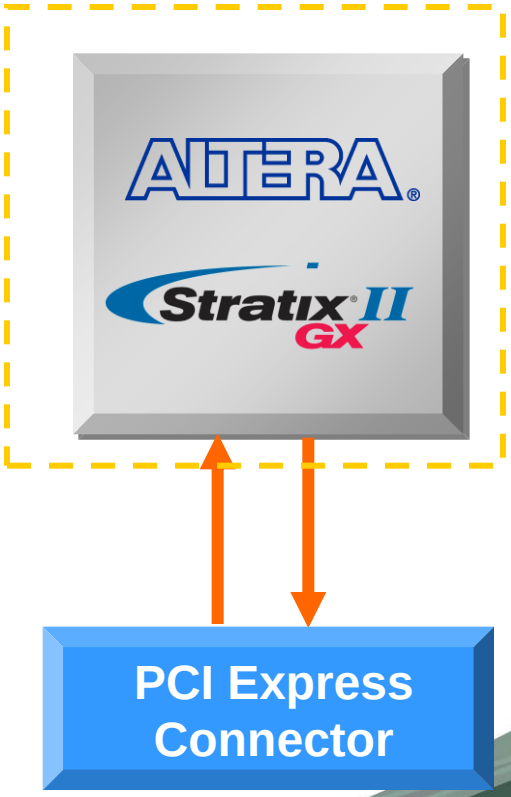
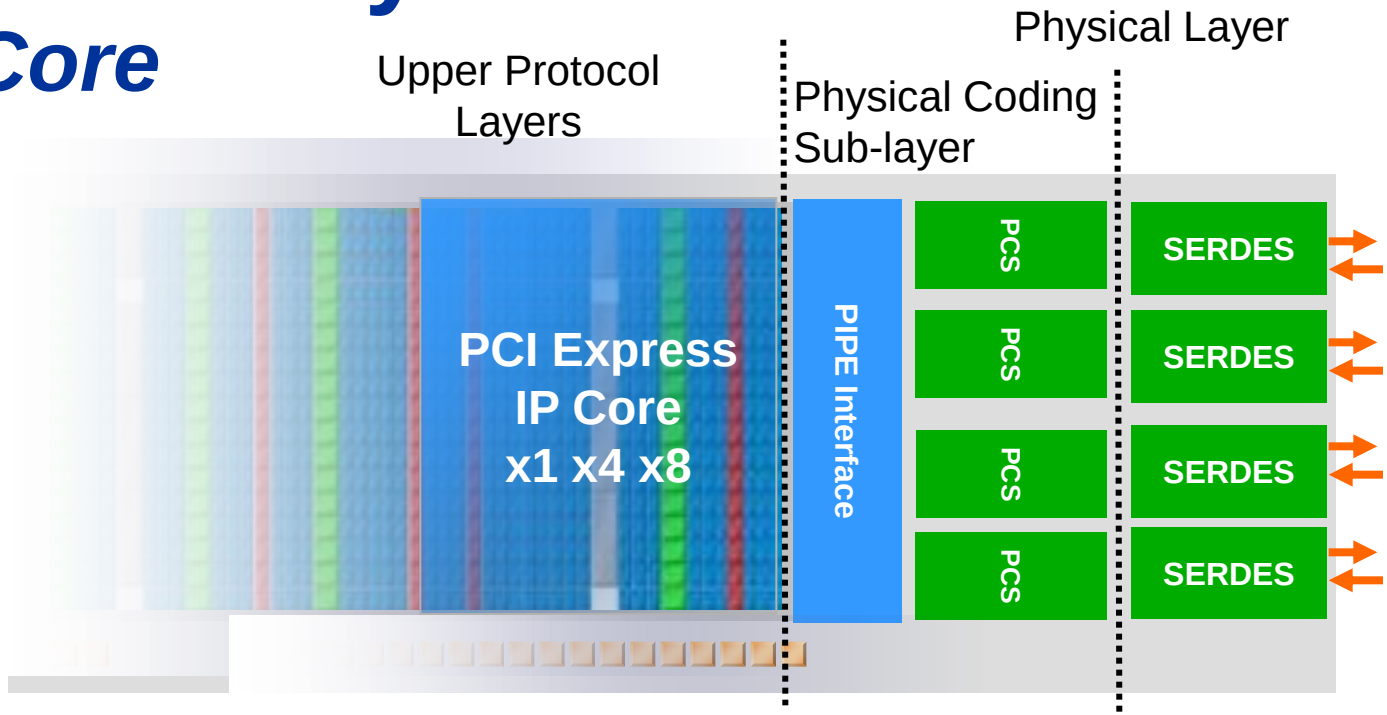
Availability
Silicon

- Stratix II GX FPGAs
  - Single device solution shipping today
  - PCI SIG-proven
  - Architected for PCI Express
    - Standard PIPE interface to IP core
    - Support for receiver detect



Availability

IP Core



- Support for up to 4 virtual channels (VCs)
- Configurable maximum payload up to 2 Kbytes
  - 128, 256, 512, 1024, or 2048 bytes
- Configurable retry buffer
- Optional end-to-end cyclical redundancy check (ECRC) generation/checking
- Optional advanced error reporting (AER)
- Flexible reference clock support (100, 125, or 156.25 MHz)

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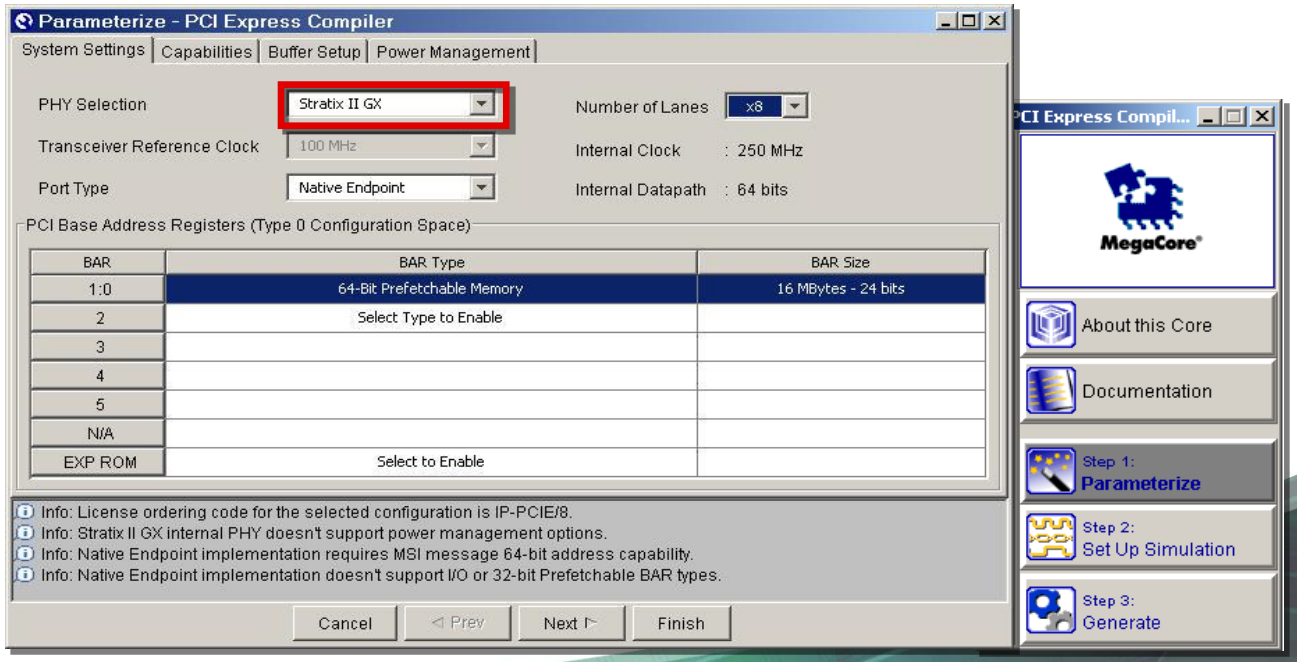
Usability
Ease of Use

- IP tool bench interface for easy configuration
  - Drop-down menu support for embedded Stratix II GX transceivers leading and other PHY vendors
- Support for OpenCore Plus for free evaluation



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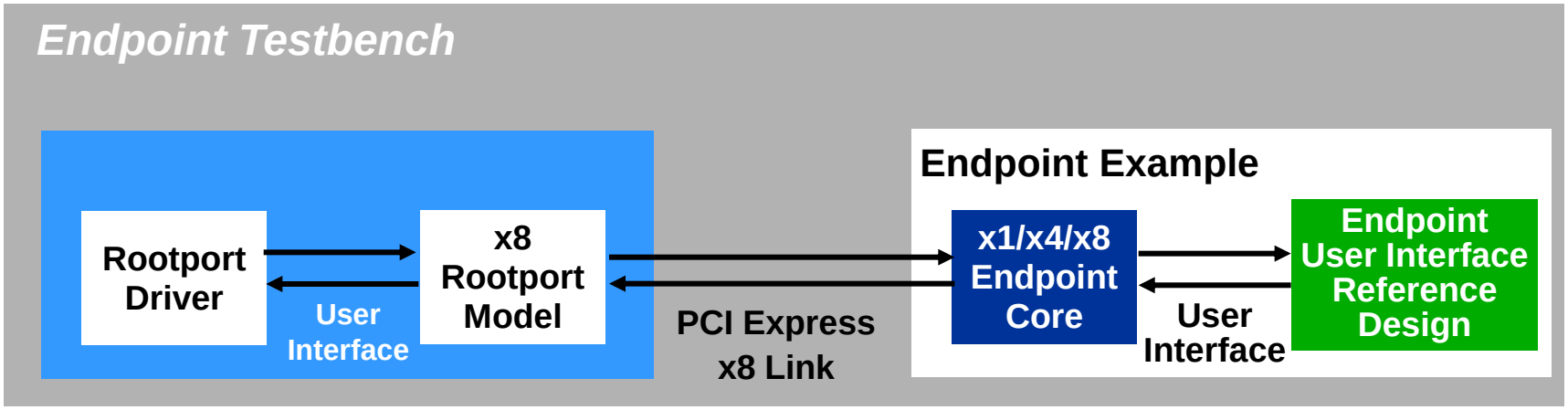
Usability
Ease of Use



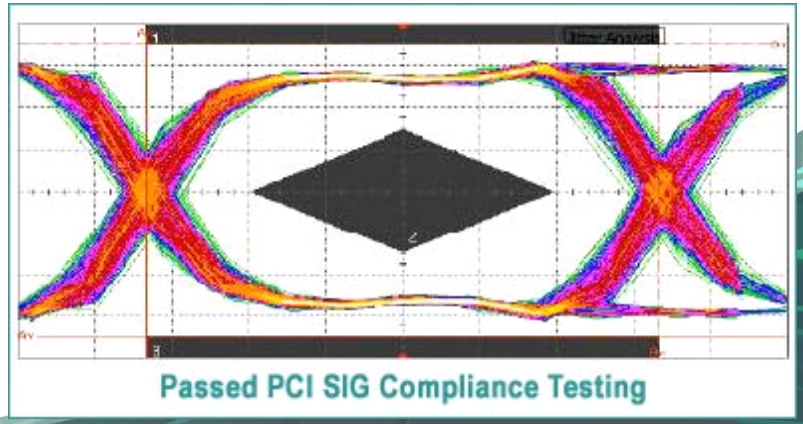
- Testbench generated with the core
  - Facilitate easy IP adoption into your design
  - Support for VHDL and Verilog
  - Instantiates the generated example design
  - Basic root port simulation model
    - Stimulus for generating transactions to the endpoint

Usability
Performance

- Simulation data shows > 80% of maximum throughput across all lane configurations
  - Finely tuned algorithms for data link layer packet transmission
    - Bandwidth maximization
    - Ensure non-starvation of the link
- High-performance reference design coming soon

Usability
Development Platforms

- Stratix II GX Development Kit
  - Complete PCI Express experience
    - PCI-SIG-compliant add-in card
    - PCI-SIG-compliant Stratix II GX EP2SGX90F1508C3 FPGA
    - PCI-SIG-compliant x1, x4, x8 IP core (OpenCore Plus)
    - 1-year Quartus II software license
    - Board schematics and layout information
    - Example design and supporting documentation
  - Modular and scalable design
  - System-level memory
    - DDR2 333-MHz components
    - QDRII 300-MHz components



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Usability
Reference Designs

- PCI Express-to-DDR2 Reference Design
  - Showcases Altera x8 IP core to external DDR2 memory running at 250 MHz
  - Supports:
    - Memory read/write from root complex
    - DMA read/write from Altera PCI Express IP core
  - Available now for download with complete documentation at
    www.altera.com/pciexpress

Reliability
Transceiver Design

- Three generations of transceiver-based products
- Strong understanding of PCI Express transceiver design
  - Stratix II GX passed PCI SIG compliance
  - Stratix GX passed PCI SIG compliance
- Extensive knowledge of serial protocols including Serial RIO, XAUI, GbE

Reliability
Breadth of Interoperability

- Partnered with Freescale to create and present joint working PCI Express solution
- Demonstrated Freescale PowerQUICC III-to-Altera Stratix II GX interoperation
- Verified working PCI Express interface for up to 8 lanes

Freescale	Altera
MPC8548E	Stratix II GX
MPC8547E	
MPC8545E	
MPC8543E	
MPC8641	
MPC8641D	
MPC8572E & Future MPC85xx Processors with PCI Express	

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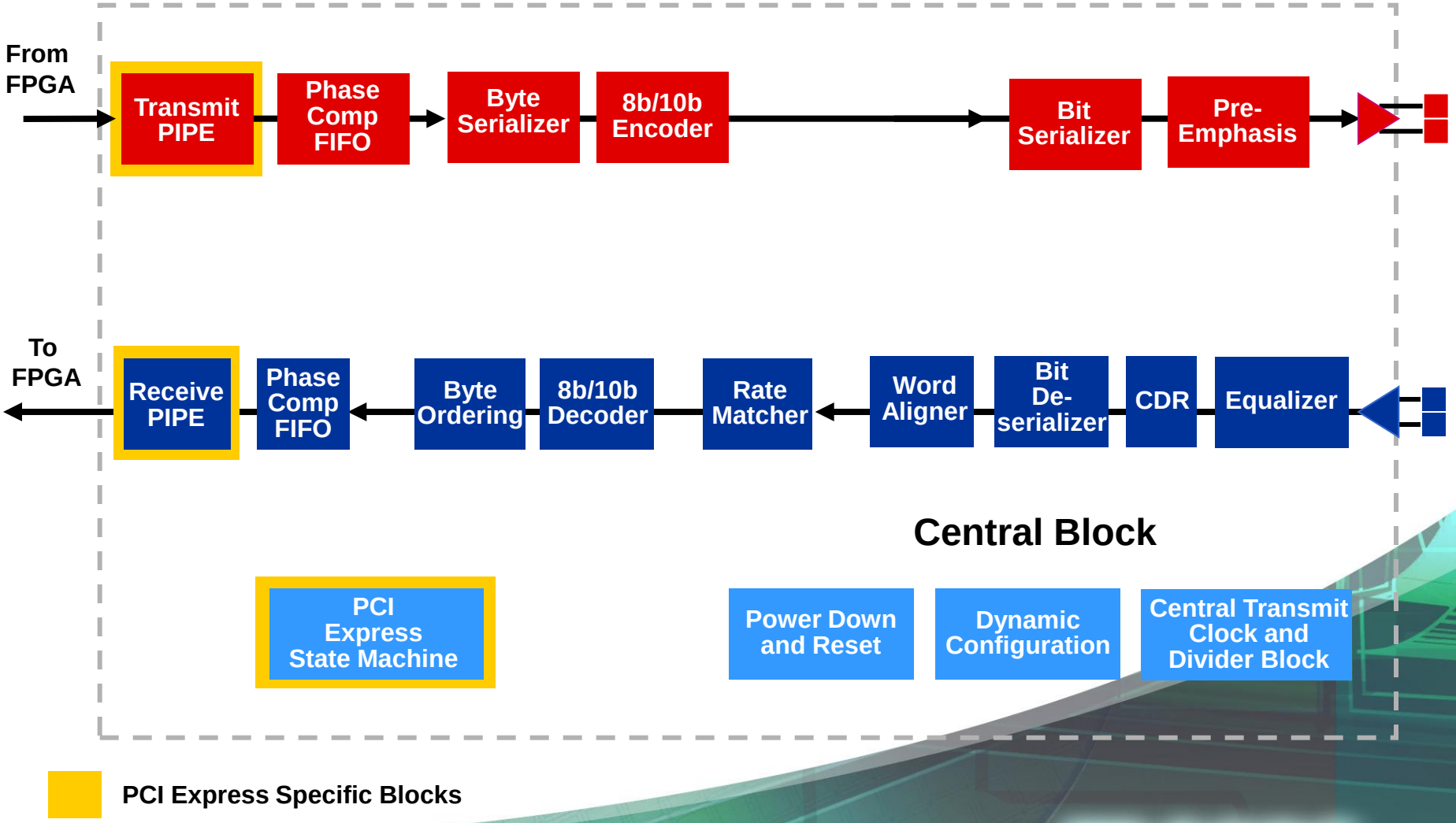
PCI Express Configuration (x1, x4, x8)



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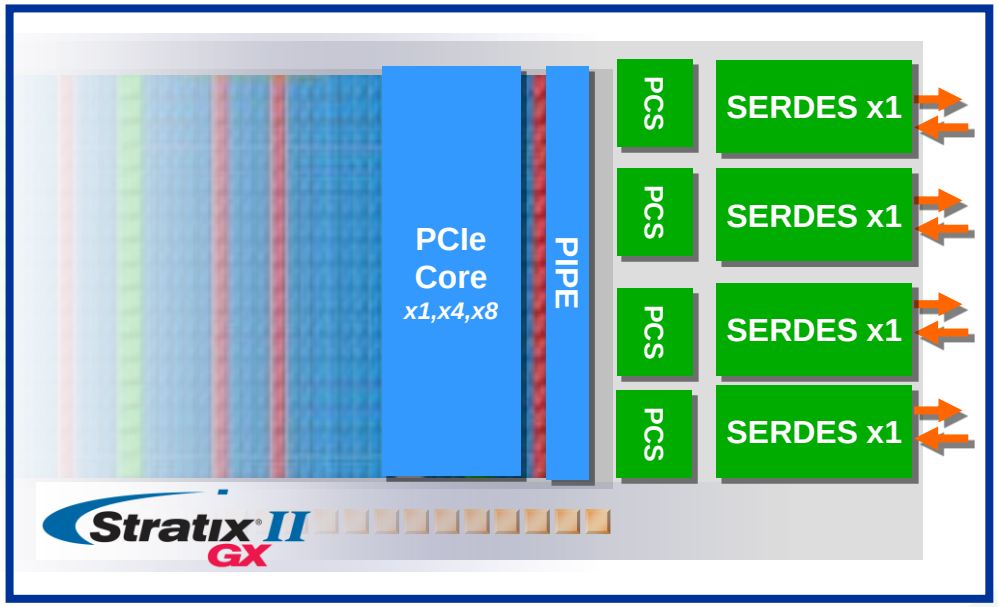
Complete Solution Example:

PCI SIG-Compliant PCI Express for x1, x4, x8

- **Hard IP**
  - --Auto negotiation
  - --State machine
- **Soft IP**
  - PCI Express MegaCore function
  - --FPGA fabric supports x8 interface at 250 MHz



Reference designs development kit

- PCI form factor
- Includes schematics and Gerber files

PCI SIG compliance / interoperability and characterization report

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Stratix II GX: PCI Express Development Board

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Stratix II GX Complete Protocol Solution

Standards	Data Rate	Complete Solution				
		Number of Channels in Link	IP	Reference Design	Development Platform	Characterization
PCI Express	2.5 Gbps	1, 4, 8				
CEI-6G	6.375 Gbps	1	N/A		SI	
SDH STM SONET OC-12	622 Mbps	1			SI	
SONET OC-48	2.488 Gbps	1				
Gigabit Ethernet	1.25 Gbps	1				
10 Gigabit Ethernet XAUI	3.125 Gbps	4			SI	
SD-SDI	270 Mbps	1				
HD-SDI	1.485 Gbps	1				
Serial RapidIO (SRIO) Standard	3.125 Gbps	1, 4				
SerialLite II	622 Mbps – 6.375 Gbps	1-256			SI	

SI: Use Stratix II GX Signal Integrity Development Kit

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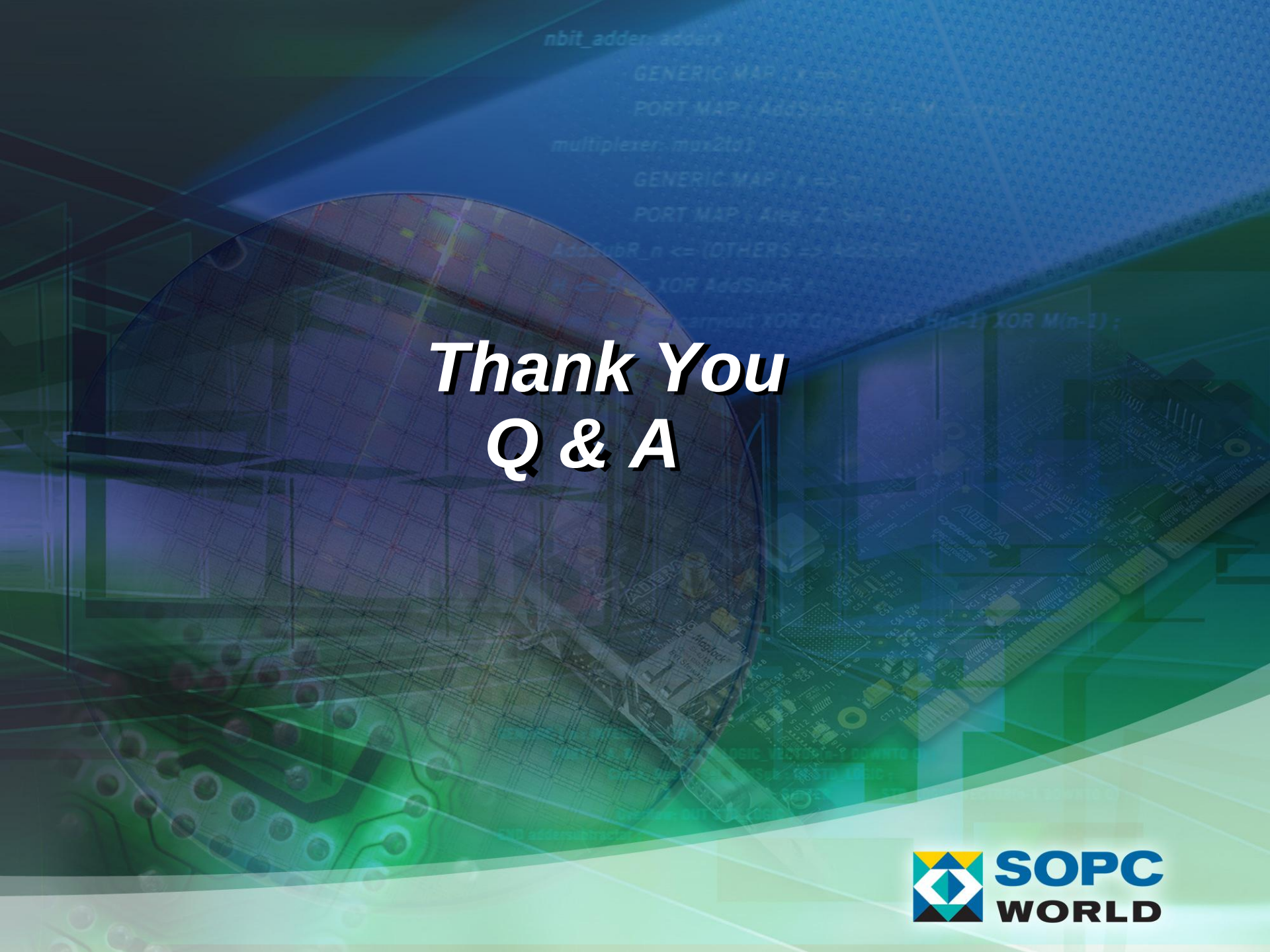
Conclusion

- Designing for High-Speed involves challenges in protocol implementation, signal integrity and board design
- Stratix II GX provides high-speed transceivers with superior signal quality
- Leading-edge design tools from Altera simplify high-speed design


Thank You
Q & A
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