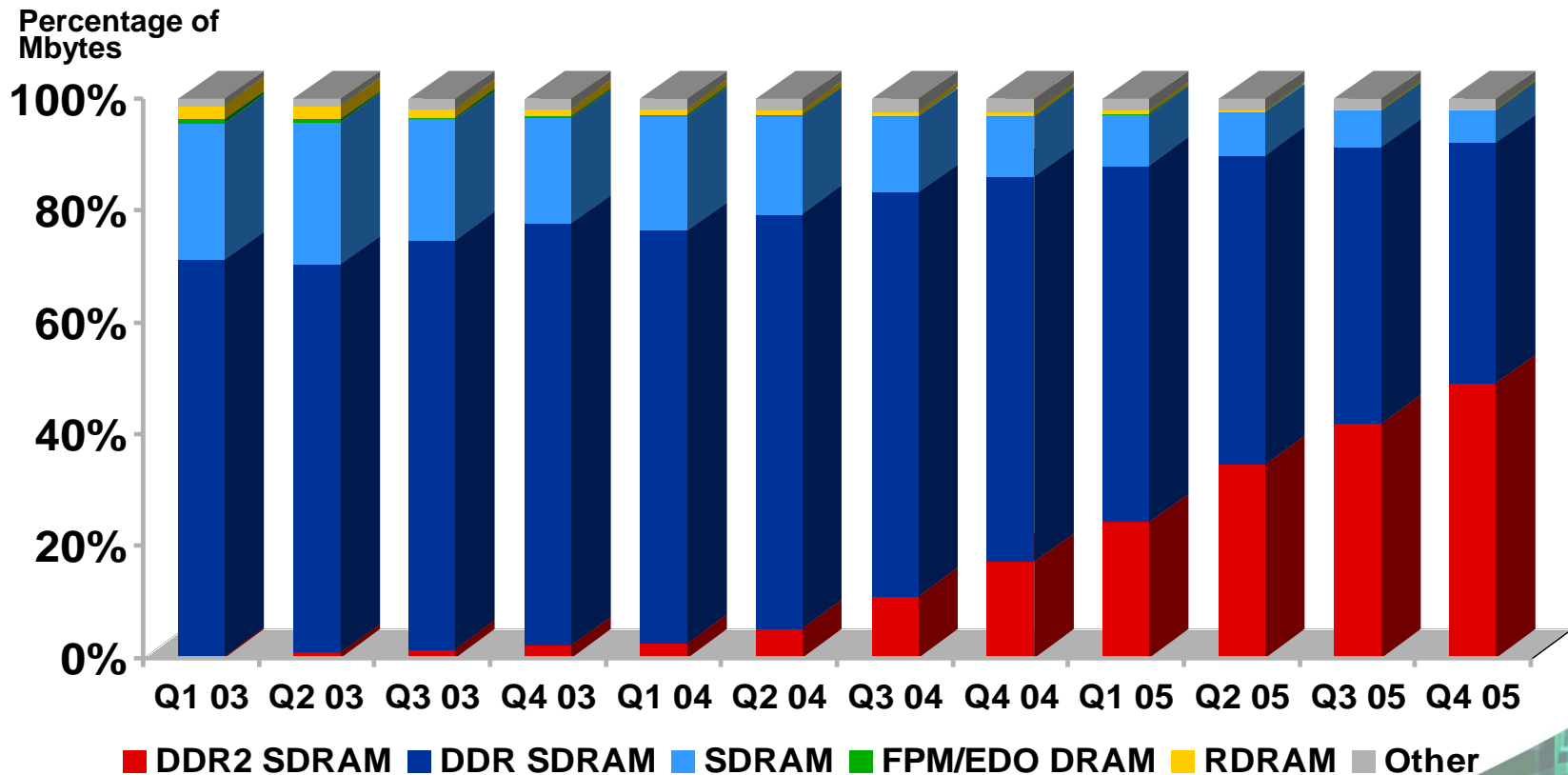# Understand and Design for High-Speed Memory Interfaces

Agenda

- Introduction
- Design challenges
- Overcoming design challenges
- Conclusion
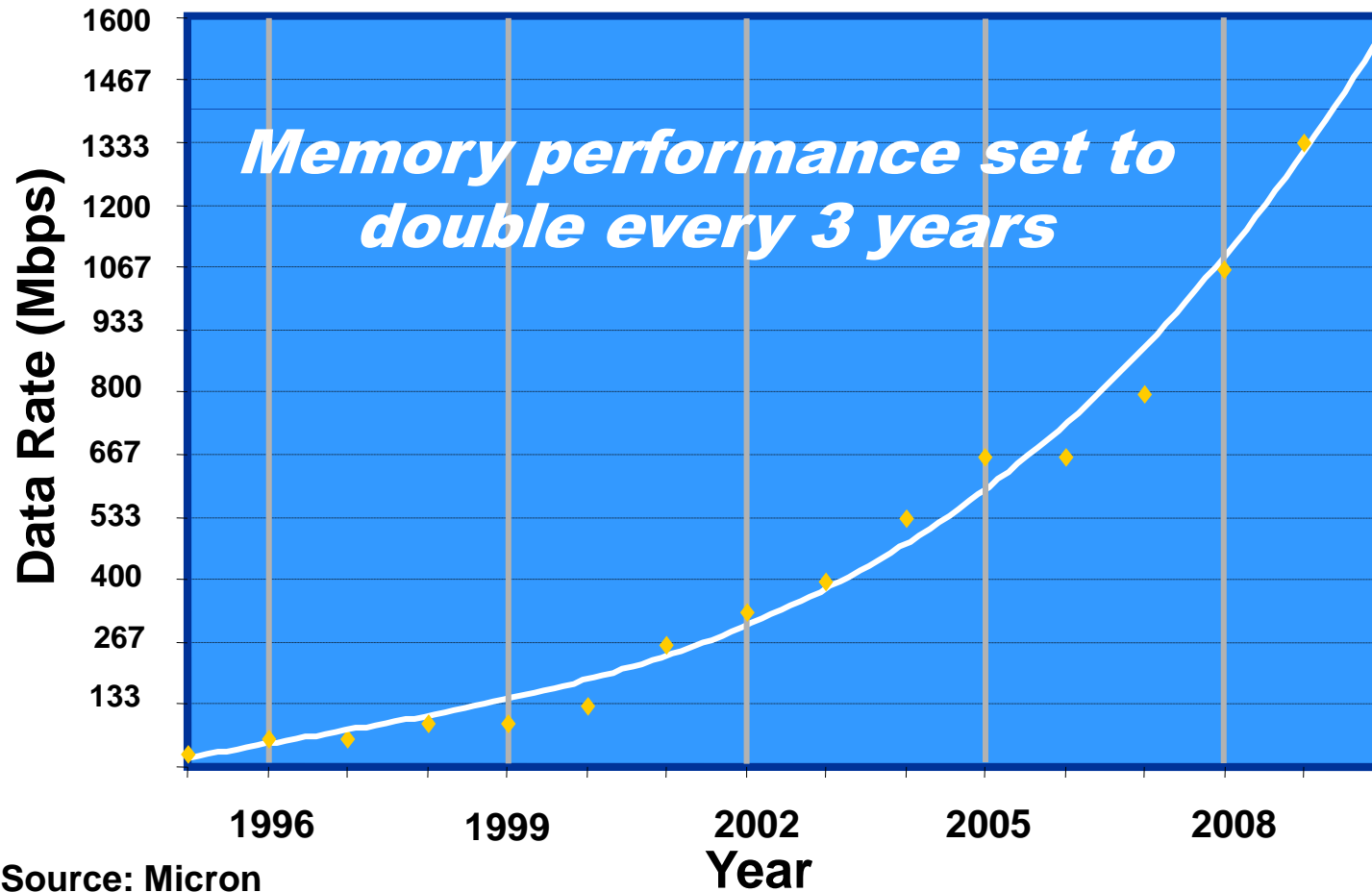
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DRAM Quarterly Supply Trend

Percentage of Mbytes

Chart legend: ■ DDR2 SDRAM ■ DDR SDRAM ■ SDRAM ■ FPM/EDO DRAM ■ RDRAM ■ Other

X-axis: Q1 03, Q2 03, Q3 03, Q4 03, Q1 04, Q2 04, Q3 04, Q4 04, Q1 05, Q2 05, Q3 05, Q4 05

More Than 90% of the Designs Use Double Data Rate (DDR) or DDR2 SDRAM

Source: Gartner Dataquest

3

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Mainstream Memory Trends

Memory performance set to double every 3 years

Data Rate (Mbps): 133, 267, 400, 533, 667, 800, 933, 1067, 1200, 1333, 1467, 1600

Year: 1996, 1999, 2002, 2005, 2008

Source: Micron

4

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Memory System Design:
No Longer Separate Tasks

Year 1995:
66 MHz, 66 Mbps
Single Data Rate

Memory Controller Design

I/O Interface Design

Board Design

Year 2006:
267 MHz, 533 Mbps
Double Data Rate (DDR)
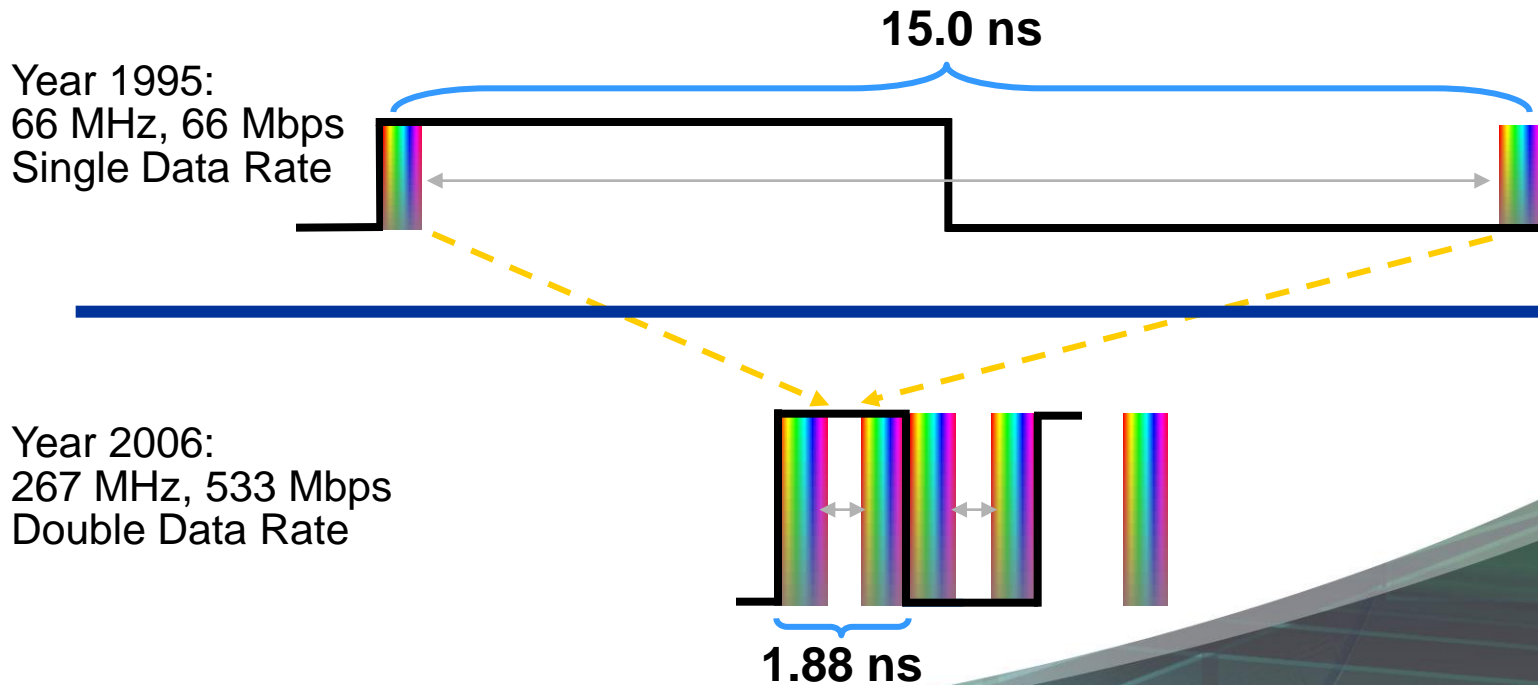
Memory Controller Design

I/O Interface Design

Board Design

A Complete Memory Interface Solution Enables Success

5

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Why a Dynamic System?

- Memory & board uncertainties do not scale with frequency
- Effects designers could once ignore are now significant proportions of the cycle

15.0 ns

Year 1995:
66 MHz, 66 Mbps
Single Data Rate

Year 2006:
267 MHz, 533 Mbps
Double Data Rate

1.88 ns

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Design Challenges

DDR2-533 Interface Design Challenges
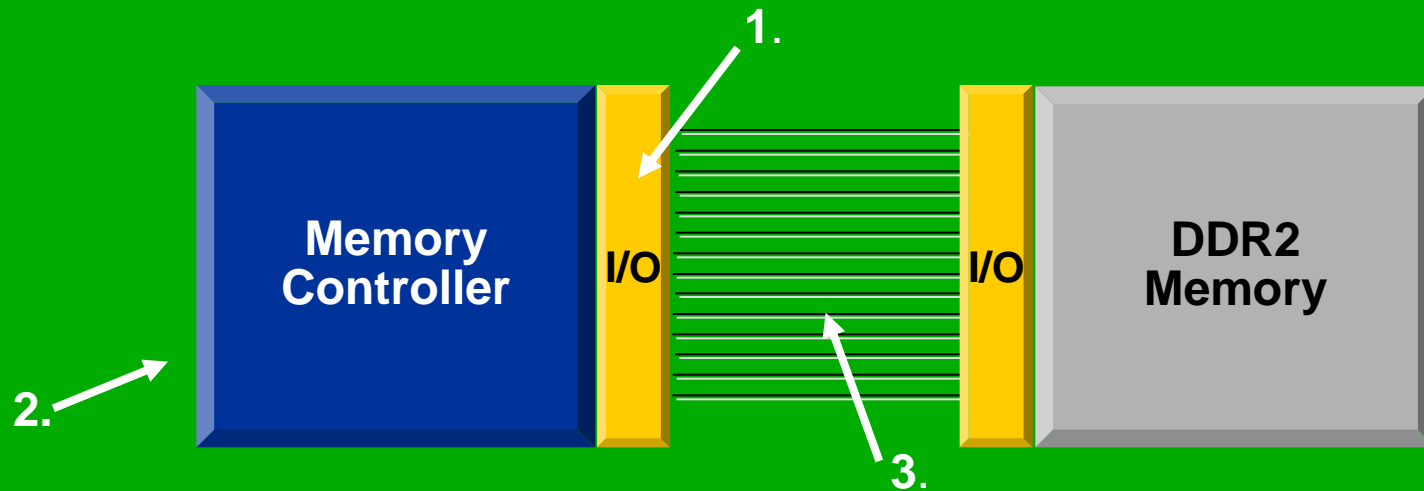
1. I/O interface challenges
2. Controller design challenges
3. Board design challenges

Printed Circuit Board

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DDR2-533 Interface Design Challenges

Challenges	Details
I/O interface	1. Maintaining DQ – DQS phase relationship 2. Analyzing timing margin and meeting time requirements at the controller and memory I/Os
Controller design	1. Designing memory controllers 2. Verifying functionality 3. Managing clock domains
Board level	1. Maintaining signal integrity 2. Managing skew between signals

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I/O Interface Challenge #1: DQ-DQS Phase Relationship
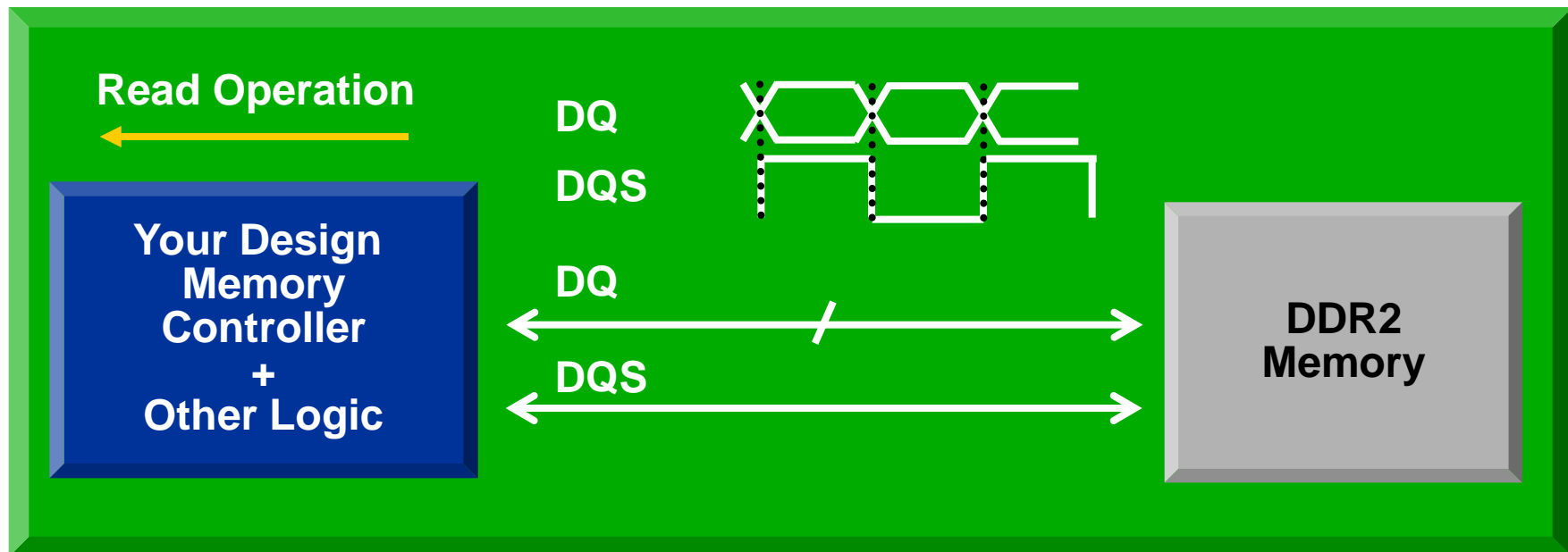
- **Write Operation**
  - DQ and DQS to the memory are 90° apart
  - Memory can easily capture write data
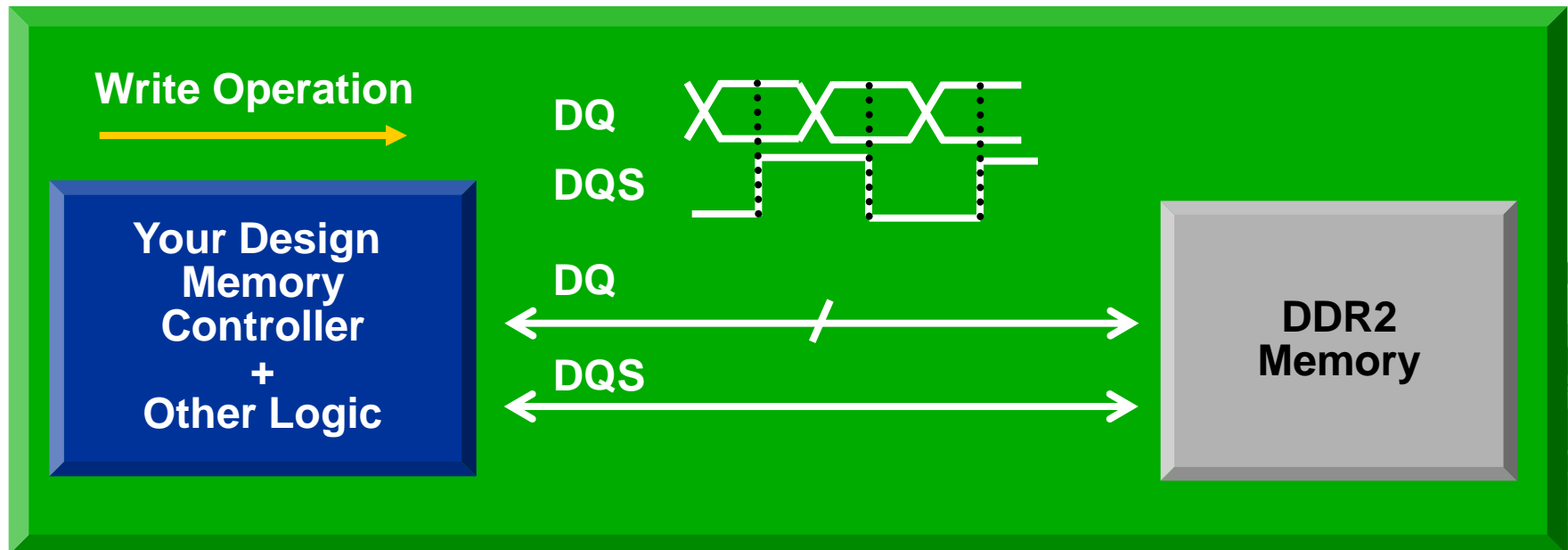
I/O Interface Challenge #1: DQ-DQS Phase Relationship

- **Read Operation**
  - DQ and DQS signals from the memory are edge aligned
  - DQS needs to be realigned to the center of data valid window

I/O Interface Challenge #1: DQ-DQS Phase Relationship

■ Traditional techniques to realign DQS for read operation

Phase Shift Technique	Issues
90^0 trace skew between DQ and DQS signals	■ DQS signal is 6 inches longer than DQ signals* ■ Complicated board design
Add fixed delay element to the DQS signal path on board	■ Susceptible to process, voltage, and temperature (PVT) variations
Use on-chip delay elements	■ Not suitable for high-performance applications ■ Susceptible to PVT variations

* Calculation is based on approximate delay of 160 ps/inch for an FR4 laminate microstrip with a 50-Ω characteristic impedance at 533 Mbps data rate.
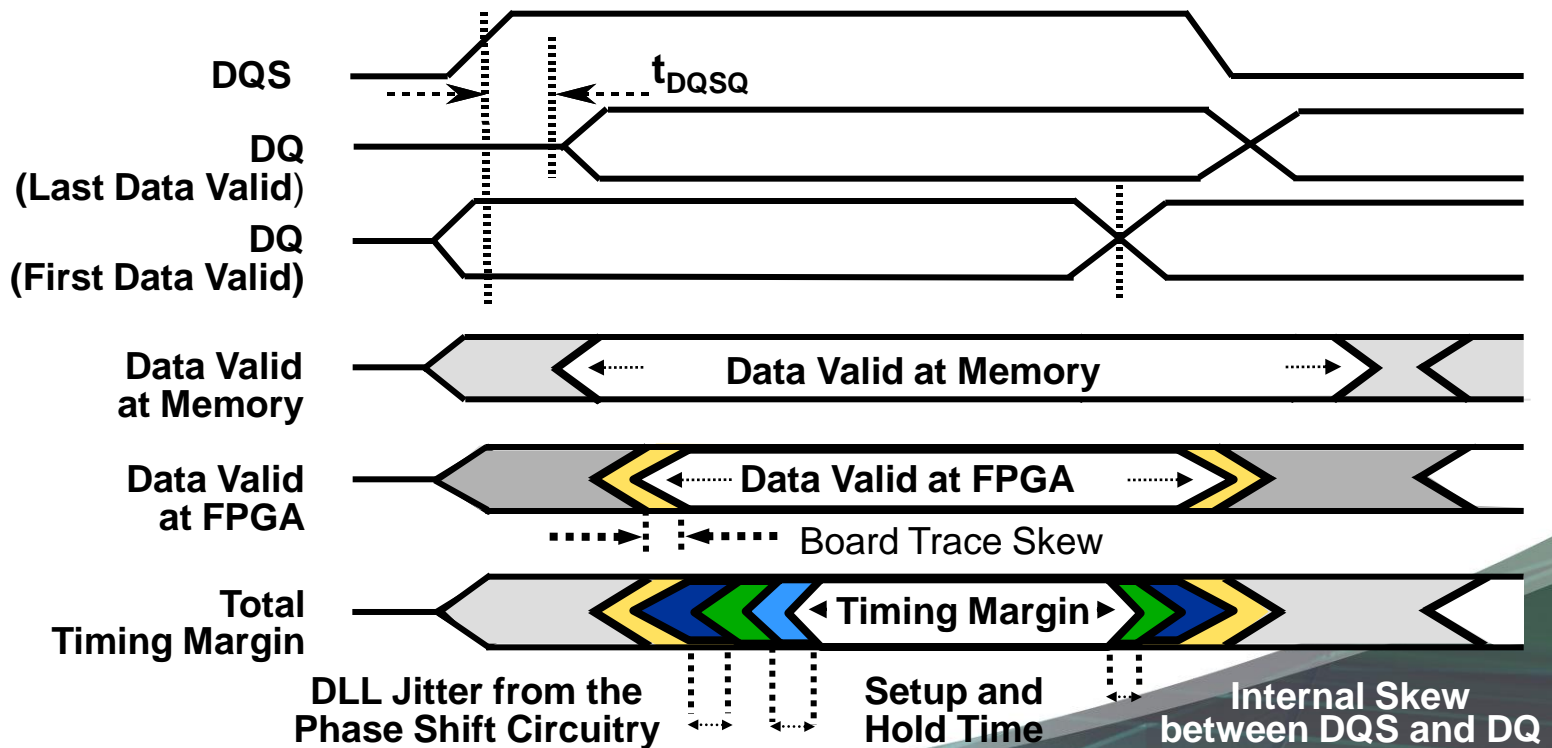
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I/O Interface Challenge #2: Timing Margin Analysis

■ Parameters that affect timing margin
  - Skew between first data valid and last data valid
  - Board trace skew
  - DLL jitter for DQS phase shift circuitry
  - Internal skew between DQS and DQ
  - Setup and hold time

I/O Interface Challenge #2: Timing Margin Analysis

- Timing margin = data valid window at memory - 2 x (board trace skew + DLL jitter + internal DQ and DQS skew) - setup and hold time
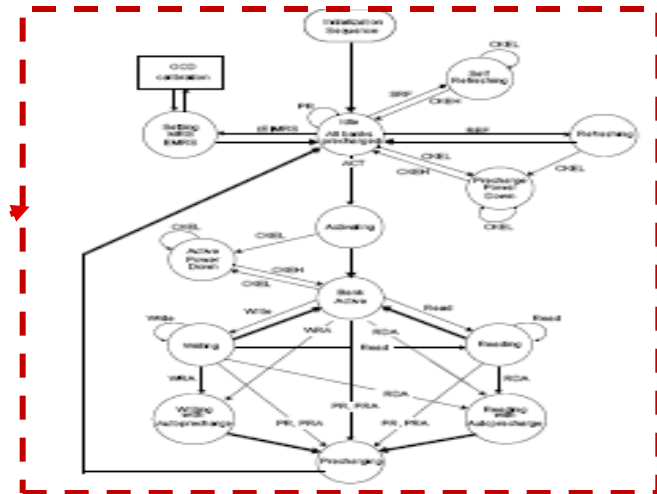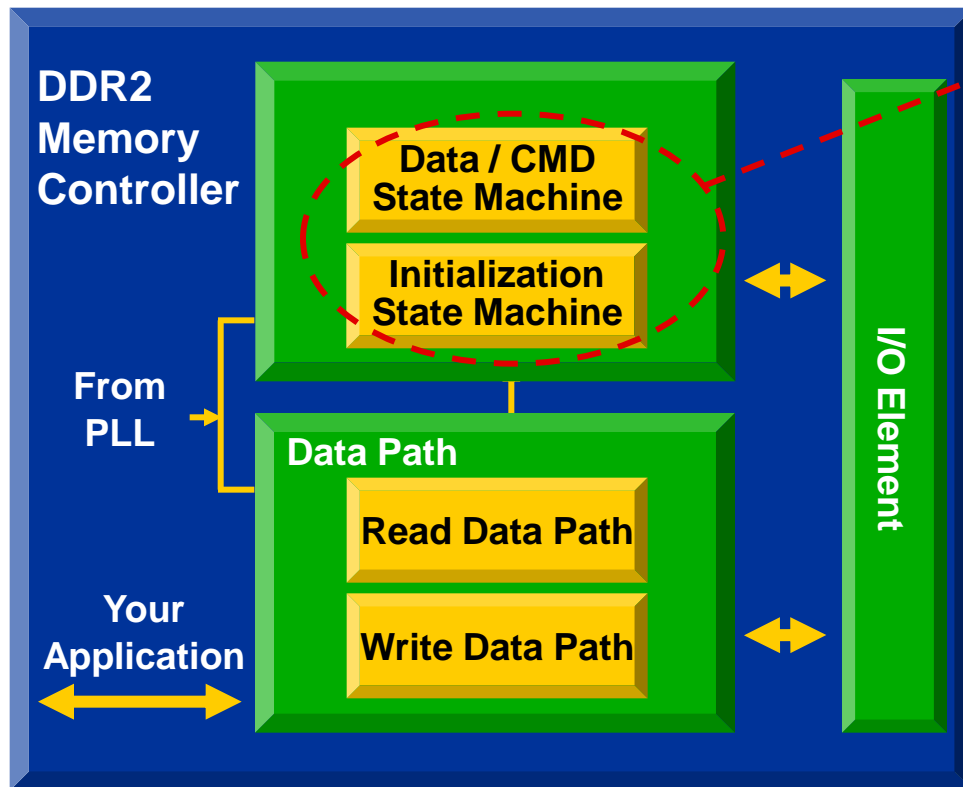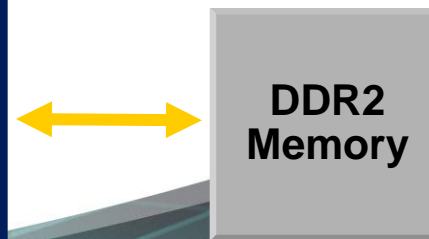
DDR2-533 Interface Design Challenges

Challenges	Details
I/O interface	1. Maintaining DQ – DQS phase relationship 2. Analyzing timing margin and meeting time requirements at the controller and memory I/Os
Controller design	1. Designing memory controllers 2. Verifying functionality 3. Managing clock domains
Board level	1. Maintaining signal integrity 2. Managing skew between signals

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Controller Design Challenge #1: Designing Memory Controller

- **DDR2 memory controller block diagram**

Source: Samsung. Simplified state diagram for illustration only.

DDR2 Memory Controller

- Data / CMD State Machine
- Initialization State Machine

From PLL

Data Path
- Read Data Path
- Write Data Path

Your Application
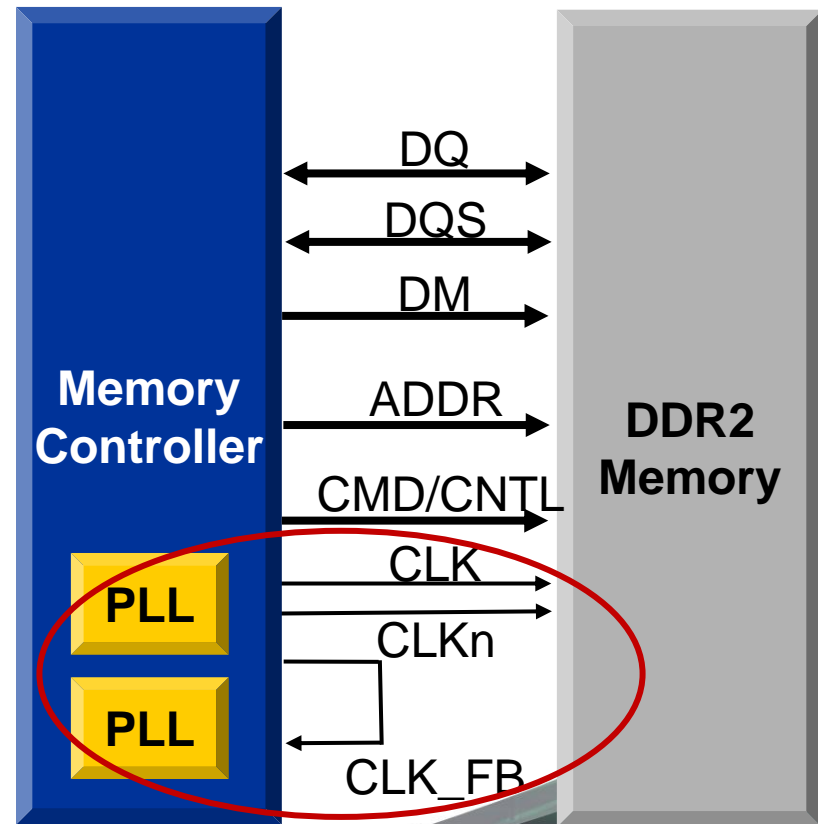
I/O Element

DDR2 Memory

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Controller Design Challenge #2: Verify Controller Functionality

- **Three major components in testbenches**
  - Memory controller instance (unit under rest)
  - Test drivers
  - Memory models

Testbench

Example Instance

Pnf (Pass not Fail)

Test_Complete

Test Drivers

DDR 2 SDRAM Controller

DDR2 SDRAM Model

Ref_CLK

PLL

Bidirectional Board Delay Model

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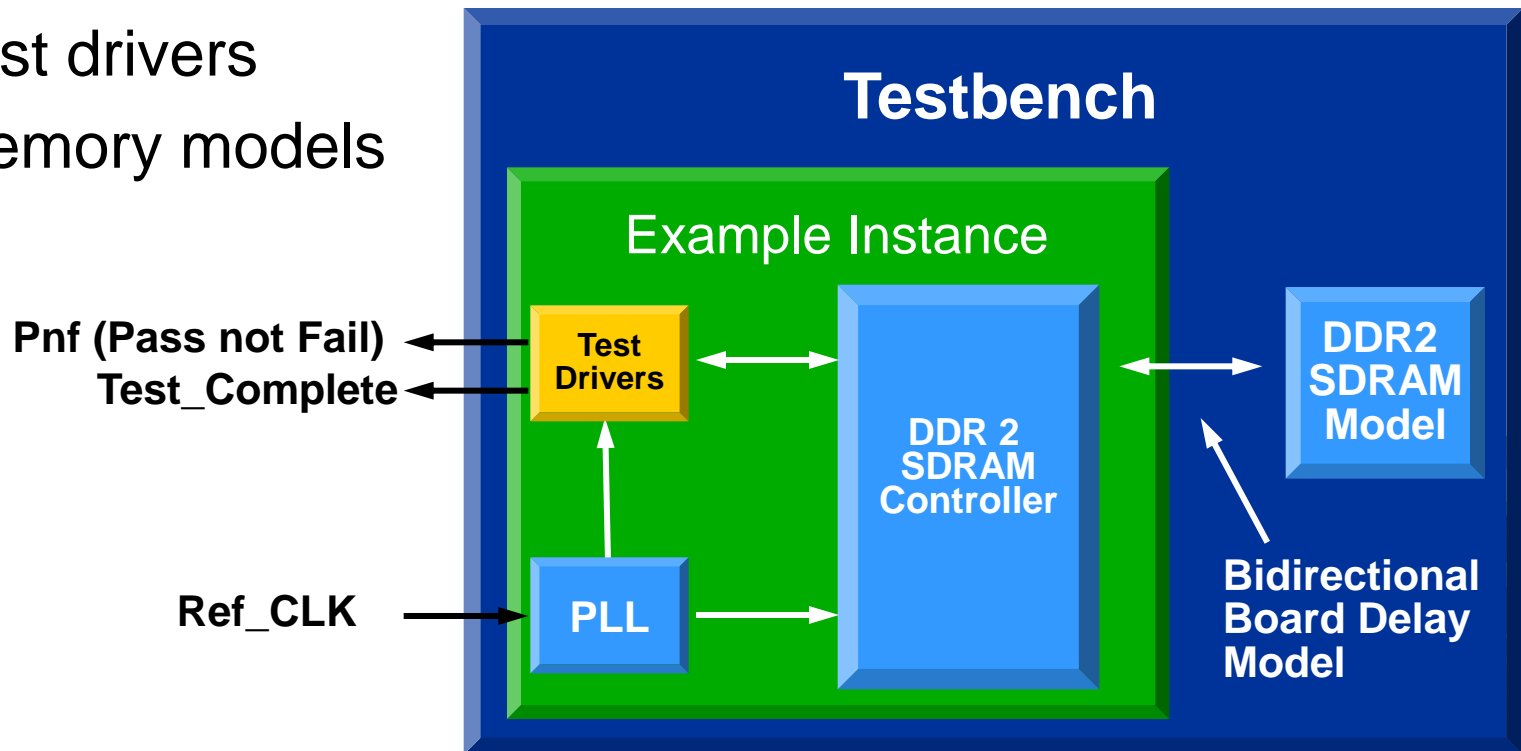
Controller Design Challenge #3: Clock Management

- **Resynchronization using clock feedback is essential for high-speed interface**
  - Compensate PVT variations for I/Os
  - Achieve high-speed data rate (400 Mbps and above)

Memory Controller

PLL

PLL

DQ

DQS

DM

ADDR

CMD/CNTL

CLK

CLKn

CLK_FB

DDR2 Memory

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DDR2-533 Interface Design Challenges

Challenges	Details
I/O interface	1. Maintaining DQ – DQS phase relationship 2. Analyzing timing margin and meeting time requirements at the controller and memory I/Os
Controller design	1. Designing memory controllers 2. Verifying functionality 3. Managing clock domains
Board level	1. Maintaining signal integrity 2. Managing skew between signals

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Board-Level Challenges

■ Maintaining signal integrity

– Selecting right termination scheme

– Minimizing noise and signal crosstalk

– Minimizing signal attenuation

■ Managing skew between signals

– Making signal traces equal length

Factors Affecting Signal Integrity

Design Item	Effect on Performance/Reliability of the System
Data width	Increasing data width increases simultaneously switching output (SSO) noise and increases board design complexity
Noise	Causes bit errors, affects signal integrity, and degrades performance and reliability
Loading	Increasing number of devices or modules will reduce performance
I/O performance	Drive strength affects quality of signals and maximum clock rate
Termination scheme	Termination scheme and resistor values affect signal quality and performance

Board Simulations Should Be Performed to Check for Signal Integrity

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Data Valid Window Shifts

Data valid window shifts with PVT variations

Data Valid Window A

Data Valid Window B
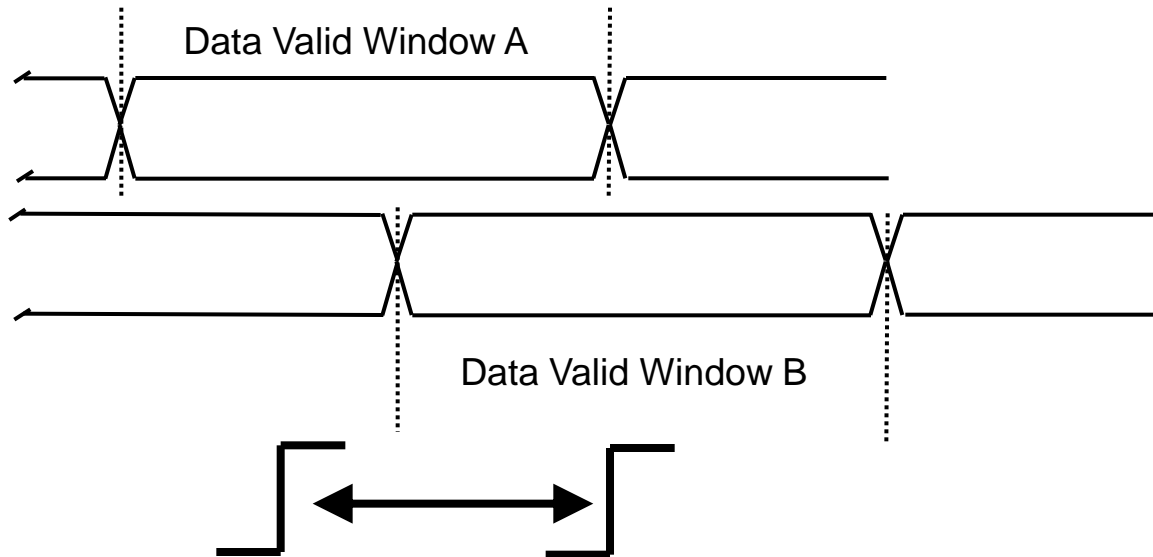
Optimum resynchronization clock position shifts

Overcoming Design Challenges
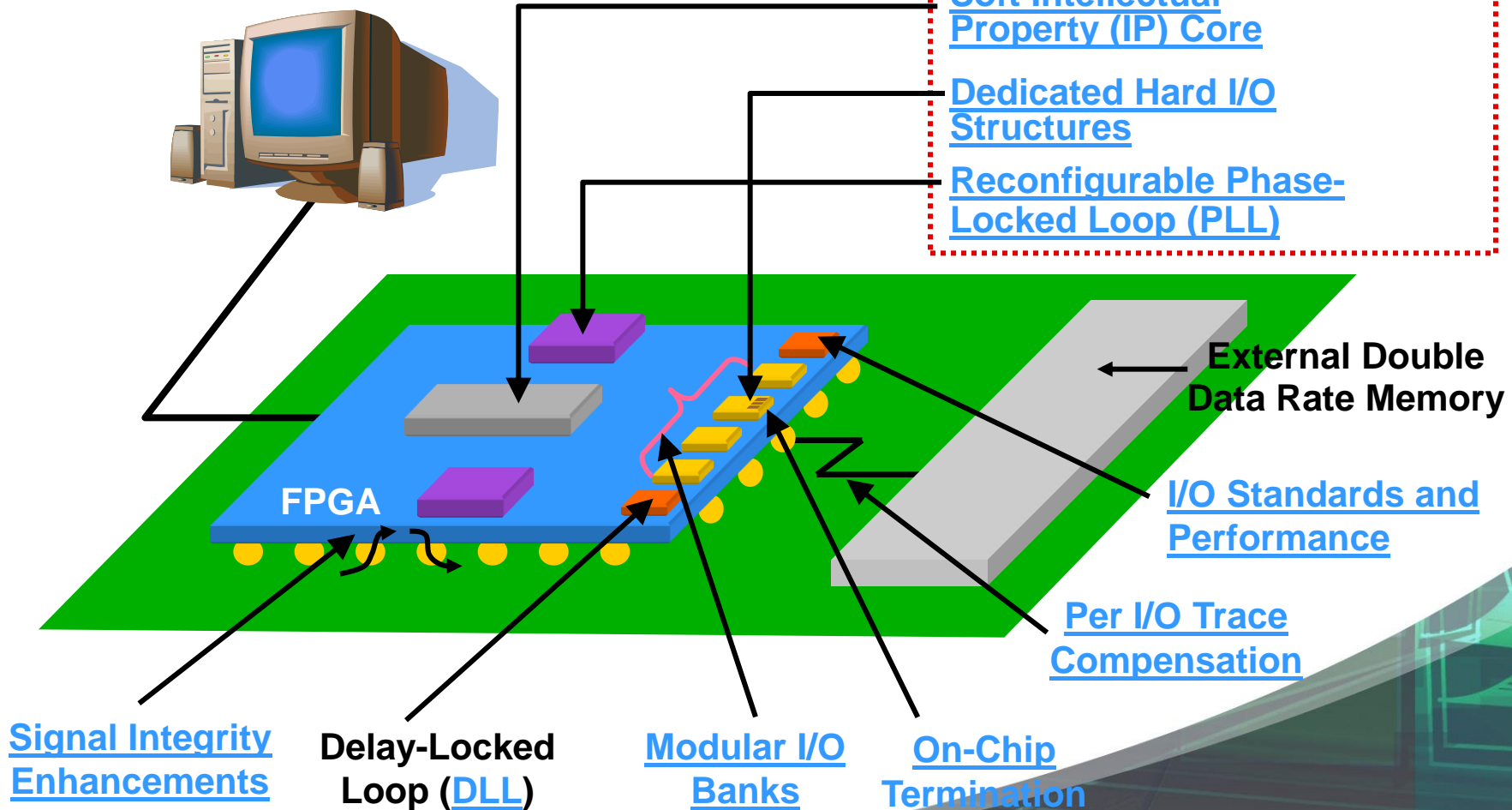
Tool Support

TimeQuest – Timing Analyzer

Signal Integrity Analyzer

Automatic Self-Calibrating Integrated System

Soft Intellectual Property (IP) Core

Dedicated Hard I/O Structures

Reconfigurable Phase-Locked Loop (PLL)

External Double Data Rate Memory

I/O Standards and Performance

Per I/O Trace Compensation

FPGA

Signal Integrity Enhancements

Delay-Locked Loop (DLL)

Modular I/O Banks

On-Chip Termination

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FPGA I/O Capabilities

External memory interfaces support on all I/O banks

Interconnect	Device Family	
	Stratix® III	Stratix II
	Performance*	Performance
DDR III	400 MHz	N/A
DDR II	400 MHz	333 MHz
DDR	200 MHz	200 MHz
QDR II	350 MHz	300 MHz
QDR II+	400 MHz	N/A
RLDRAM II	400 MHz	300 MHz

Memory Interface Standard	I/O Standard
DDR III	1.5-V SSTL-1.5
DDR II	1.8-V SSTL-1.8
DDR	2.5-V SSTL-2
QDR II	1.8-V HSTL
QDR II+	1.5-V HSTL
RLDRAM II	1.8-V HSTL

*Stratix III left and right banks support 300-MHz DDR rates.

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# Specialized I/O Structures

- Dedicated hard I/O structures
  - Characterized over process, voltage, and temperature (PVT)
- DDR support on all I/O
  - Flexibility in positioning interface
 - Predefined DQS locations
- Built-in capability
  - On-chip termination
    - Parallel, serial, and dynamic on-chip termination (OCT)
  - Trace compensation
    - Compensate for board mismatch
    - Deliberately skew DQ data output to reduce simultaneous switch noise (SSN)
  - Read write leveling capability
    - Compensates for DDR3 (JEDEC) fly-by topology used for clock signals, which causes skew between clock and DQS across DIMM
  - Half- and full-rate registered outputs
    - Run at 2x lower frequency and 4x wider data bus than memory interface
- 4-, 8-, 9-, 16-, 18-, 32-, or 36-bit programmable DQ group widths

DQ Hard I/O   1:2 Demux   Sync Block   Read   Write

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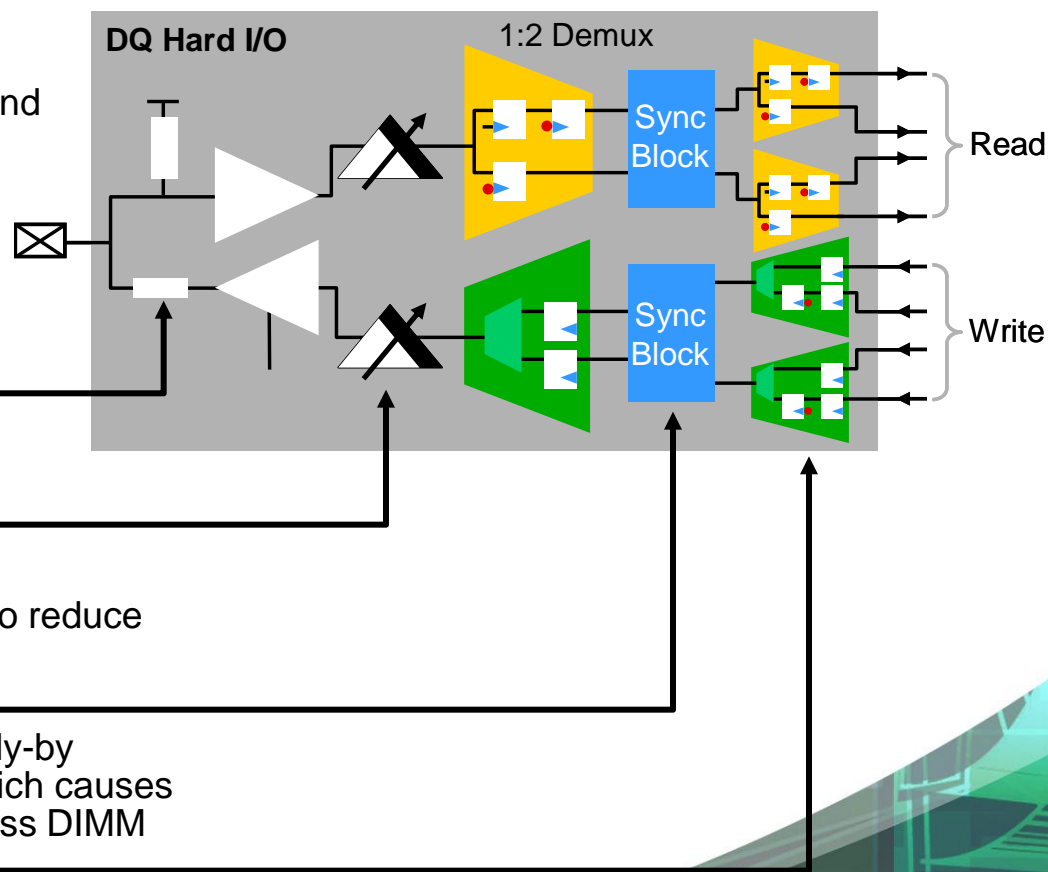
Meeting Timing Margins

- Used to maintain best setup and hold margins
    - Voltage and temperature variations cause data valid window to shift
    - Shifting resynchronization clock edge by same amount maintains best setup and hold margins
    - Free soft IP core monitors voltage and temperature variations and automatically adjusts resynchronization clock phase

- One PLL drives all clock signals required for interface
    - Stratix III PLLs have 7 to 10 outputs
    - DDR uses 3 to 7 clocks; QDR uses 4 to 5 clocks
    - Only 1 PLL required per interface
        - 2 required for >200 MHz in Stratix II devices

- No interruption of external memory interface operation when PLL reconfigured

**Data valid window shifts with PVT variations**

Data Valid Window A

Data Valid Window B
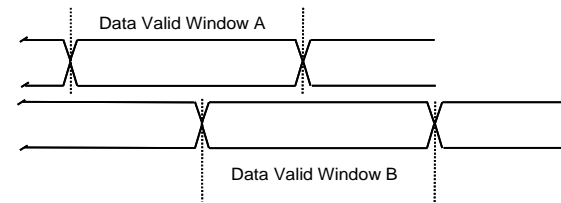
Optimum resynchronisation clock position shifts
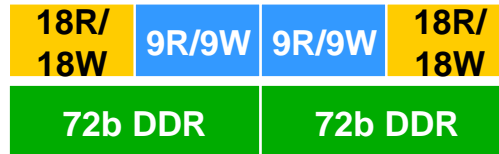
SOPC WORLD
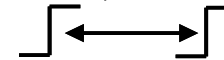
Maintaining Phase Shift Relations

■ DLL dynamically adjusts DQS delay chain to maintain phase shift over PVT

■ 4 DLLs

– Each has 2 independent outputs

– Each I/O bank can access 2 DLLs

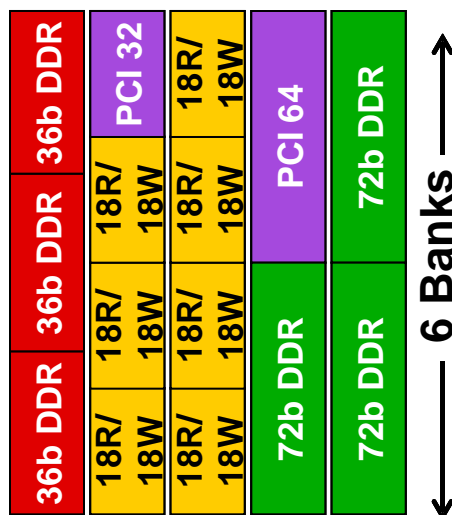– Allows external memory interfaces with different frequencies and phase shifts to coexist on same side
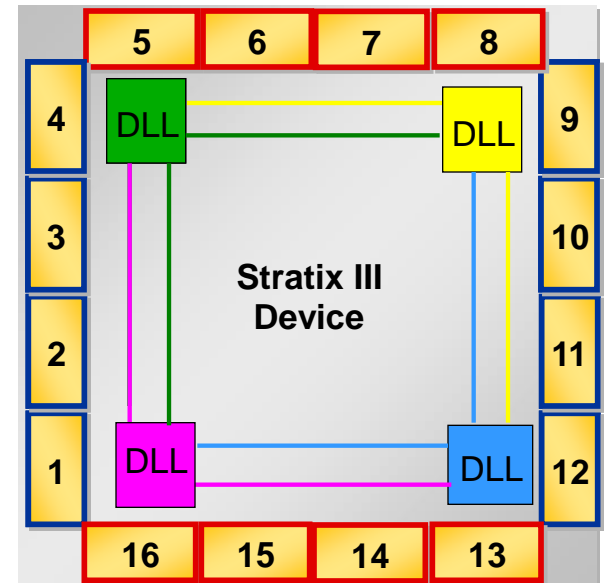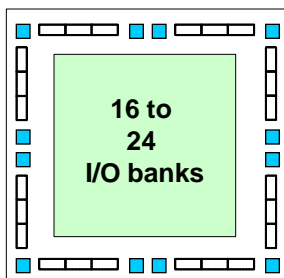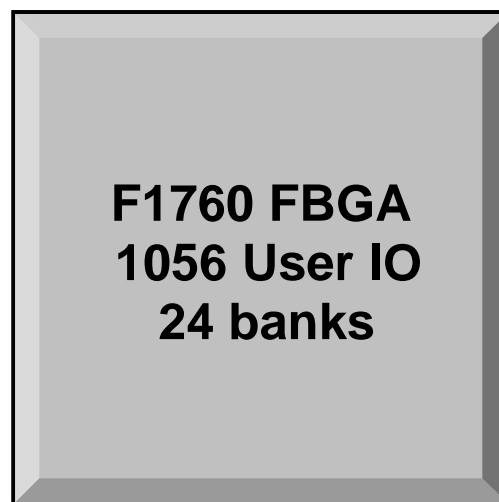
Efficient Modular I/O Banks

■ New modular bank structure
  – Many small I/O banks
    ● Fixed bank widths: 24, 32, 36, 40, or 48 user I/Os per bank
    ● 16 to 24 banks
    ● Greater pin efficiency
  – Common bank structure
    ● Eases device migration

Example showing how to combine various sized interfaces

18R/18W	9R/9W	9R/9W	18R/18W
72b DDR		72b DDR	

← 6 Banks →

16 to 24 I/O banks

F1760 FBGA
1056 User IO
24 banks

Bottom I/O: Same as Top

Right I/O: Same as Left

18R/18W	18 Read/18 Write QDR I/II/II+
9R/9W	9 Read/9 Write QDR I/II/II+
PCI 32	32 bit PCI
36b DDR	36 bit DDR I/II/III
PCI 64	64bit PCI
72b DDR	72 bit DDR I/II/III

Requires ? 120 I/O

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# On-Chip Termination on All Banks

- Parallel serial and dynamic on-chip termination for single ended DQ pins

- Dynamic termination for better control of reflections
  - Writes
    - Series termination enabled
    - Parallel termination disabled
  - Reads
    - Series disabled
    - Parallel termination enabled

- Calibrated for repeatable and predictable termination
  - Tolerance controlled with digital auto calibration circuits

OCT

Read

FPGA

Memory

Write

30

SOPC WORLD
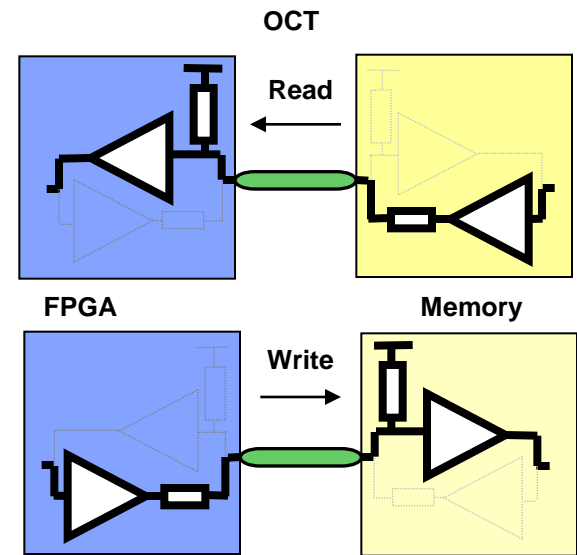
Integrated System for Rapid Implementation

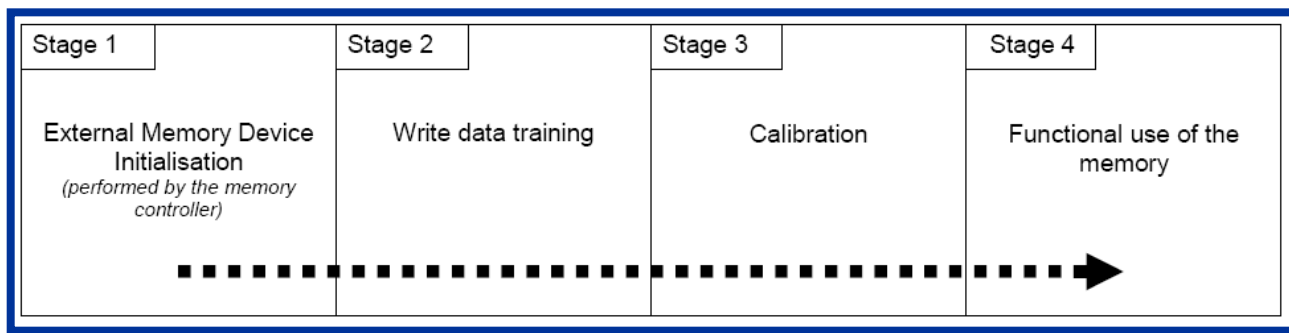■ **Altera offers free ALTMEMPHY megafunction to maximize performance**

– **ALT**era external **MEM**ory **PHY**sical layer interface

– Integrates hard I/O blocks and soft logic data path section

– Self-calibrating

– Optimized to take advantage of Stratix III silicon features

– Simple user interface

– Complexity kept inside
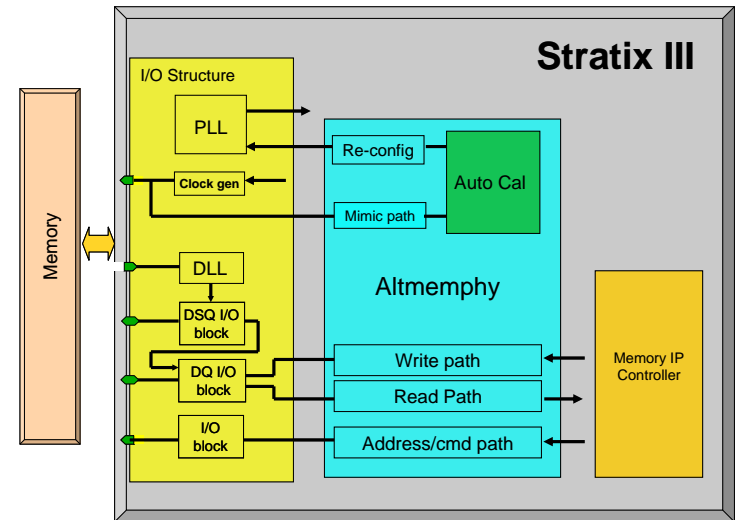
# Self-Calibrating for Highest Reliable Frequency of Operation Across PVT

■ **Self-calibrating control block**
  – Training pattern
    ● Calibrates out process differences on both FPGA and external memory
    ● Works on a pin-by-pin basis
  – Monitor and Adjust
    ● Monitors voltage and temperature variations during operation via mimic path
    ● Adjust resynchronization phase of PLL output without interrupting operation

| Stage 1	Stage 2	Stage 3	Stage 4
External Memory Device Initialisation *(performed by the memory controller)*	Write data training	Calibration	Functional use of the memory

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Configurable Megafunction

- Quickly and easily configure physical layer interface to match desired memory

- Optimized to take advantage of Stratix III I/O structures and hard blocks

- Constrained with Synopsys design constraints (SDC)
  - Industry standard
  - Easy to constrain data with respect to sourced clock
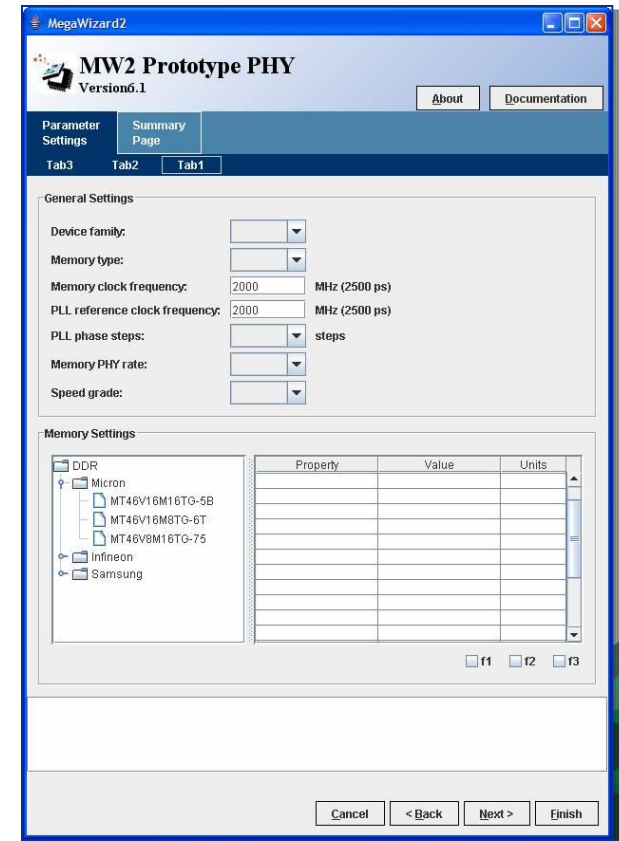
# TimeQuest Timing Analysis Tool

■ **ASIC strength timing analysis tool**
- Native support for industry-standard SDC timing constraints
- Easily constrain source synchronous interface
  - Constrain data with respect to clock
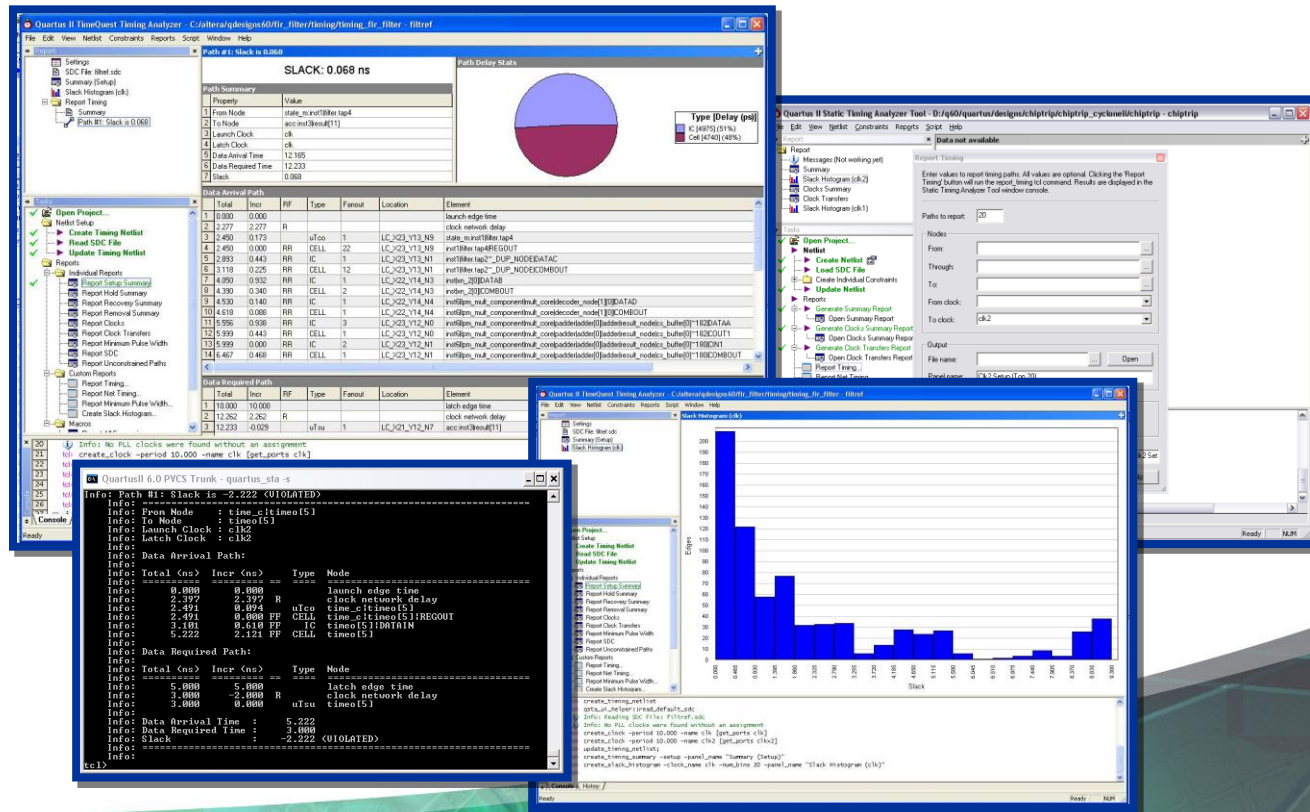
# Robust Signal Integrity Tool Support

- **Quartus II signal integrity analyzer**
  - Drives signal integrity analysis and automatic optimization
- **Signal integrity advisor**
  - Provides design-specific guidance
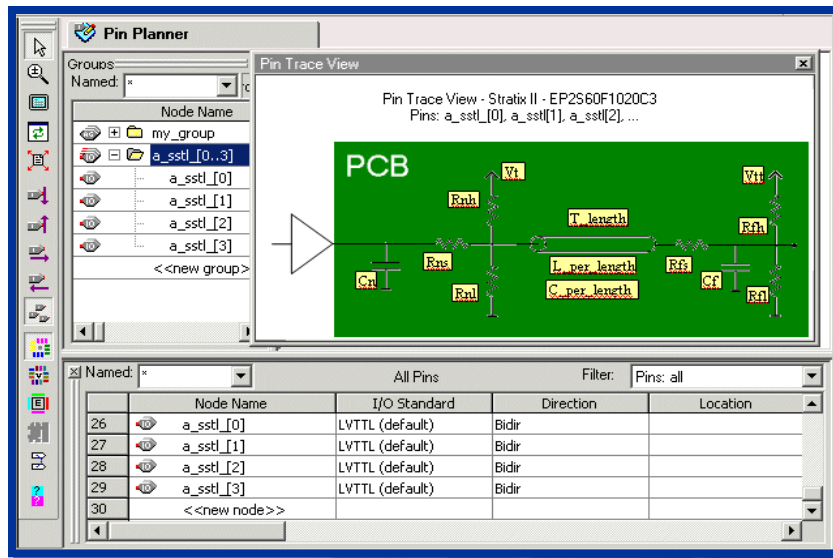
Per I/O Trace Compensation

■ Programmable single-ended I/O features that help compensate for trace characteristics

   – Controllable slew rate

      ● 4 settings to match desired I/O standard and control noise and overshoot

   – Programmable output drive strength

      ● Match desired I/O standard

   – Programmable output delay

      ● Board trace mismatch compensation

      ● Deliberately skew DQ data output

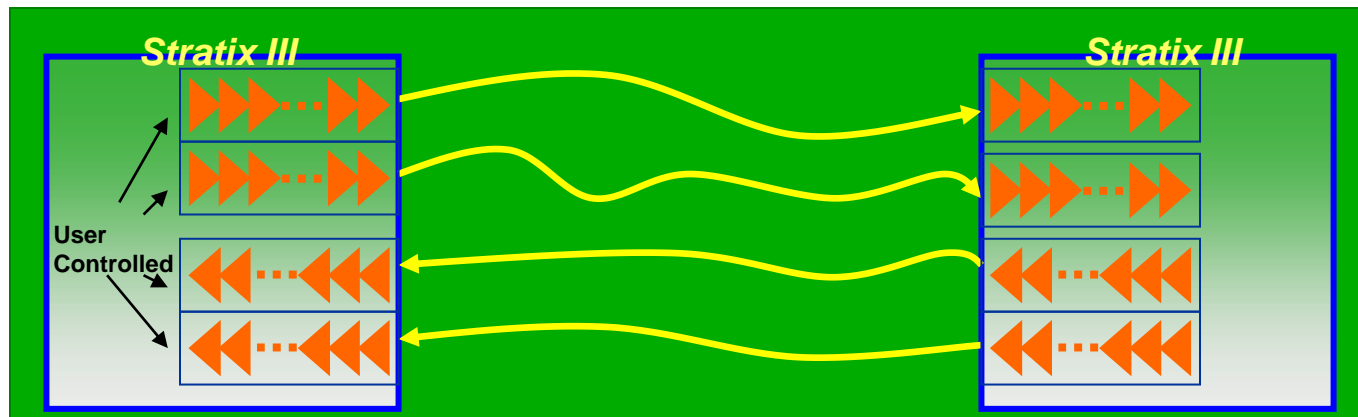   – Reduce simultaneous switching noise (SSN)
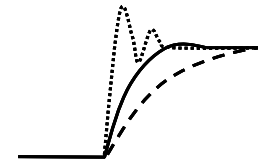
Settings depend on standard, SSTL-18 example shown

I/O Standard	mA	mA	mA	mA	mA	mA
SSTL-18 Class I	4	6	8	10	12	
SSTL-18 Class II			8			16

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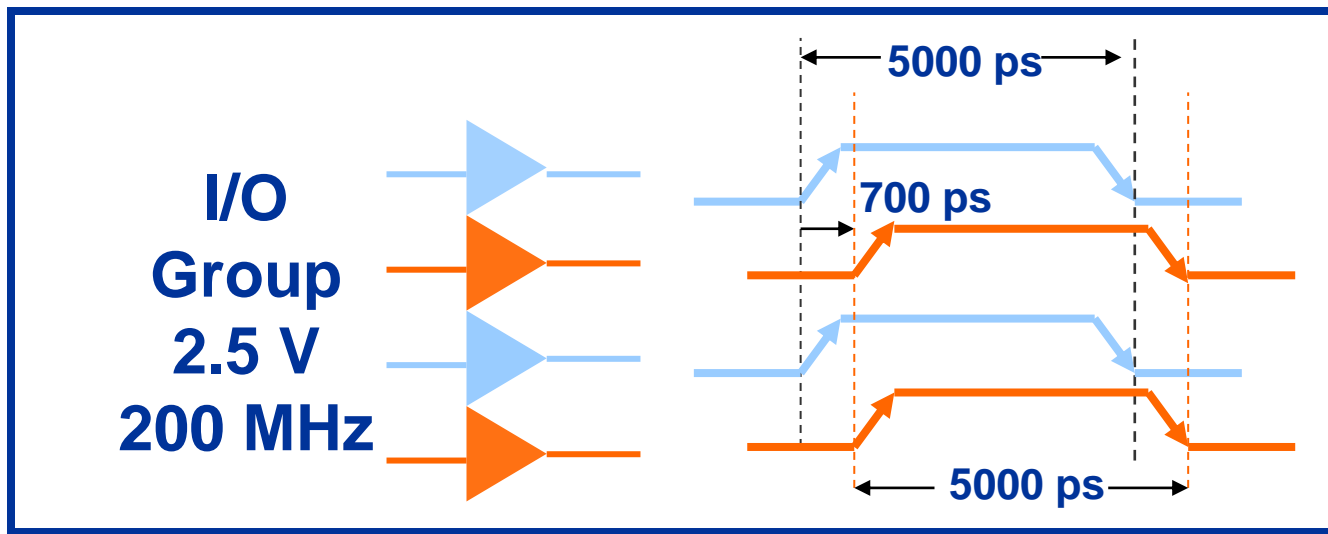# Board Trace Mismatch Compensation

- Output delay per I/O: 0 to 1000 ps
- Input delay per I/O: 0 to 800 ps
- Digitally programmable in 50 ps steps
- Compensation for 0 to 5 ½ inches
  - FR4 delay: ~170 ps/inch

Deliberately Skew DQ Data Output

- Reduce SSN
    - Delaying adjacent edges reduces total number of simultaneous switching output (SSO) edges
    - Controllable in 50 ps steps

Signal Integrity Enhancements

■ Programmable slew rate

 – Lowering signal rise time reduces $\partial i/\partial t$

■ Signal integrity die and package enhancements

 – Increased number of power/ground pairs reduces L

■ Deliberately skew DQ data output

 – Delaying adjacent edges to reduce simultaneous edges

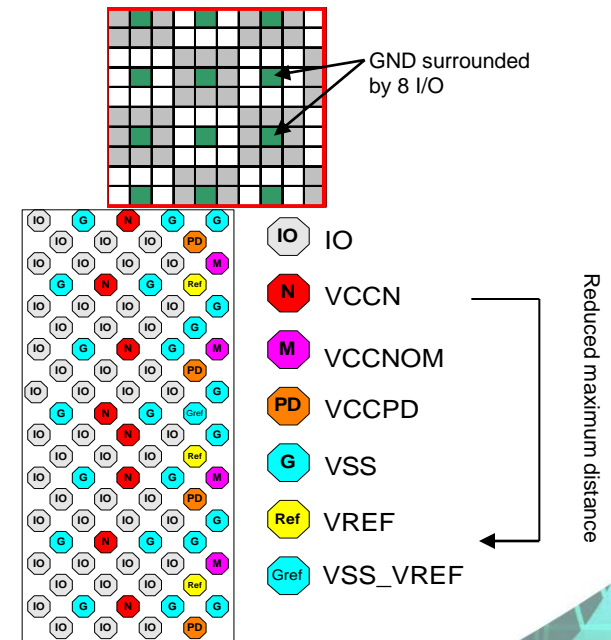*SSN Depends on Loop Inductance and Signal Rise Time*

$L\ \partial i/\partial t$
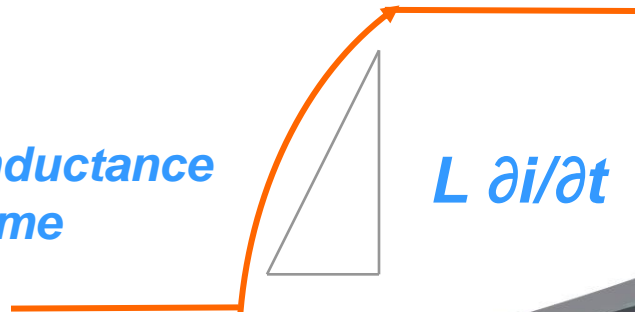
Signal Integrity Package and Die Enhancements
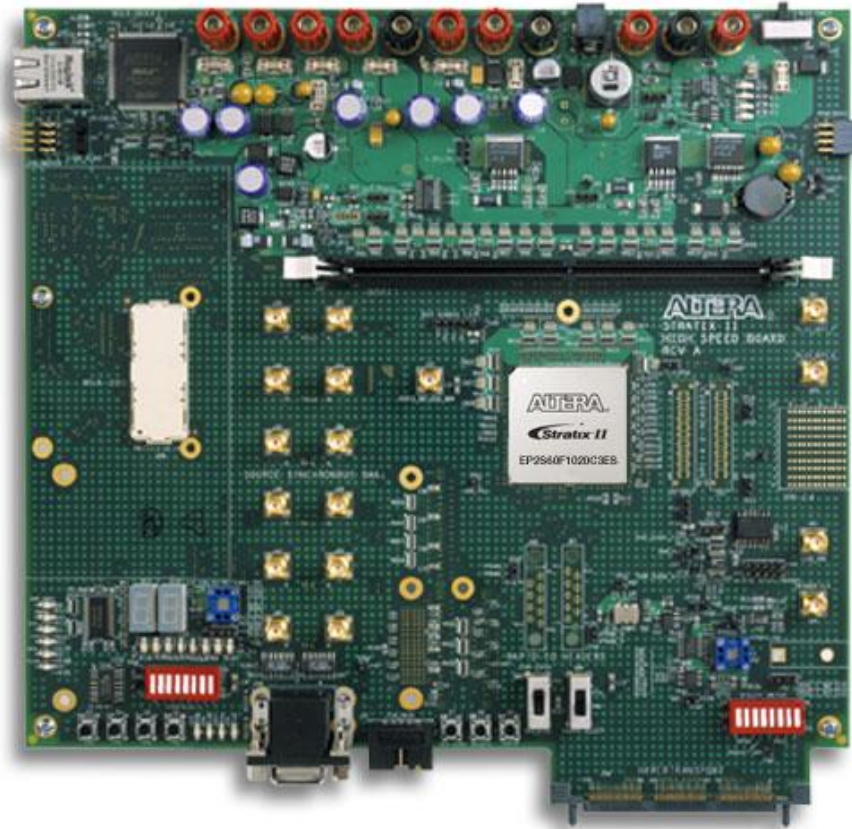
- **Package enhancements**
  - 8:1:1 user I/O-ground-power ratio
  - Limited number of I/Os per bank
  - Maximum distance between I/O and GND = 1
    - Reduced loop inductance in package
- **Die enhancement**
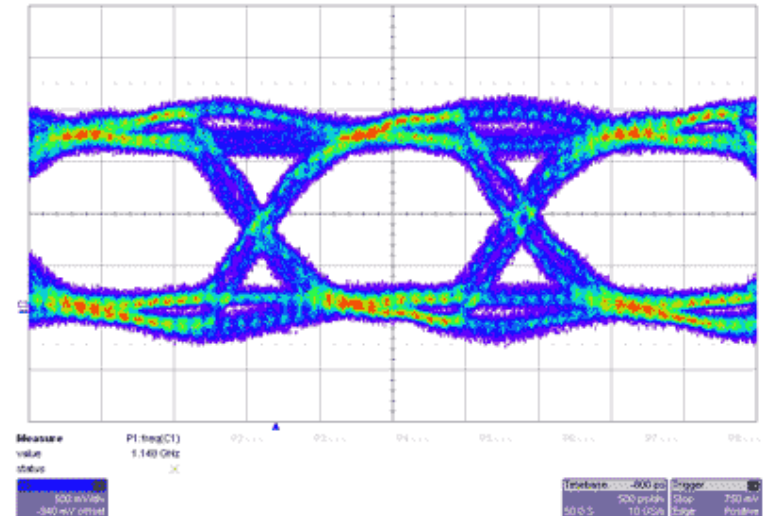 - Extensive distributed ground bumps
    - Enhanced return path
  - Programmable edge rate control
  - Programmable staggered outputs
    - Control SSO noise

GND surrounded by 8 I/O

Reduced maximum distance

- **IO** — IO
- **N** — VCCN
- **M** — VCCNOM
- **PD** — VCCPD
- **G** — VSS
- **Ref** — VREF
- **Gref** — VSS_VREF

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667-Mbps DDR2 SDRAM Interface

DDR2 SDRAM Write Data Eye 667 Mbps

*For Stratix II Devices

Conclusion

- Interfacing with external memory devices has I/O timing, controller design, and board design challenges

- Stratix series FPGAs from Altera provide advanced features to meet I/O interface challenges

- Fully verified hardware platforms including Altera IP and board design tools simplify memory interface design

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Thank You
Q & A

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