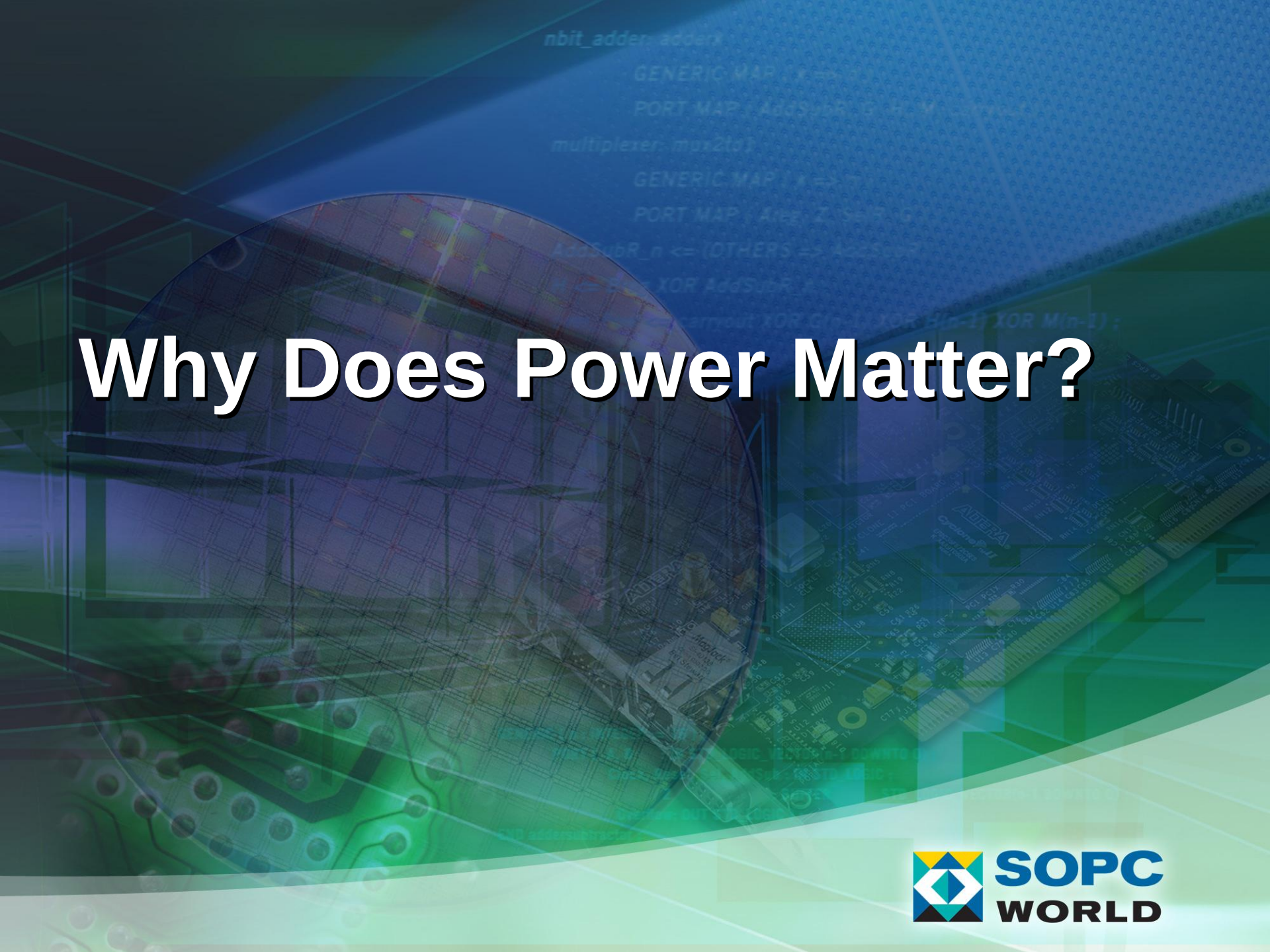
Why Does Power Matter?



SOPC WORLD

Agenda

- Introduction
- Power in low-end applications
- Power in high-end applications
- Designing for power
- Conclusion

Applications Demand Lower Power

Low-End Applications

Example:

- Portable media players
- Modems and customer's premises equipment (CPE)
- Software-defined radio

- **Battery operated**
- **Form factor restrictions**
- **Operating conditions**

High-End Applications

Example:

- Core routers
- Backplanes
- High-performance digital signal processing (DSP)

- **High performance**
- **New process nodes**
- **Operating conditions**

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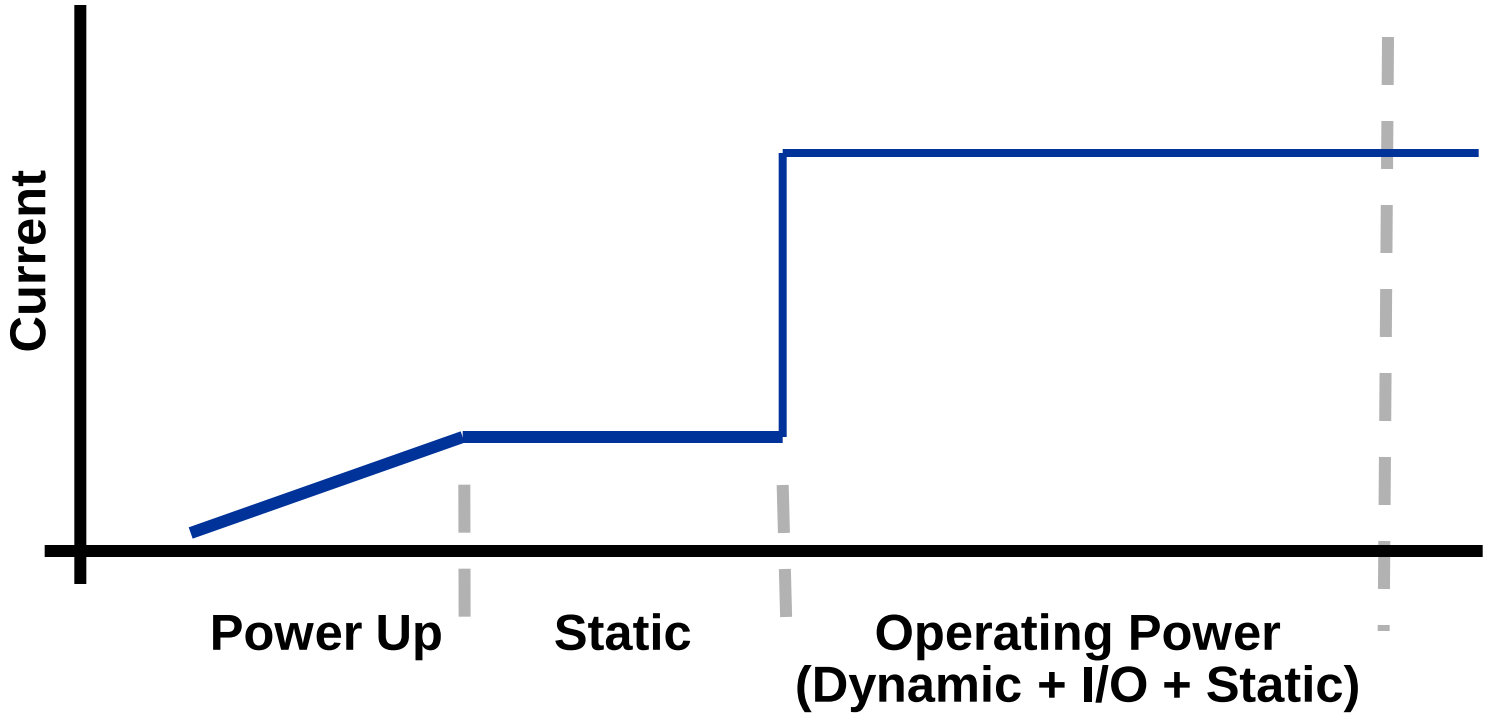
Power in PLDs



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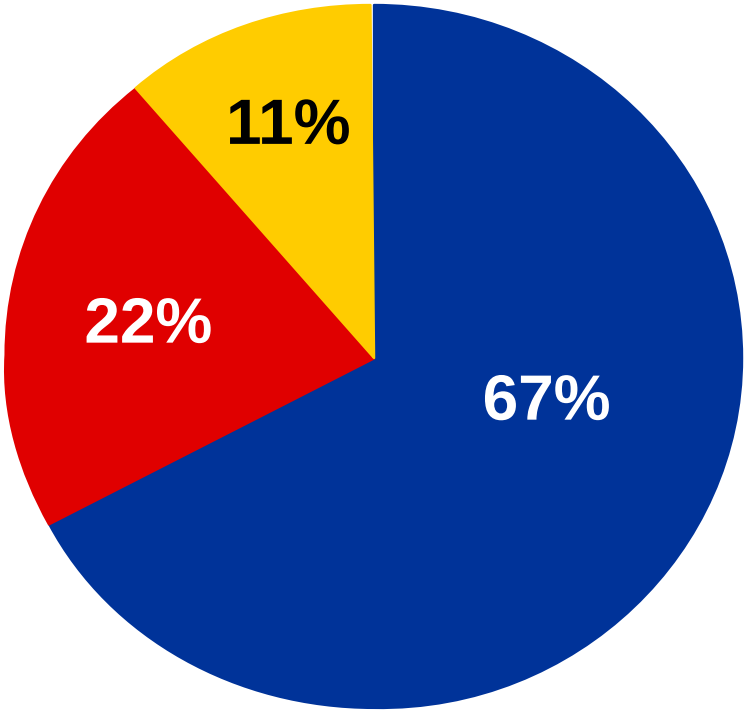
Operating Power



Analysis of 99 User Designs

- Core dynamic
- Core static
- I/O

Dynamic Power Dominates

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Power in Low-End Applications

Low-End Applications

- Meet customer performance and power/thermal requirements simultaneously
- Eliminate or reduce cost of cooling systems
- Enable operation in thermally challenged and space-constrained environments
  - Airplane cockpits, software-defined radios
- Extend battery life for portable applications

Portable Applications

Point of Sale

- Scanners
- RF identification device (RFID)
- Tax collection
- Credit checks
- ATM PIN terminal

Everything wireless

- Bluetooth
- Wireless fidelity (WiFi)
- 802.11x
- Headphones
- Camera
- Game controllers

OS processor

- Industrial PDA
- Test equipment
- Remote terminal
- GPS
- Portable media player

Sensors

- Gas
- Temperature
- Machine-vision
- Location/GPS
- RF signal
- RFID

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Portable Applications and Requirements

Applications	Requirements		
	3.3 V	High I/O Count	High Density
Consumer handheld (Educational toys and portable media players)	✔	✔	✔
Handheld instrumentation (Bar code scanners and handheld testers)	✔	✔	
Industrial computer (Meter readers and industrial PDAs)	✔	✔	✔
Industrial cameras (Camera modules)	✔	✔	
Wireless and wireline (Optical modules and PCMCIA express cards)	✔	✔	

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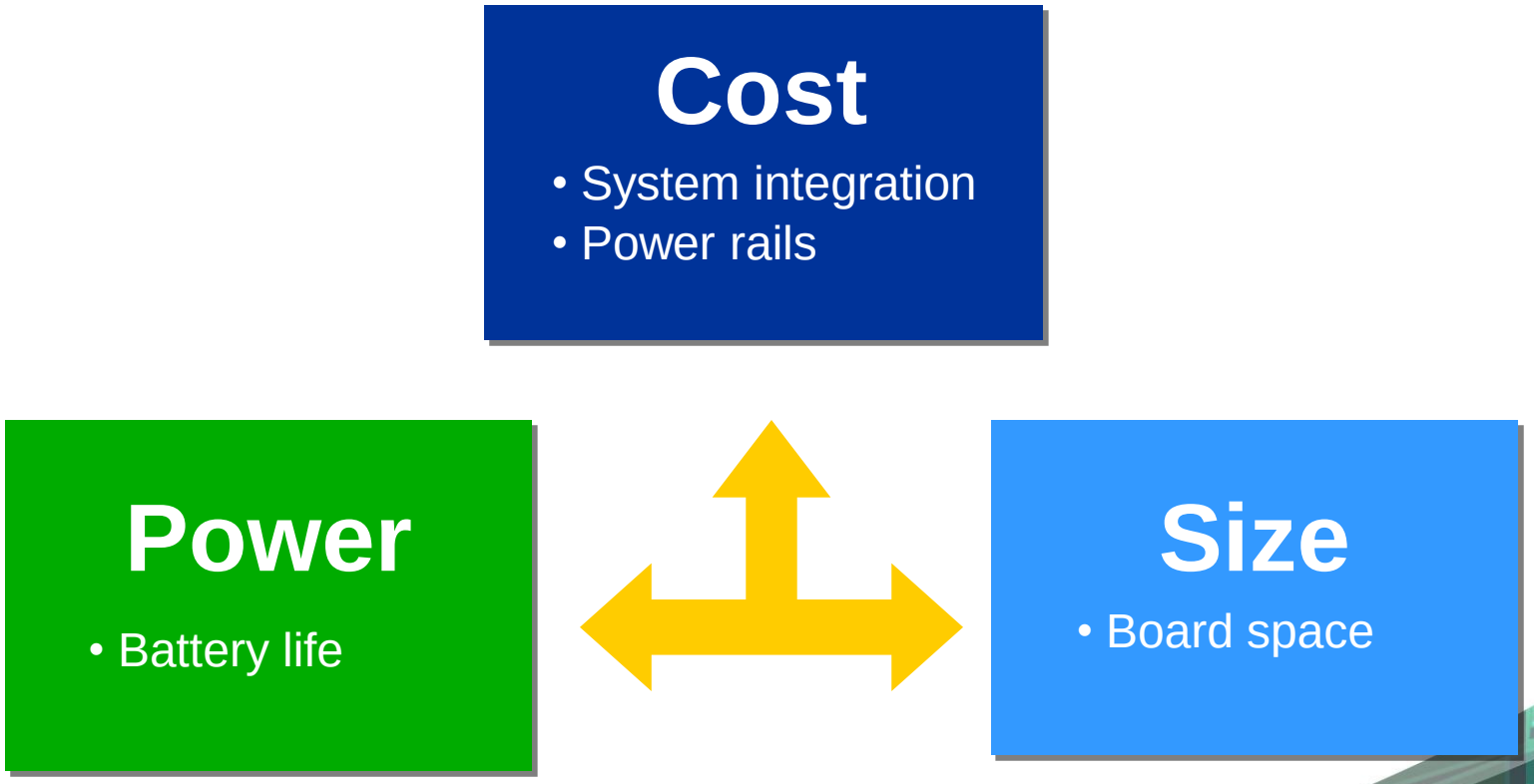
Portable Design Challenges



Low-Power Considerations

- Reduce power consumption in devices
  - How portable, consumer products designers model power consumption
  - Using this model to evaluate CPLDs
- Manage power for entire system
  - Self power down
  - Auto power up
  - Power management

Power Consumption Model

Mode	Definition	Power Consumption
Active	Part is being used	Dynamic power Application dependent
Standby	Part is powered, but not being used	Static I_{CC}, but only valid if no inputs are switching
Sleep/ Hibernate	Inactive, but retains information	< 50 - 100 uA
Off	Powered off	Zero power

Static I_{CC} Is Difficult to Achieve

- Low static I_{CC} depends on:
  - Small density: limits PLD usefulness
  - Quiescent I/Os: but “don’t care” inputs are often toggling
- Customers prefer to power off the device when not used

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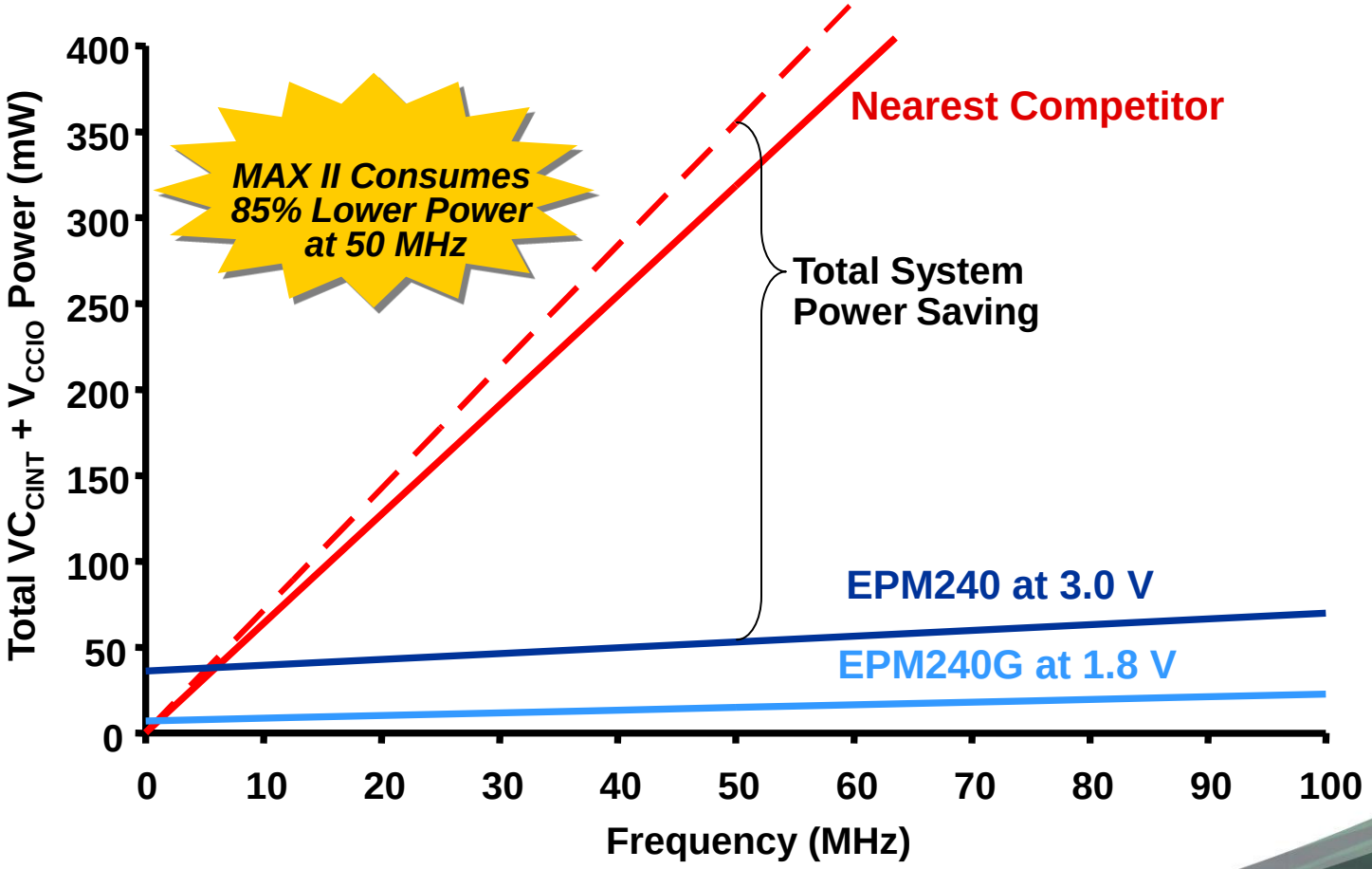
Off Mode Constraints

- CPLD core and I/O can be powered off and on in any sequence
  - Outputs must not affect the system operation
- When CPLD is powered off, inputs can be driven with
  - No damage to part
  - No power consumption

MAX® II CPLDs in Off Mode

- No power sequence requirements
  - Outputs: stable and do not affect the rest of the system
- Well-behaved I/O
  - Active inputs: no damage
  - Active inputs: no power consumption

Dynamic Operation Power Consumption



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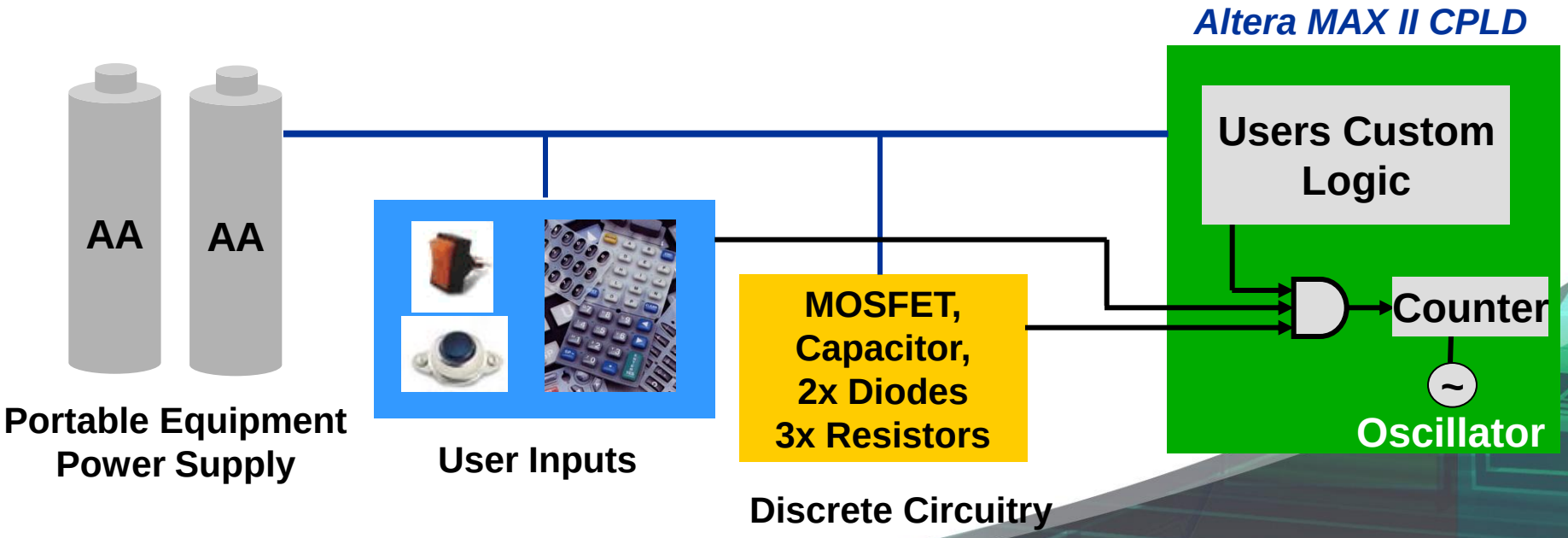
CPLD Power-Down Mode

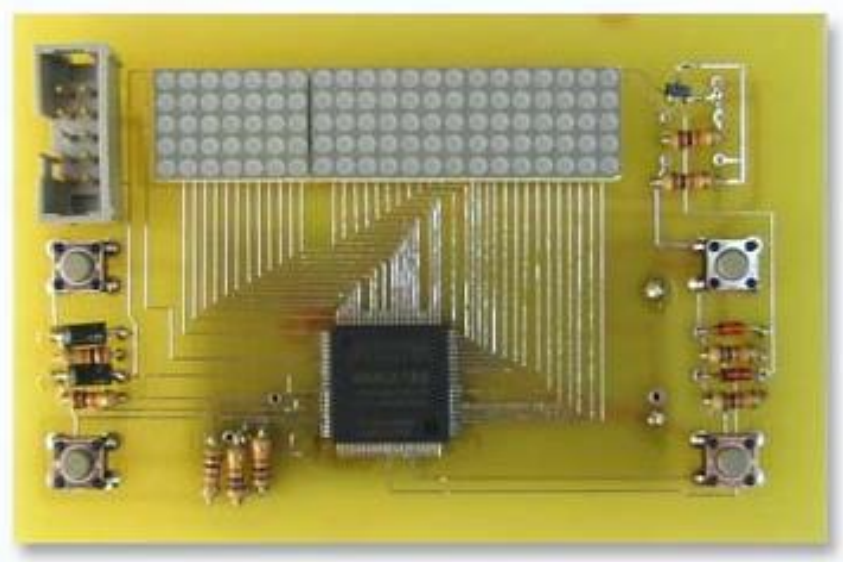
- Auto power down and instant-on (300 us)
- Internal oscillator makes system self contained
- Hot socket + power down mode
  - OK to drive CPLD I/Os: no damage and no power consumption
- Concept can be expanded to overall system power management



MAX II Power-Down Mode Design

- Application note and design files

Available Now



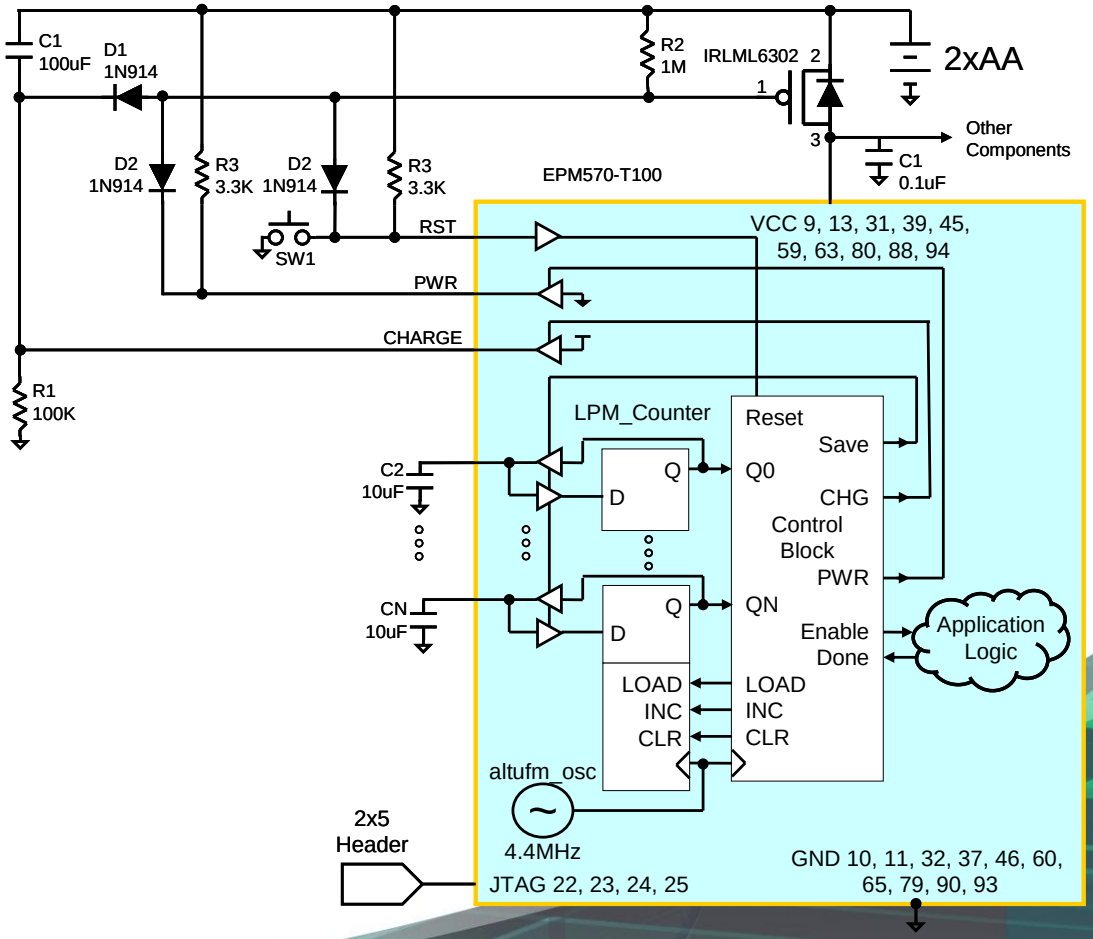
Front

Back

SOPC WORLD

Auto Power Up

- Extends MAX II CPLDs to include auto power up (APU)
- Numerous applications
  - Self-optimized power management
  - Multiple input power up
  - Periodic status checks



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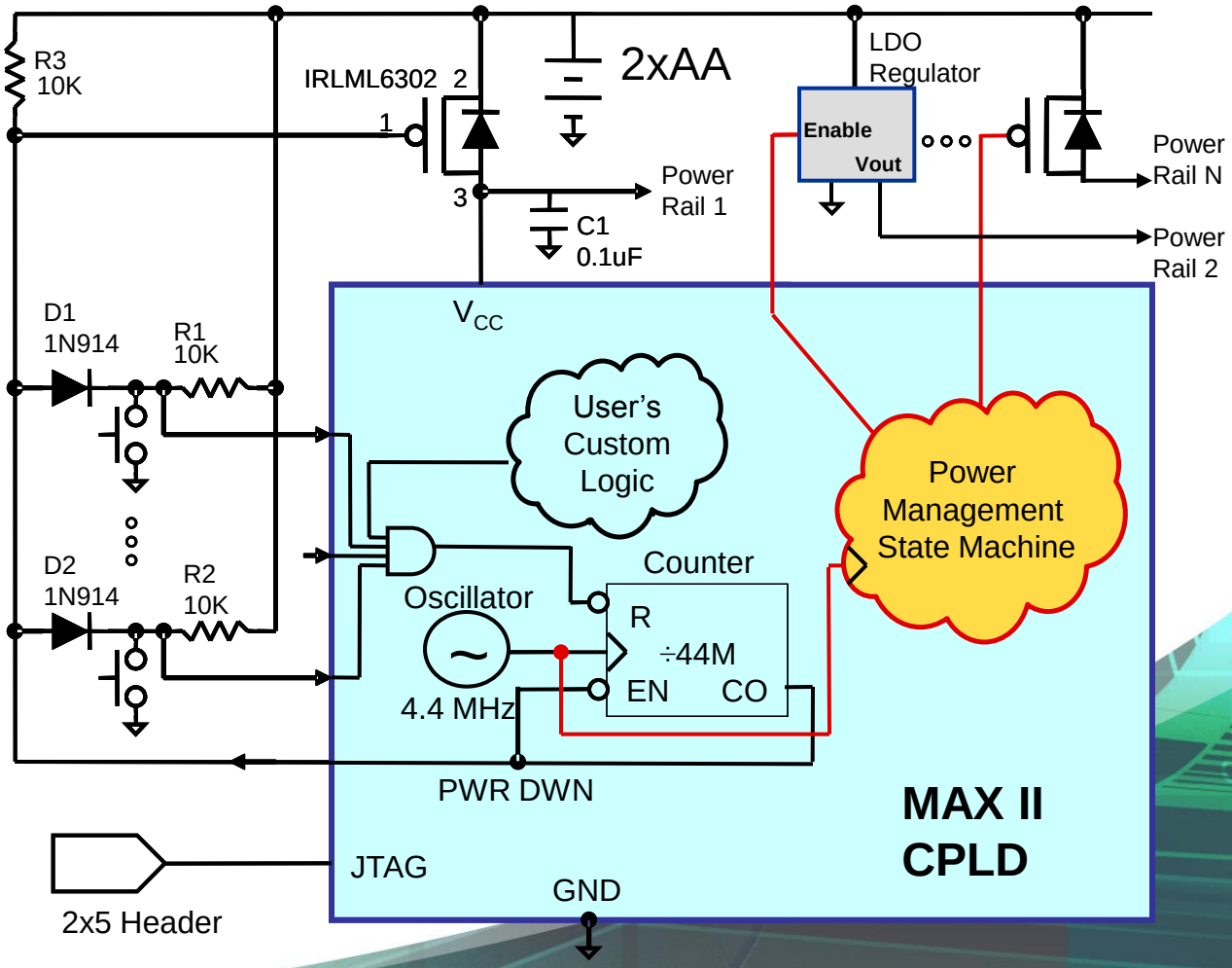
Controlling System Power

- Extend MAX II power-down design to include complete system power management
- MAX II CPLD is always the first to power up and the last to power down



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Power in High-End Applications

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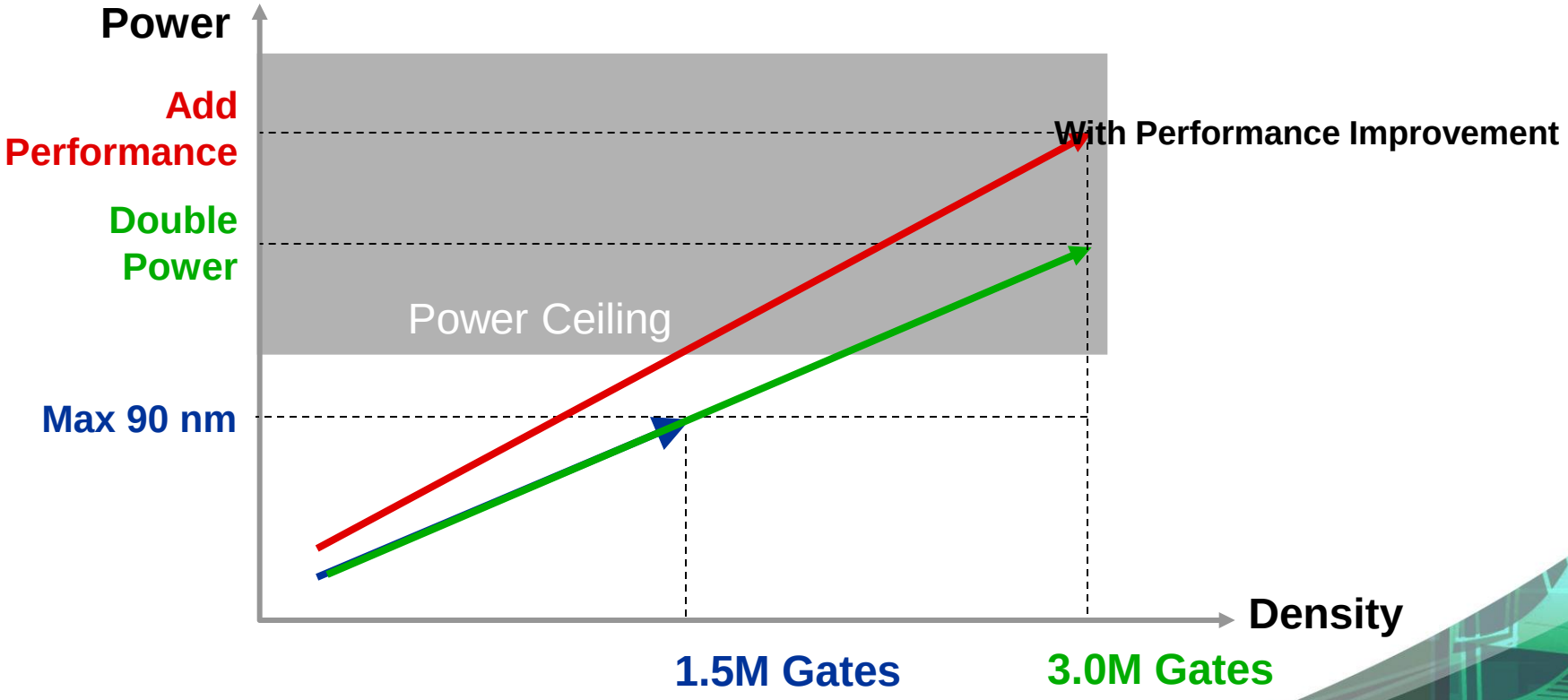
Factors Affecting Power

- New process technologies
  - Voltage and dimension scaling
  - Silicon characteristic changes
  - Novel materials used
- Higher performance and higher density
  - Affects dynamic power
  - Process changes
  - Geometry shrink

Power Challenge



Power limitations for applications while scaling

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Leading Edge Process Technology

Process or Design Technology	When Altera Introduced	Benefit
All Copper Routing	180nm	Increased performance
Low-K Dielectric	130nm	Increased performance Reduced power
Multi-Threshold Transistors	90nm	Reduced power
Variable Gate-Length Transistors	90nm	Reduced power
Triple Gate Oxide	65nm	Reduced power
Super-thin Gate Oxide	65nm	Increased performance
Strained Silicon	65nm	Increased performance

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Leading-Edge Process Technology

Increased Performance, Reduced Power

- Advanced 65-nm process
  - 15% capacitance reduction → reduces dynamic power 15%
- Strained silicon
  - Increased performance
- Multiple-gate oxide thicknesses (triple oxide)
  - Tradeoff: power vs. speed per transistor
- Multiple-threshold voltages
  - Tradeoff: power vs. speed per transistor
- Low-k inter-metal dielectric
  - Reduces dynamic power, increases performance
- Copper interconnect
  - Increased performance, reduced IR drop

Altera at 65 nm

- Maximum performance with minimum power
  - Innovative architecture and circuit techniques
  - The latest process optimizations
  - Integrated software solutions
- Customers get:
  - Performance they need with the minimum power
  - High productivity with automated tools that meet target performance and minimize power

Industry-Leading Low-Power Technology

Stratix® III Power Reduction Technique	Lower Static Power	Lower Dynamic Power
Silicon Process Optimizations	✓	✓
Programmable Power Technology	✓	✓
Selectable Core Voltage (0.9 V or 1.1 V)	✓	✓
Quartus® II PowerPlay Power Optimization		✓

Stratix III FPGAs Are the Lowest Power High-End FPGAs Available

SOPC WORLD

Individual Block Optimization

- All core blocks completely redesigned for 65-nm process AND power reduction
  - Adaptive logic module (ALM), memories, DSP, CRAM, etc.
- Every mode of operation is optimized for:
  - AC: Least amount of switching activity
  - DC: Low-power mode setting for all unused circuitry
- Combined hardware hooks and Quartus II software intelligence to achieve power savings

Dynamic Power

- Process reduction reduces capacitance and voltage

$$P_{dynamic} = \left[\frac{1}{2} CV^2 + Q_{ShortCircuit} V \right] f \cdot activity$$

Capacitance charging

Short circuit charge during switching

Percentage of circuit that switches each cycle

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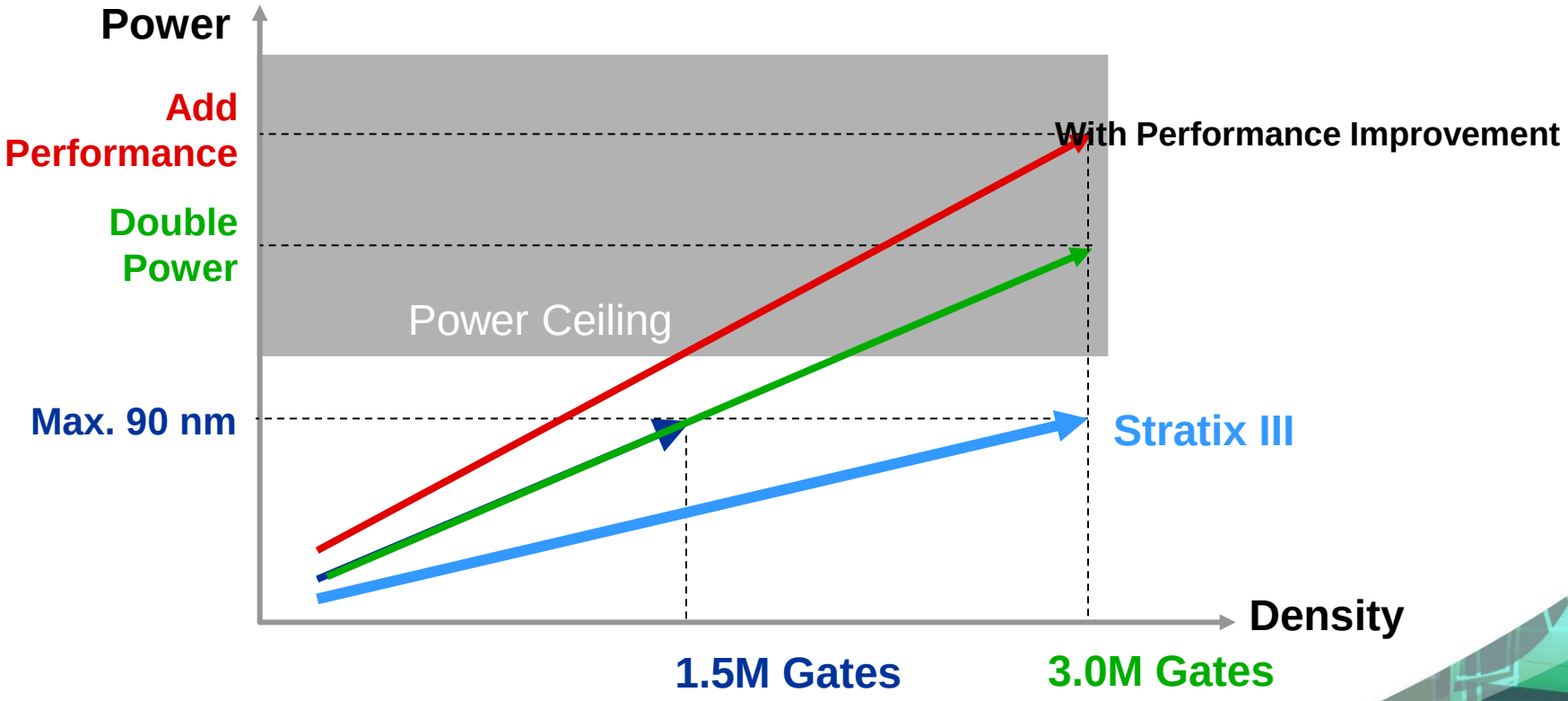
15% Reduced Capacitance

- 15% power reduction proportional to reduction in capacitance
- Source of lower capacitance
  - Process scaling
  - Design improvements

Power Challenge



Stratix III FPGAs Cut Power by 50% vs. 90 nm

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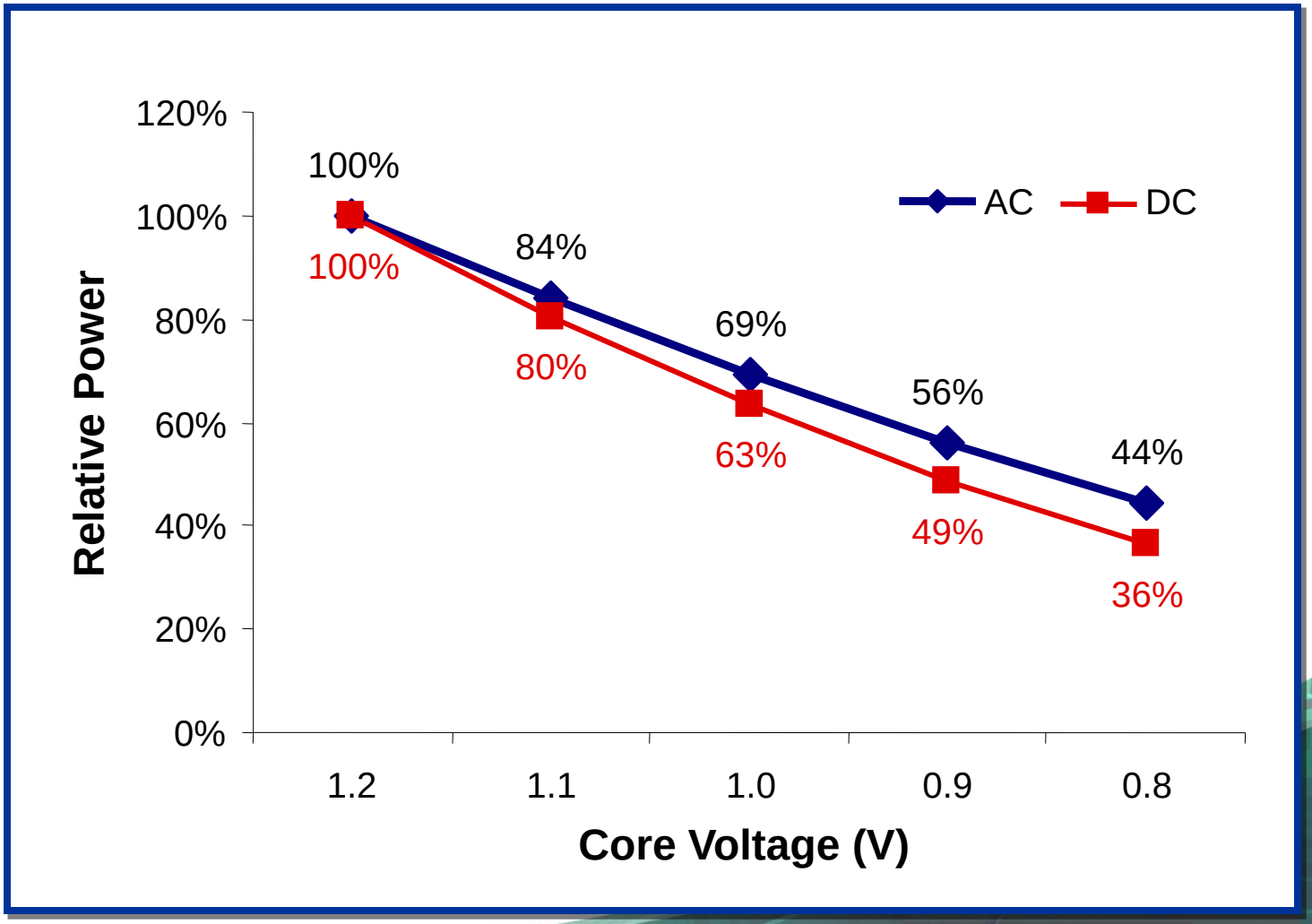
Selectable Core Voltage

- User selects core voltage operation
  - 0.9 V* or 1.1 V

Core Voltage	Dynamic Power Reduction** from 1.2 V	Static Power Reduction*** from 1.2 V
1.1 V	16%	20%
0.9 V	44%	51%

* 0.9 V requires an additional power supply
** Dynamic power decreases by square of voltage reduction
*** Static power decreases by ^2.5 of voltage reduction

Core Voltage Component



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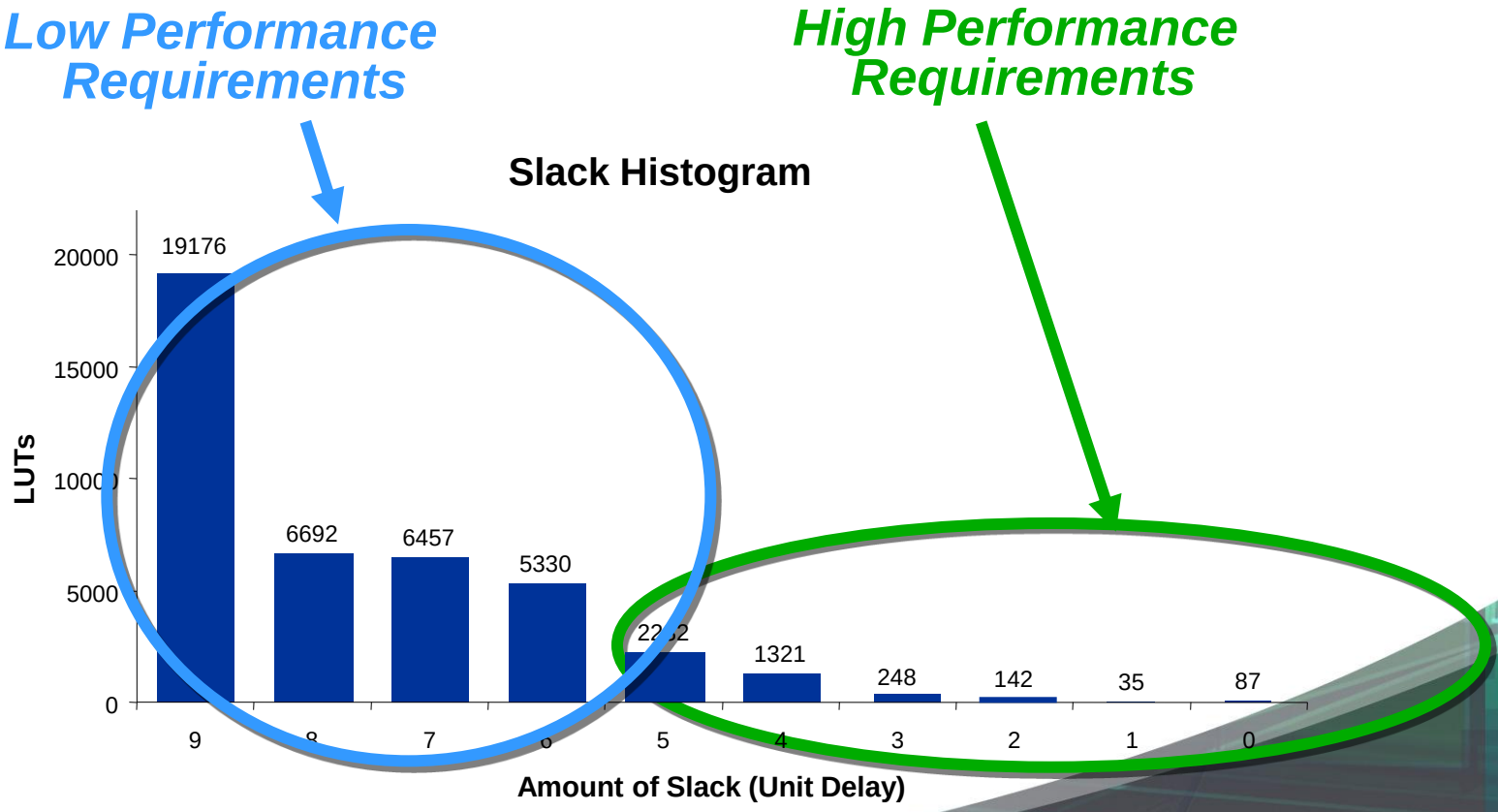
Design-Specific Power Optimization

- Only a small proportion of logic is performance-critical



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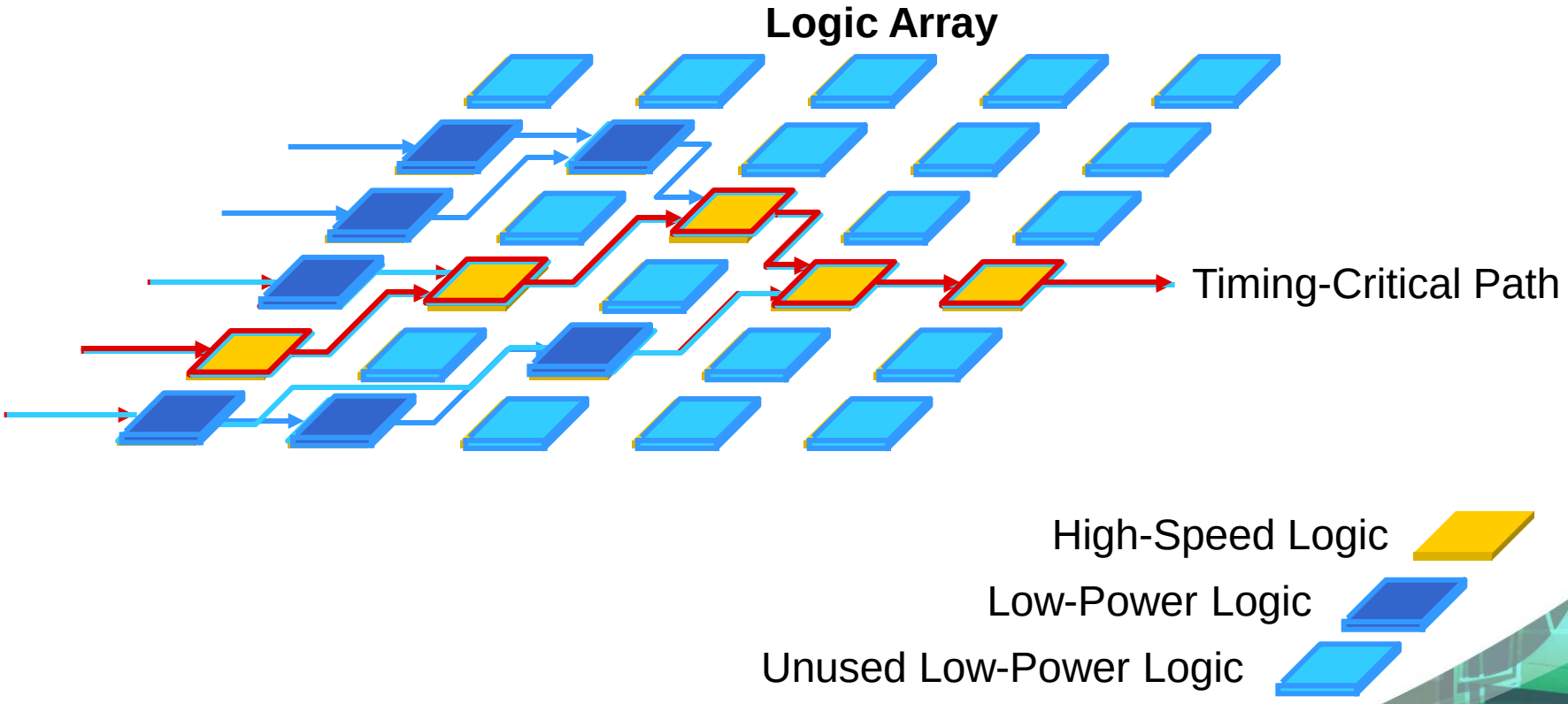
Programmable Power Technology

- Block-level adjustments lower total power consumption
  - Automatically programmed via Quartus II software based on design's performance requirements
- Puts the performance where you need it
  - Minimizes power everywhere else
- Patented techniques exclusively used by Altera

Reduces Power Without Impacting Performance

Programmable Power Technology



Performance Where You Need It, Lowest Power Everywhere Else

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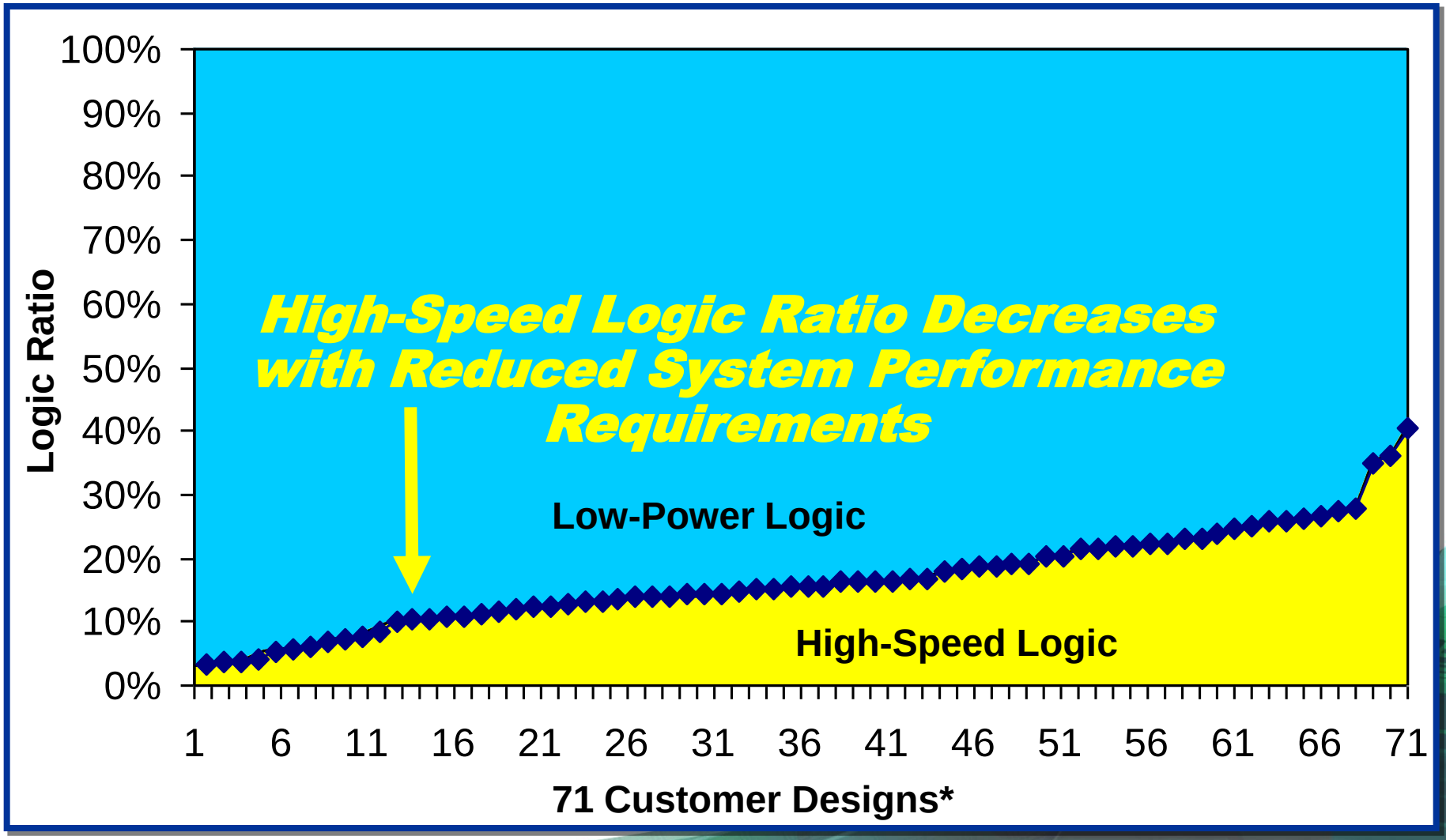
High-Speed vs. Low-Power Logic



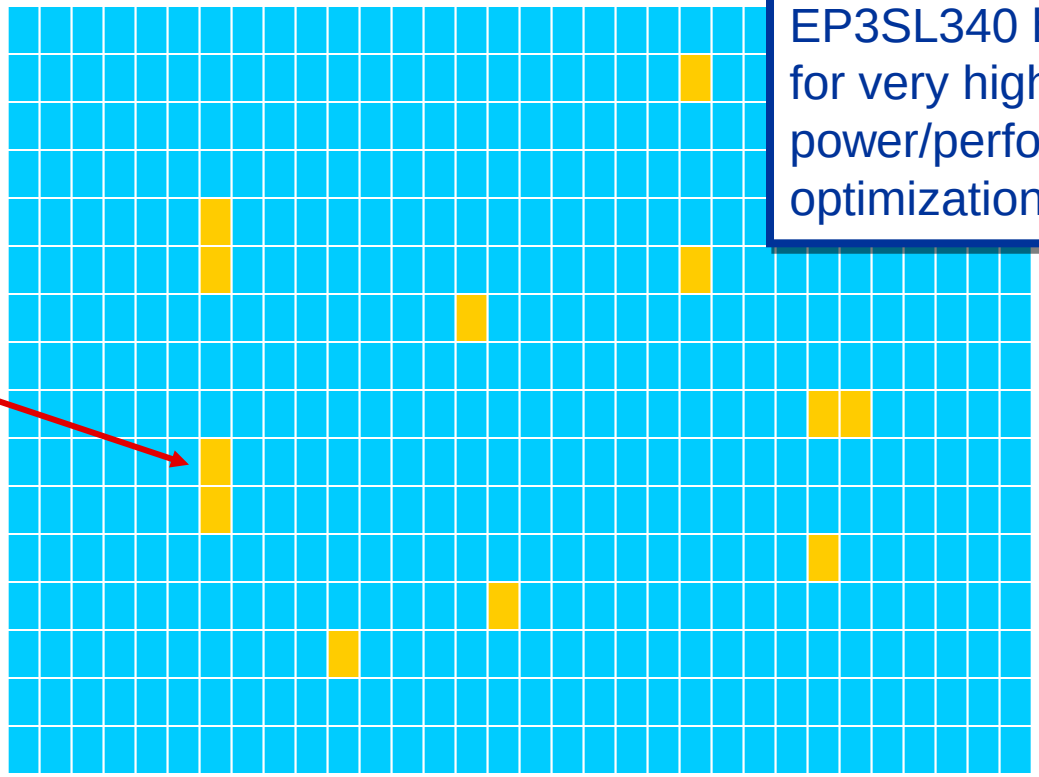
*All designs compiled for maximum performance.

SOPC WORLD

High-Resolution Power Control

EP3SL340 has **13,500 LABs** for very high-resolution power/performance optimization

Only small % of LABs need to be fast to maintain the system performance



Speed of the Fastest LABs, Power of the Slowest

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Designing for Power

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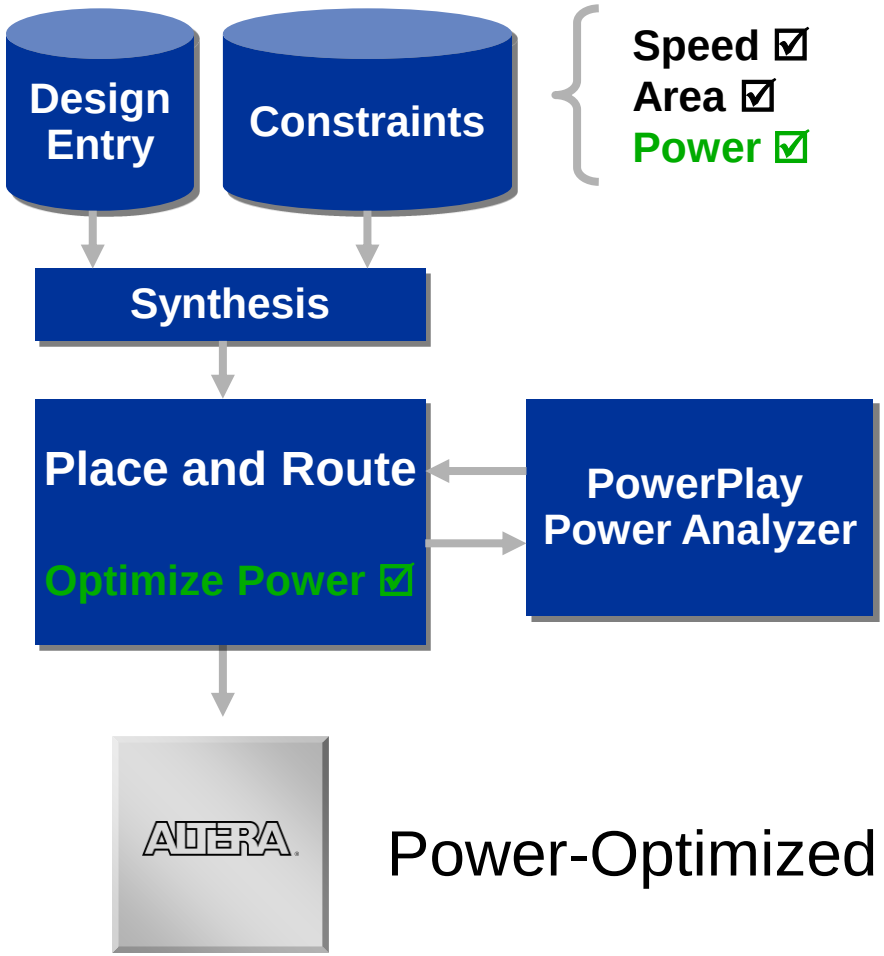
Designing For Power

- Need to plan for power right from the beginning of the design
  - Cannot wait until board bring-up
- Design tools available for managing power in FPGAs
  - PowerPlay Analyzer
- Power-based design optimization possible
  - PowerPlay Advisor

Automated Power Optimization



Power-Optimized Design ☑

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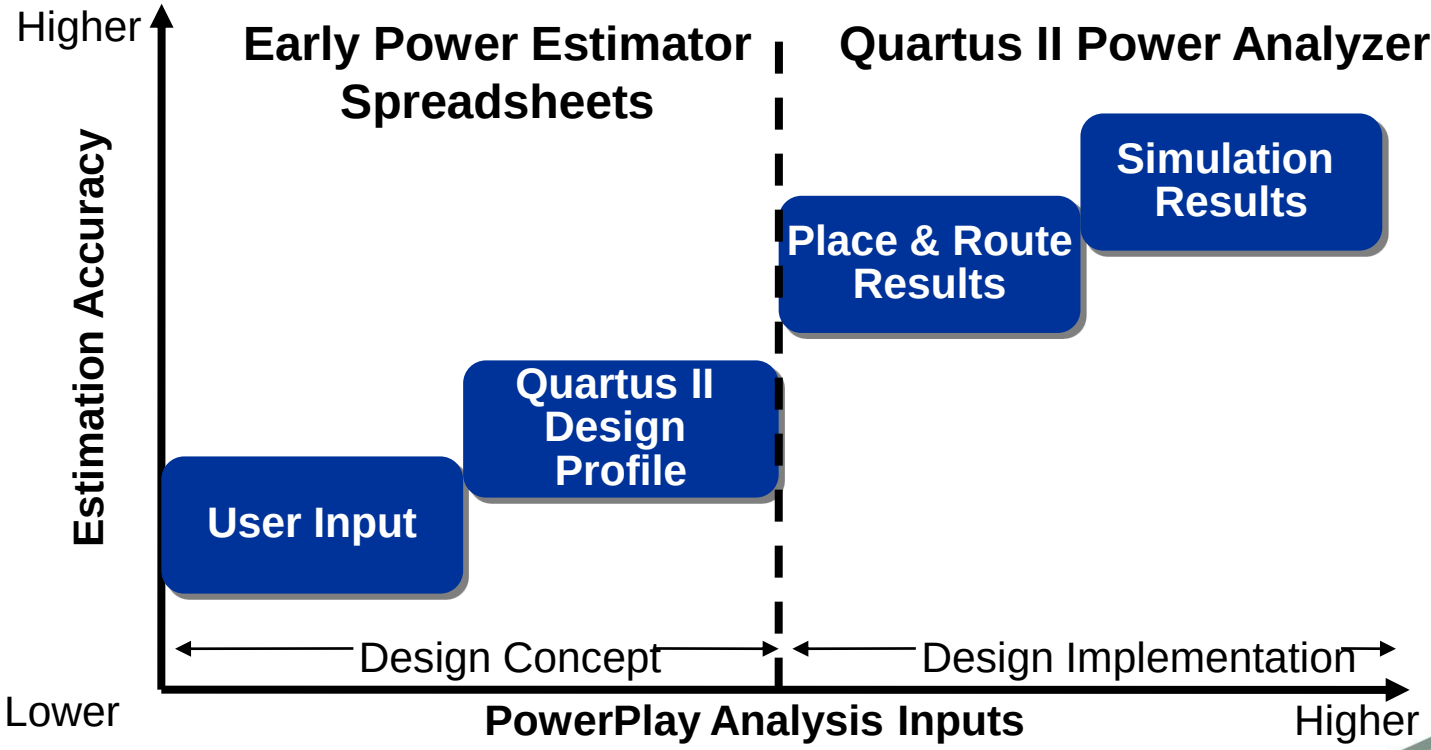
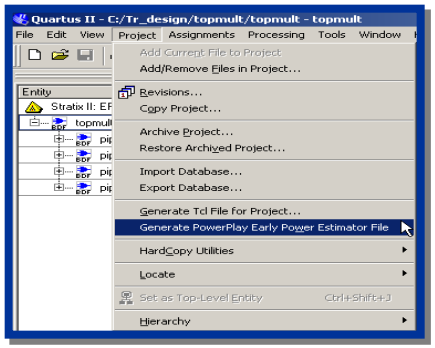
PowerPlay Power Analysis Tools



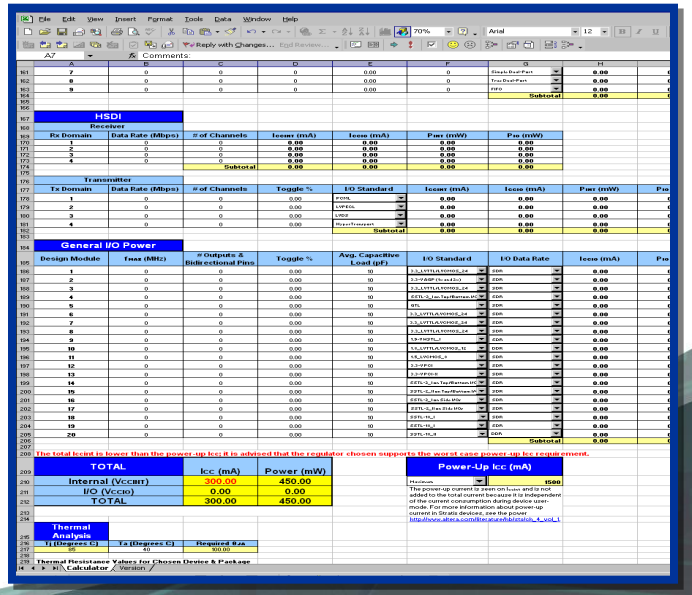
SOPC WORLD

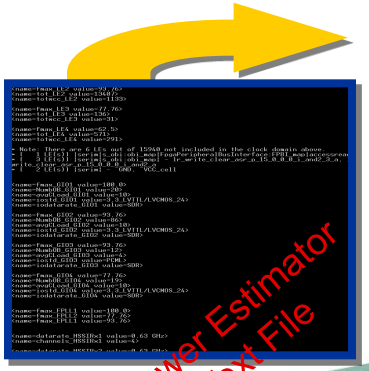
PowerPlay Early Power Estimator

- Quartus II software generates file and macro to import into web-based Excel spreadsheet
- Can estimate performance for partially complete designs
  - User can modify number of logic elements (LEs), etc. in Excel
  - Computes power as a function of number of LEs, I/Os, clock frequencies, activities, etc.



PowerPlay Early Power Estimator spreadsheet imports text file.





Quartus II software generates Power Estimator text file.

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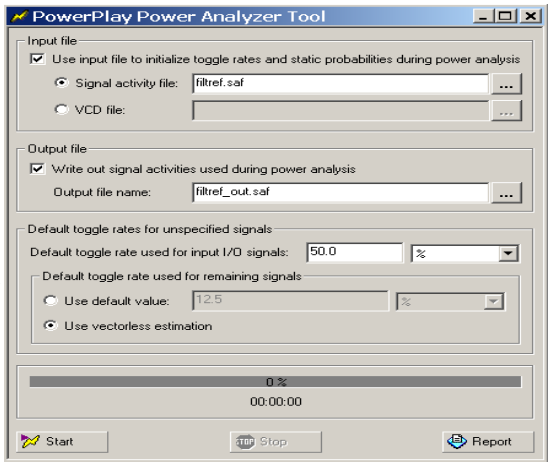
PowerPlay Power Analyzer

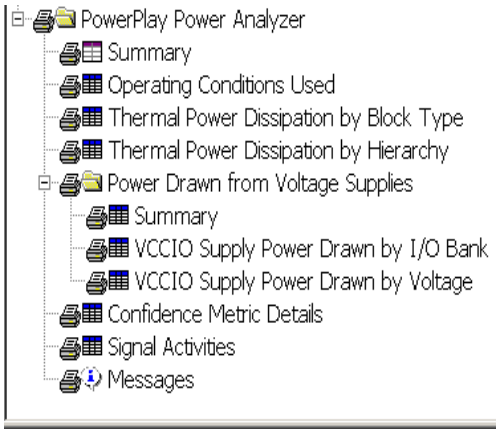
User Inputs

- RTL or Timing Simulation (VCD*)
- Default Node Activity
- Operating Conditions

PowerPlay Analyzer



Reports



QUARTUS® II

- Power models
- Place-and-route results
- Vectorless activity rates

Analyze Power

*VCD: Vector Change Description

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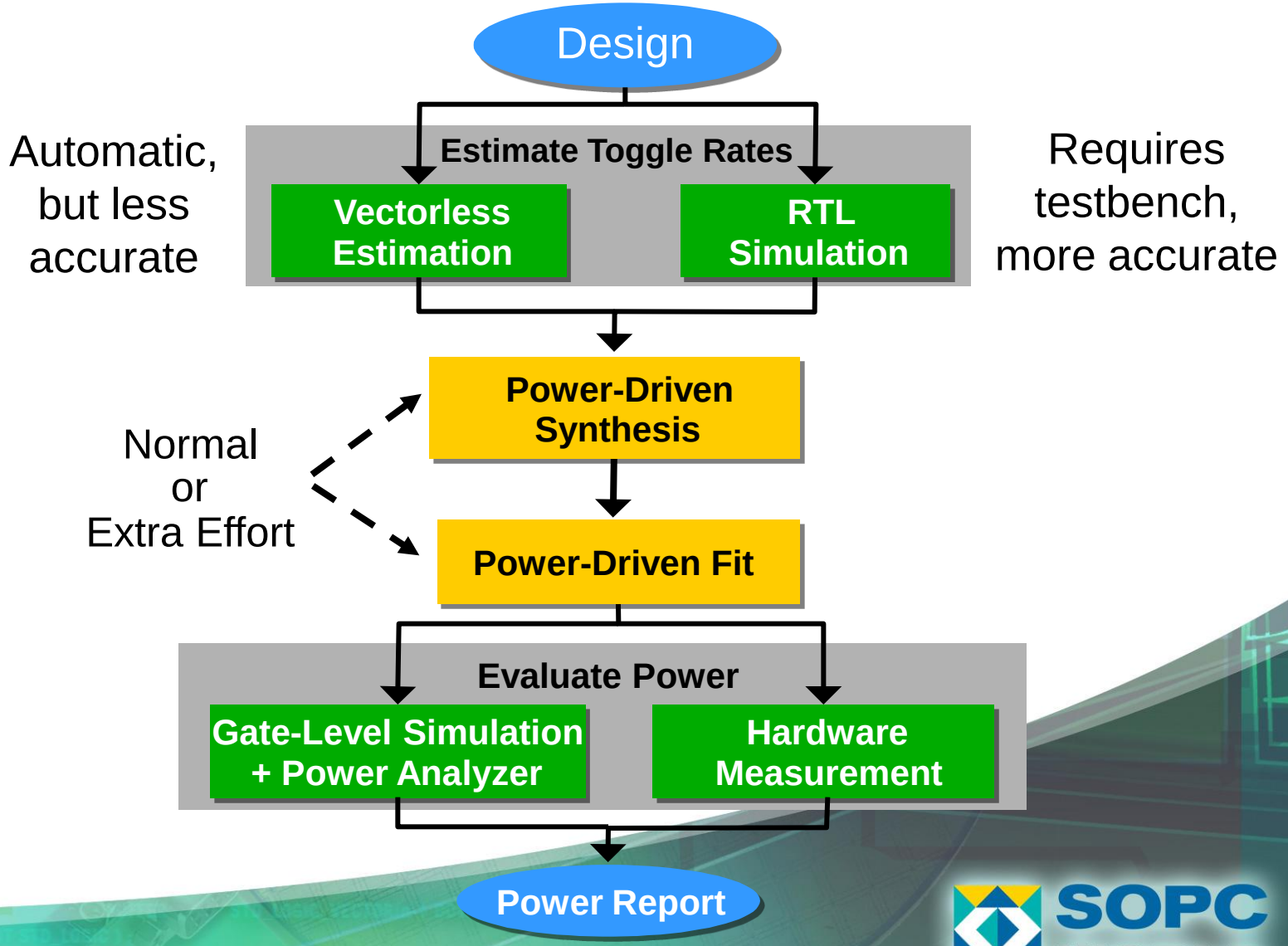
PowerPlay Power Optimization



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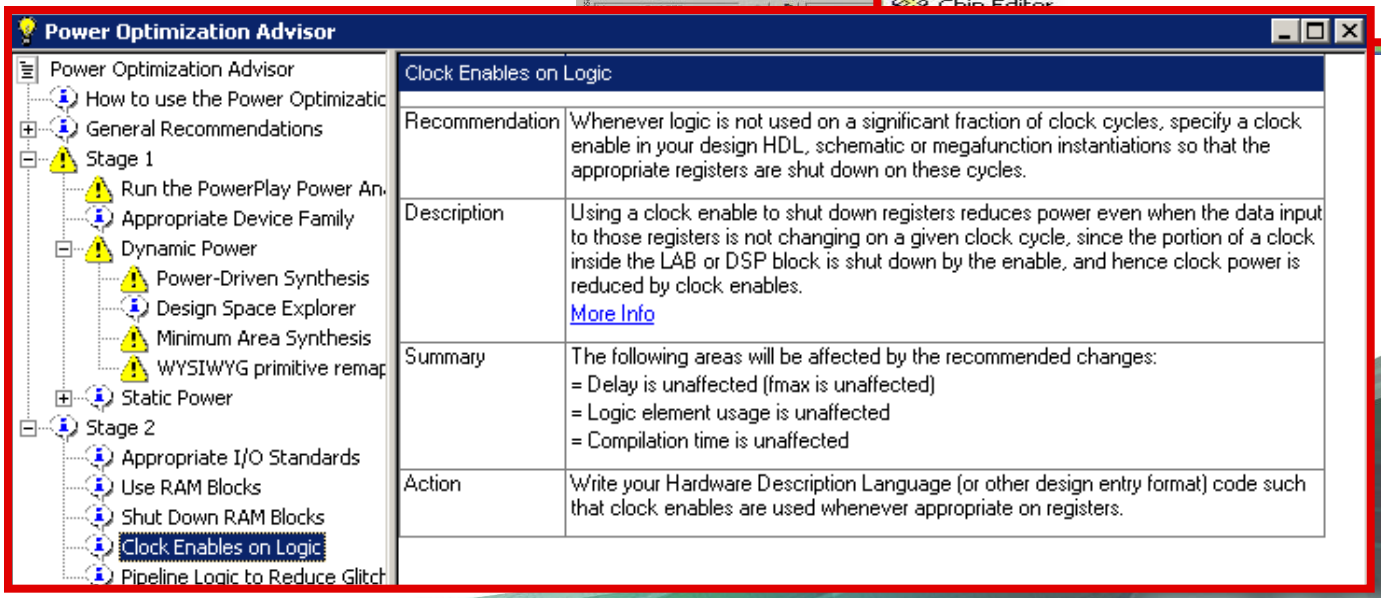
Power Optimization Advisor

- Recommended settings and design changes to minimize power



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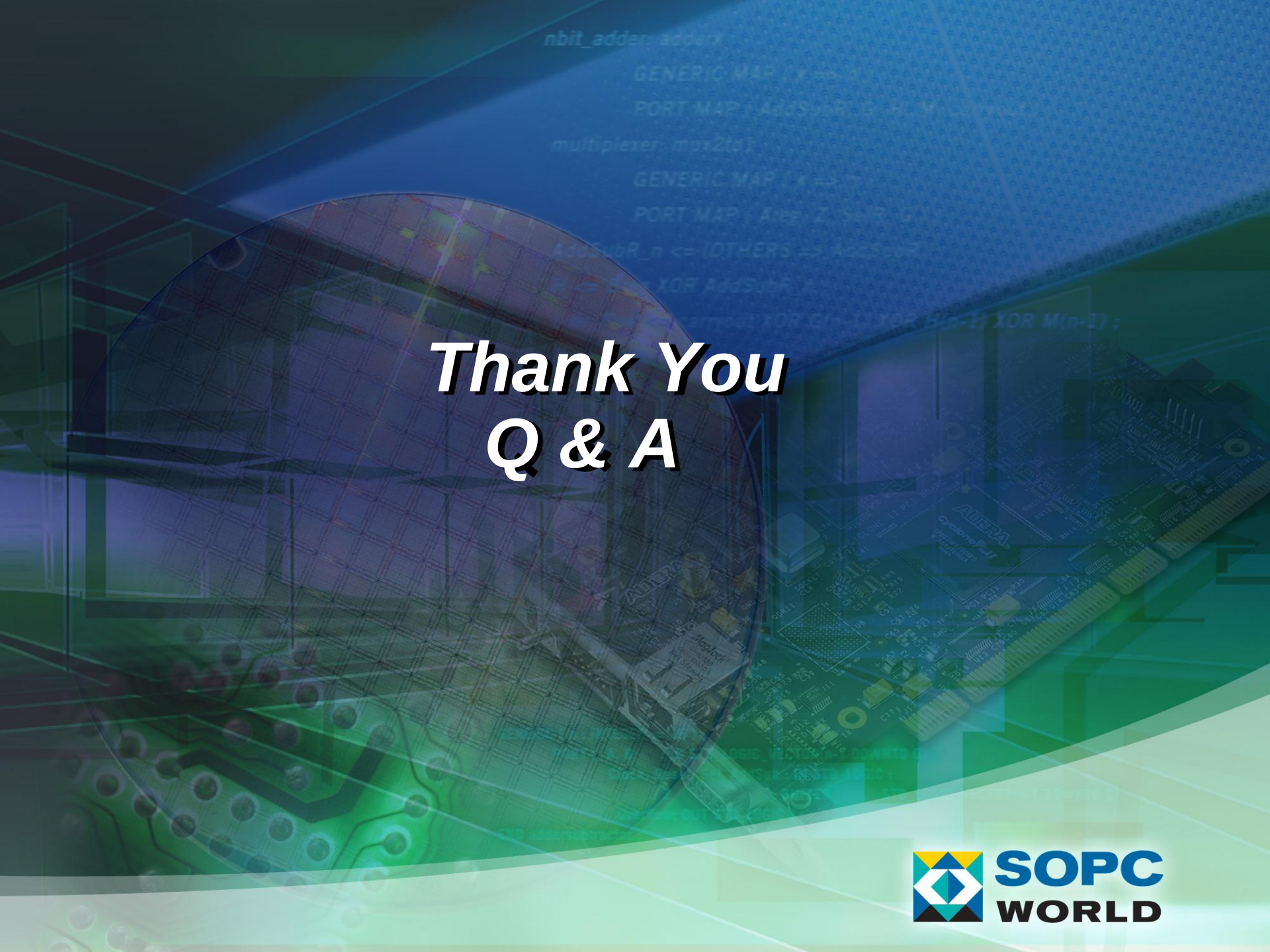
Conclusion

- Power optimization and power management is becoming a critical aspect of system design
- Stratix III FPGAs provide innovative programmable power technology for power optimization
- Industry leading PowerPlay tools from Altera enable optimum power


Thank You
Q & A
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