Implement System-on-a-Programmable Chip (SOPC) Designs in Minutes

The Embedded Revolution

- FPGAs offer a new way to develop embedded systems
- Widely adopted:
  - Over 15,000 development kits shipped
  - Many products already in the market

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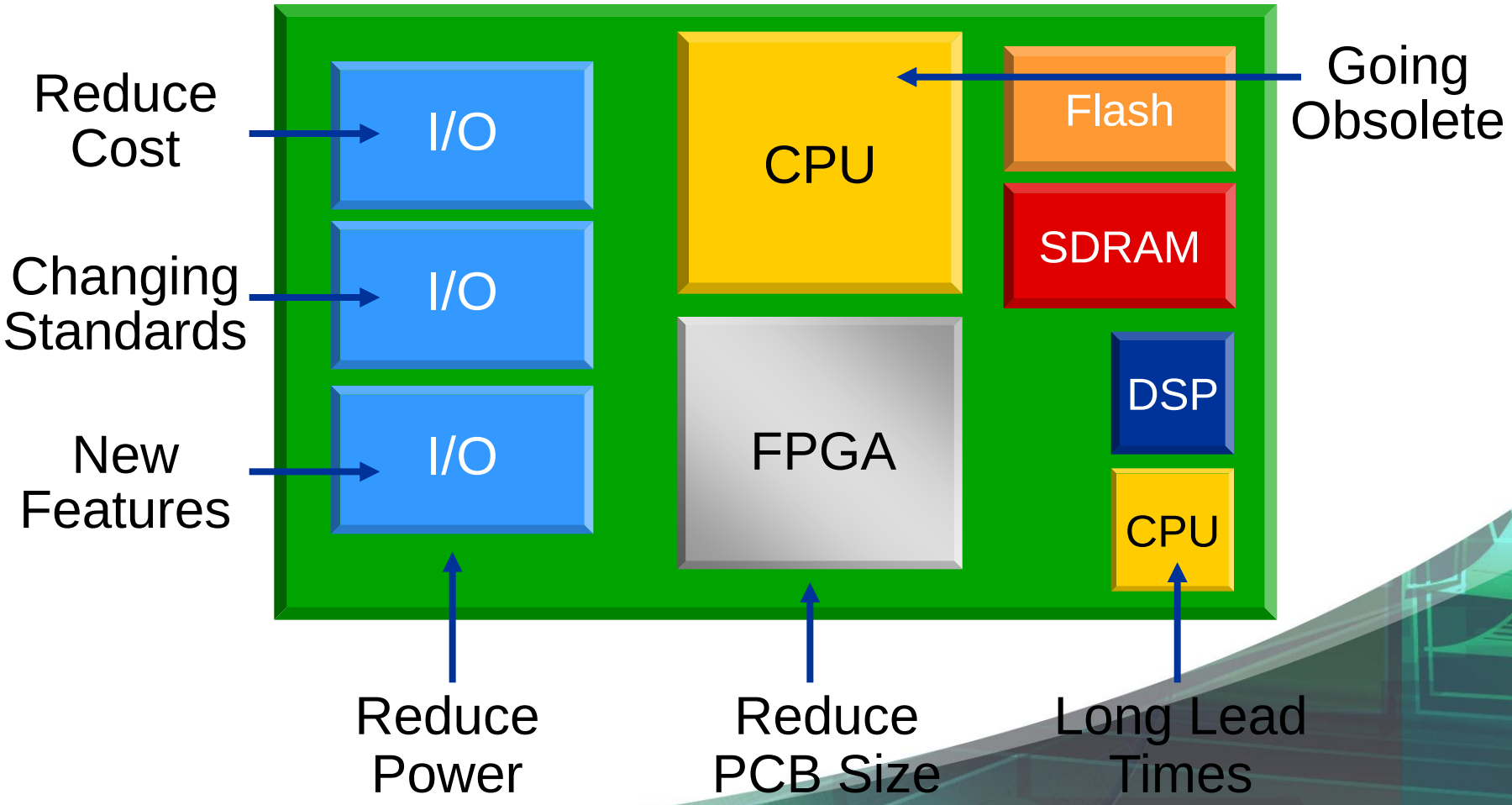
Embedded Design Challenges



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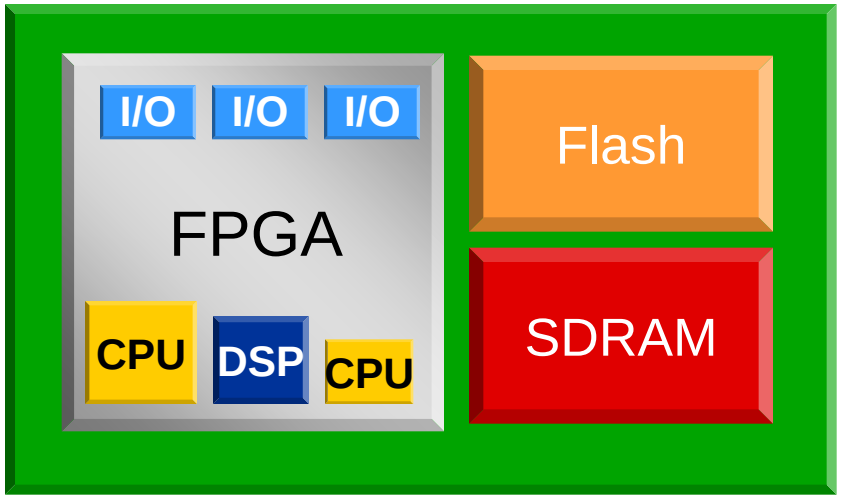
FPGA-Based Solution



- Reduced power
- Reduced cost
- Reduced PCB size
- Easier to support
- Add new features
- Smaller B.O.M.
- Obsolescence protected

System Level Integration

Replace External Devices with Programmable Logic

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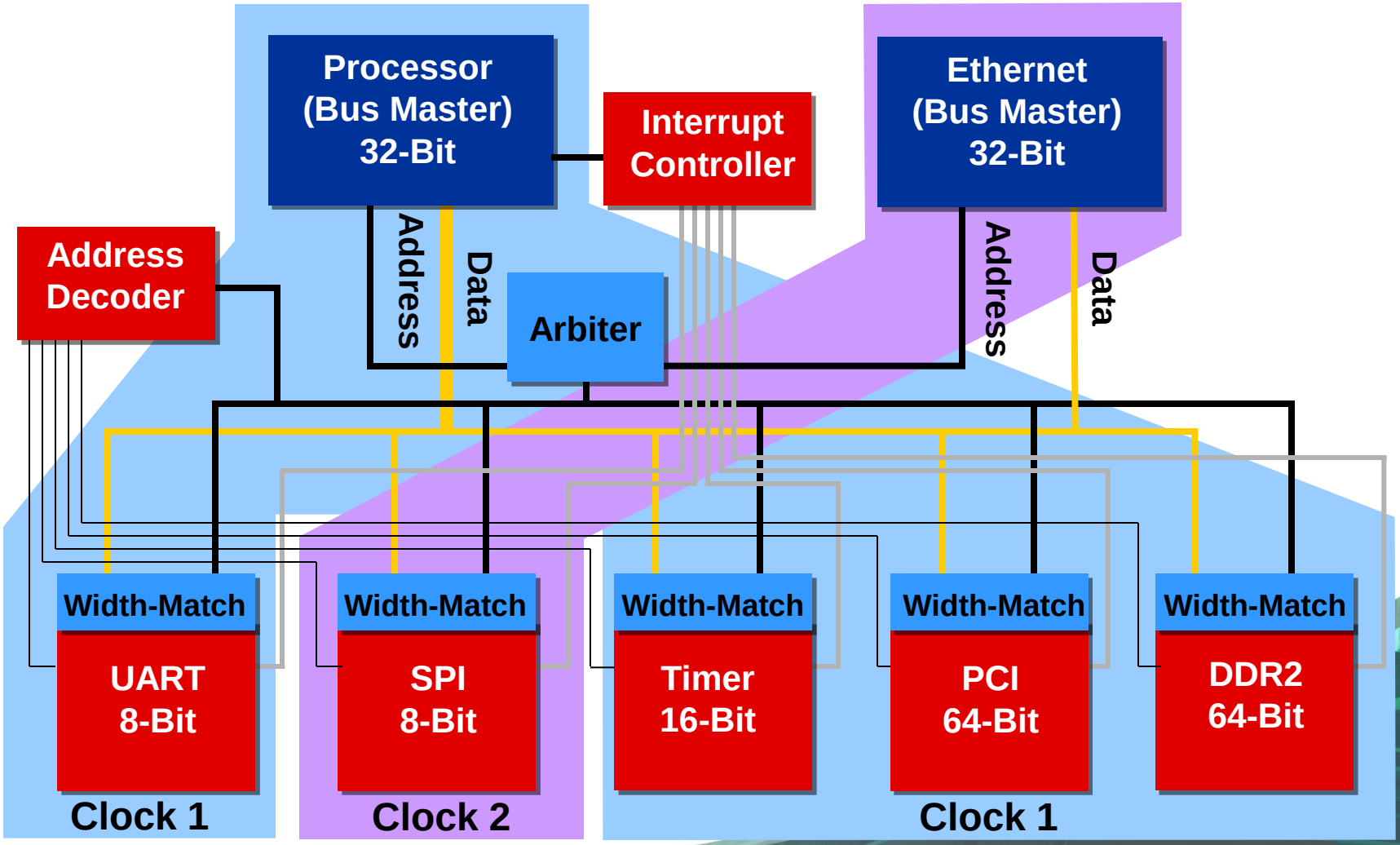
Traditional System Design



Large Amount of Complexity

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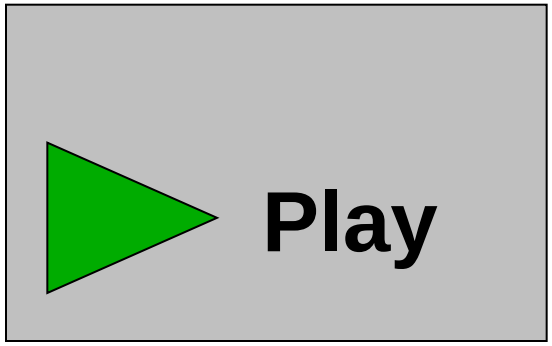
What If…

Processor
(Bus Master)
32-Bit

Ethernet
(Bus Master)
32-Bit



UART
8-Bit

SPI
8-Bit

Timer
16-Bit

PCI
64-Bit

DDR2
64-Bit

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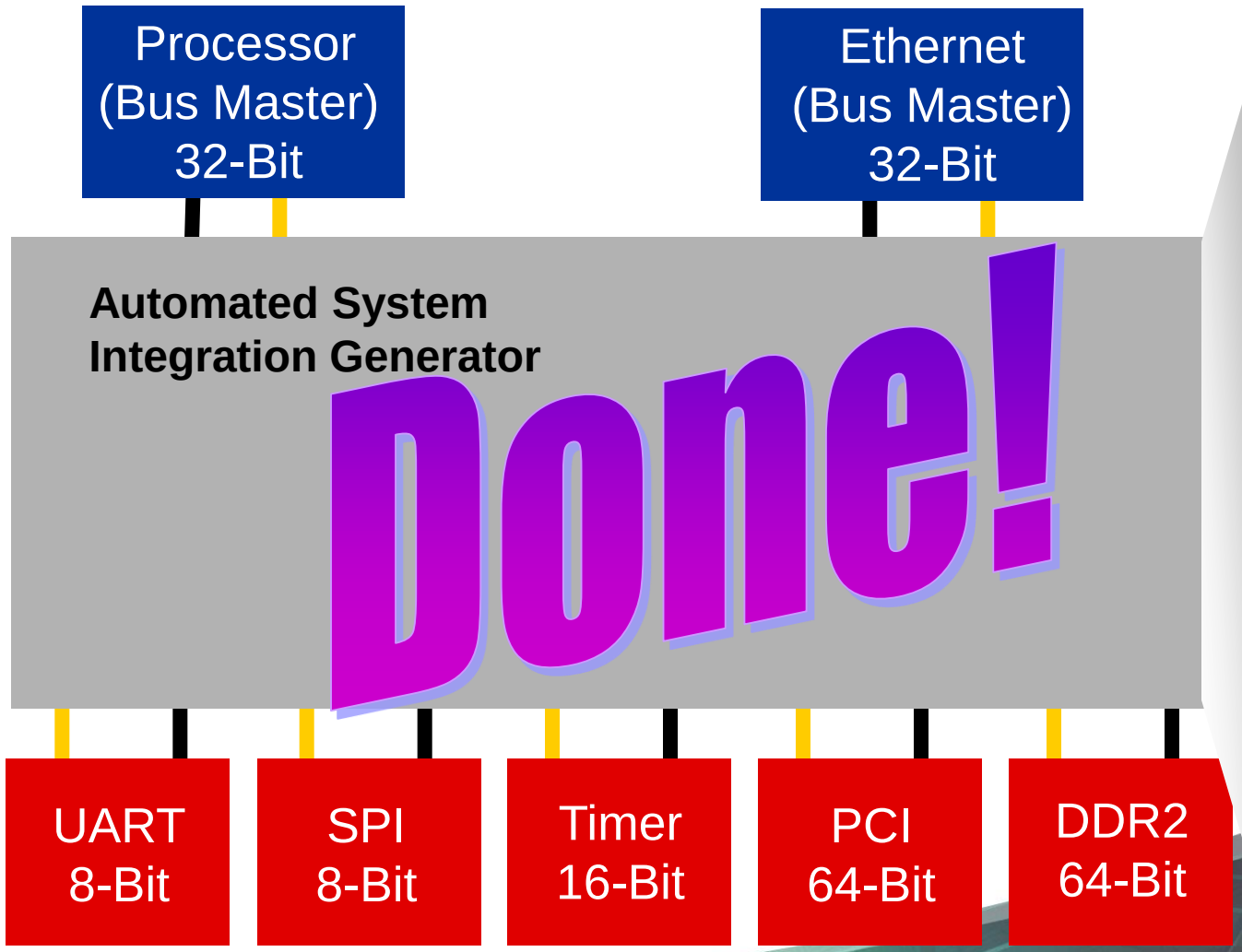
What If…



Basic Integration

- Bus width matching
- Address decoding
- Interrupt controller

Advanced Tasks

- Arbitration logic
- Clock domain crossing
- Burst transfers

Optimization

- System throughput
- Resource utilization

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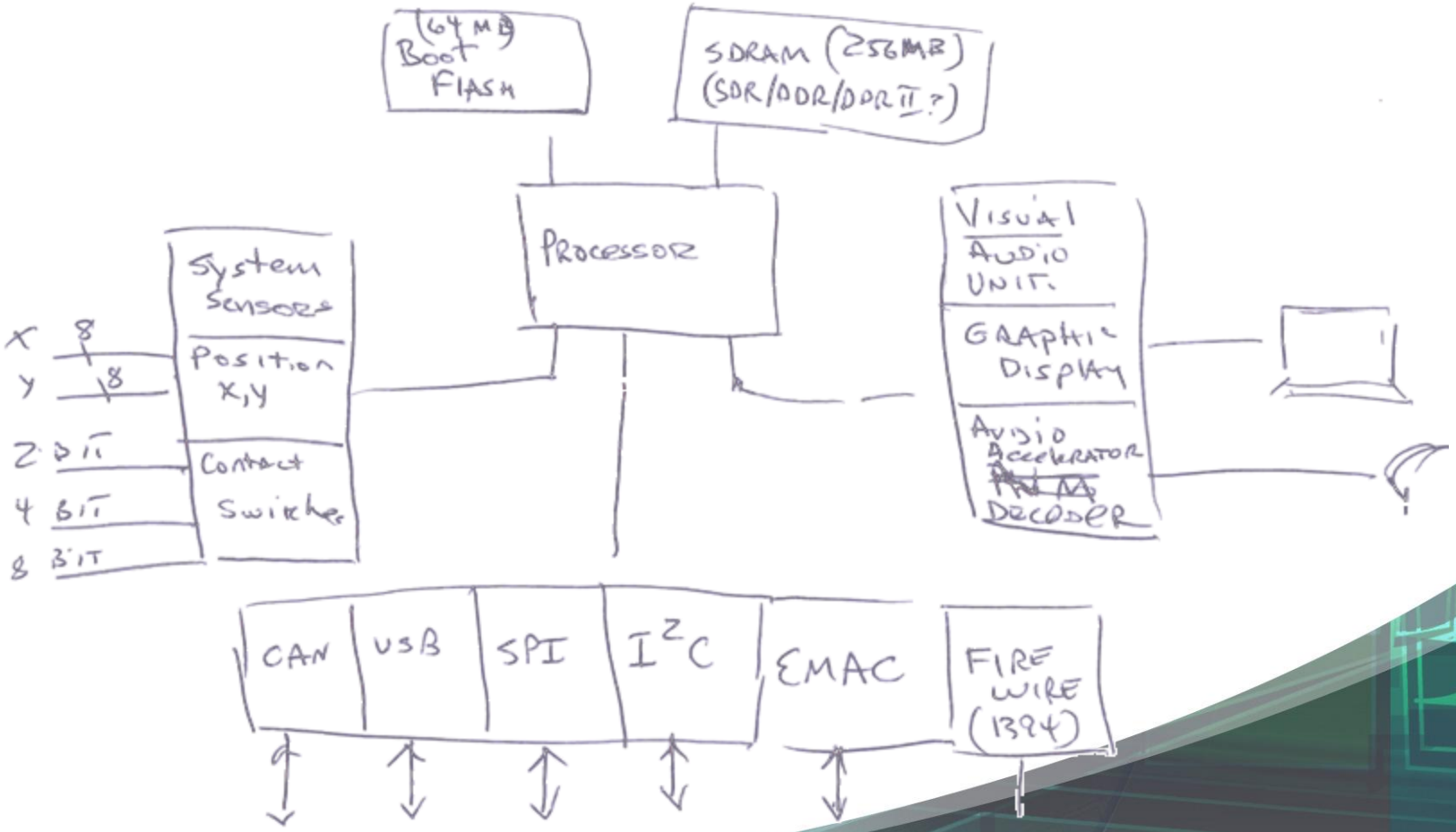
System Concept



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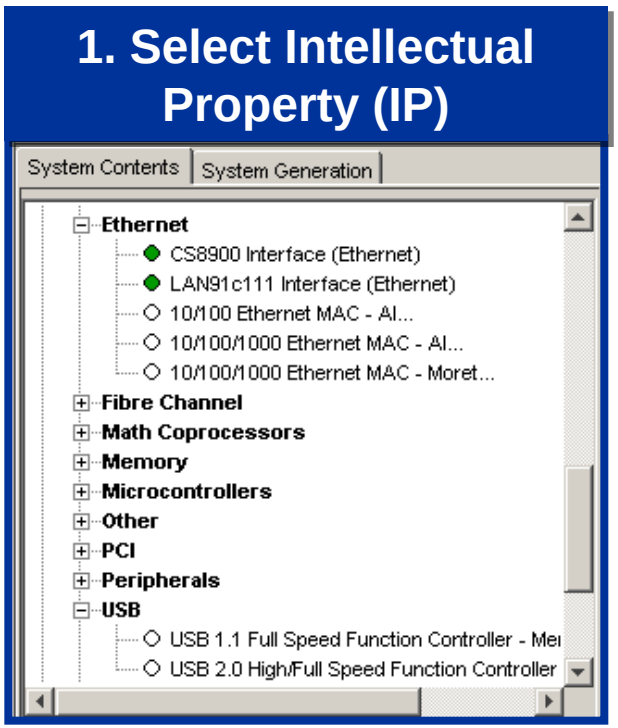
Design Flow

1. Select Intellectual Property (IP)



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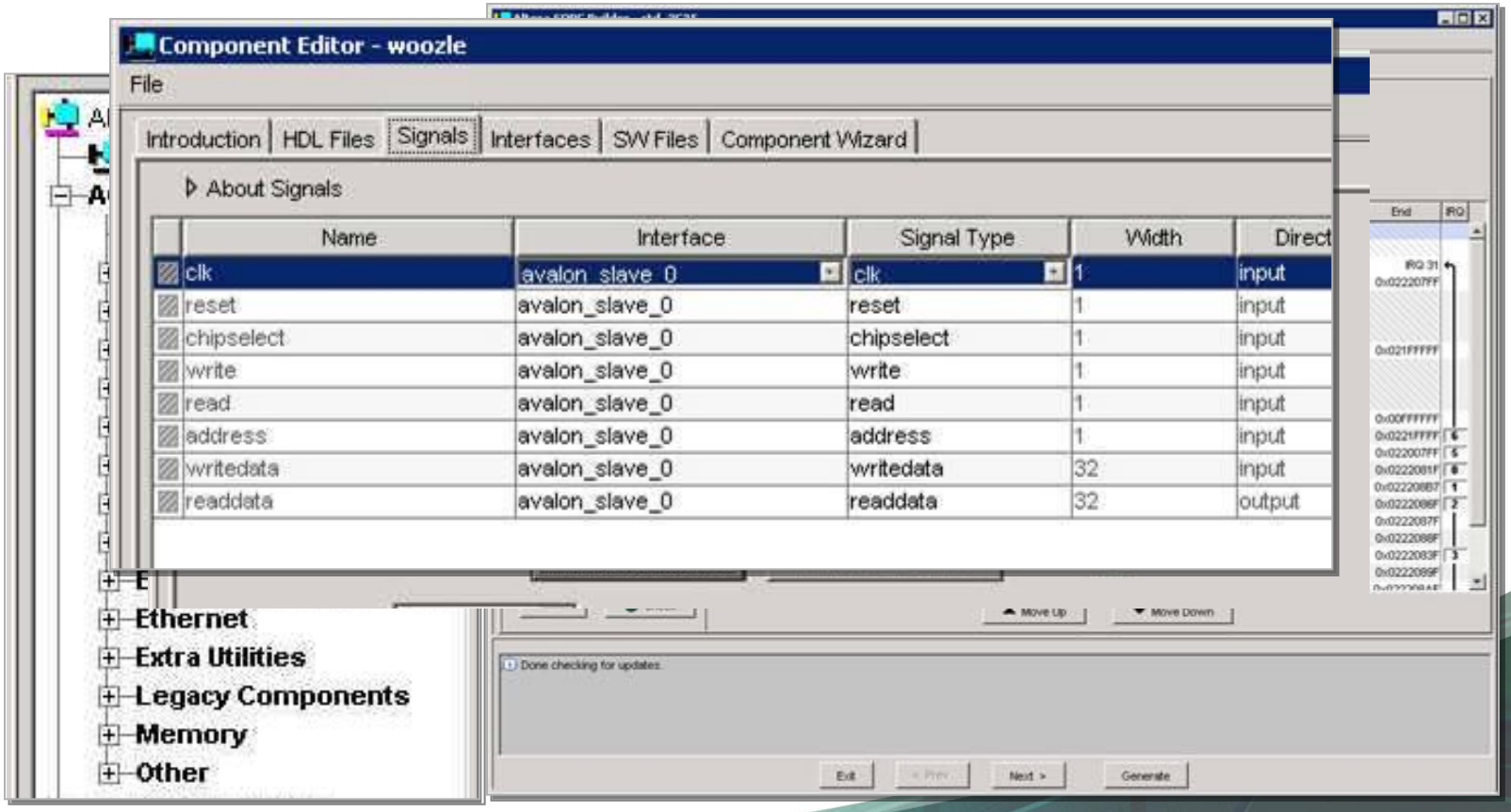
Component Selection

- Extensive portfolio of system components
- Component editor imports user-designed functions



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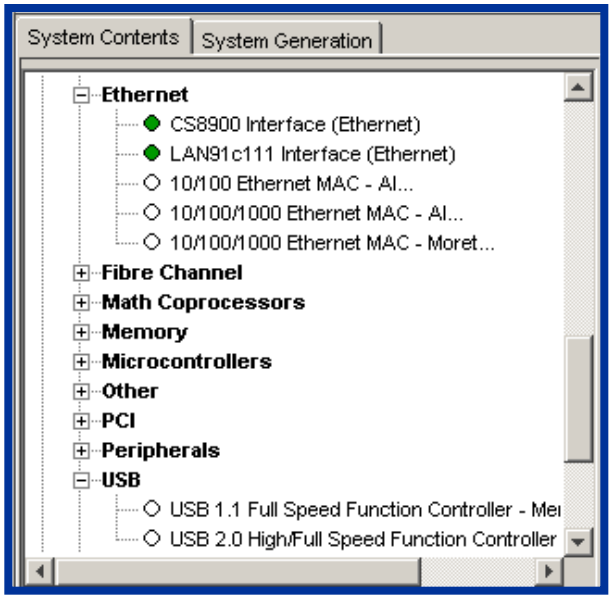
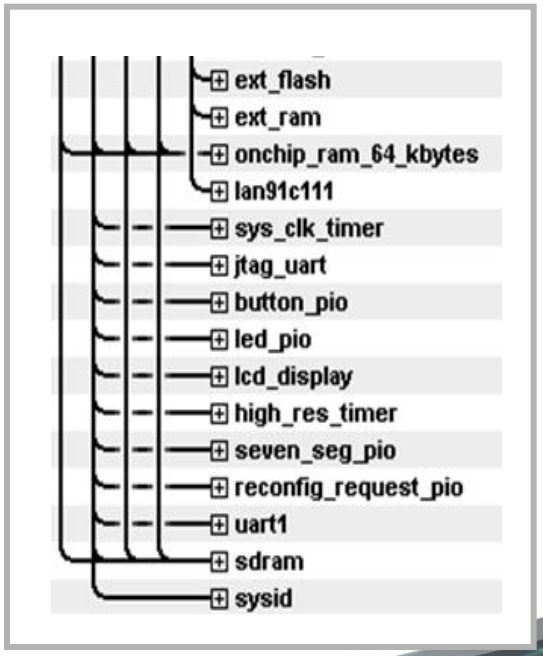
Design Flow

1. Select IP



2. Select Connections



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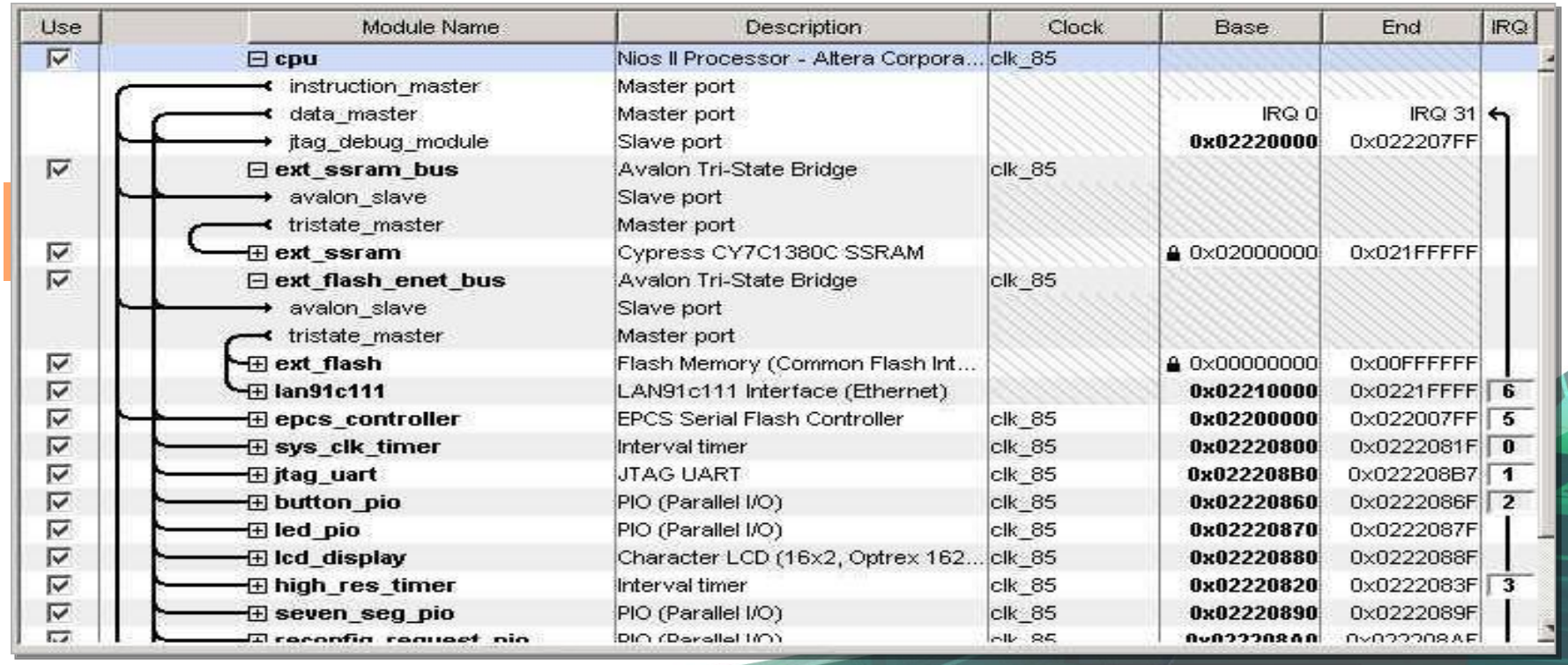
System Editor

Connection Panel

Clock Domains

Address Map

Interrupt Controller (IRQ) Priorities



Use	Module Name	Description	Clock	Base	End	IRQ
☑	cpu	Nios II Processor - Altera Corpora...	clk_85			
	instruction_master	Master port				
	data_master	Master port		IRQ 0	IRQ 31	
	jtag_debug_module	Slave port		0x02220000	0x022207FF	
☑	ext_ssram_bus	Avalon Tri-State Bridge	clk_85			
	avalon_slave	Slave port				
	tristate_master	Master port				
☑	ext_ssram	Cypress CY7C1380C SSRAM		0x02000000	0x021FFFFF	
☑	ext_flash_enet_bus	Avalon Tri-State Bridge	clk_85			
	avalon_slave	Slave port				
	tristate_master	Master port				
☑	ext_flash	Flash Memory (Common Flash Int...		0x00000000	0x00FFFFFF	
☑	lan91c111	LAN91c111 Interface (Ethernet)		0x02210000	0x0221FFFF	6
☑	epcs_controller	EPCS Serial Flash Controller	clk_85	0x02200000	0x022007FF	5
☑	sys_clk_timer	Interval timer	clk_85	0x02220800	0x0222081F	0
☑	jtag_uart	JTAG UART	clk_85	0x022208B0	0x022208B7	1
☑	button_pio	PIO (Parallel I/O)	clk_85	0x02220860	0x0222086F	2
☑	led_pio	PIO (Parallel I/O)	clk_85	0x02220870	0x0222087F	
☑	lcd_display	Character LCD (16x2, Optrex 162...	clk_85	0x02220880	0x0222088F	
☑	high_res_timer	Interval timer	clk_85	0x02220820	0x0222083F	3
☑	seven_seg_pio	PIO (Parallel I/O)	clk_85	0x02220890	0x0222089F	
☑	reconfig_request_pio	PIO (Parallel I/O)	clk_85	0x022208A0	0x022208AF	

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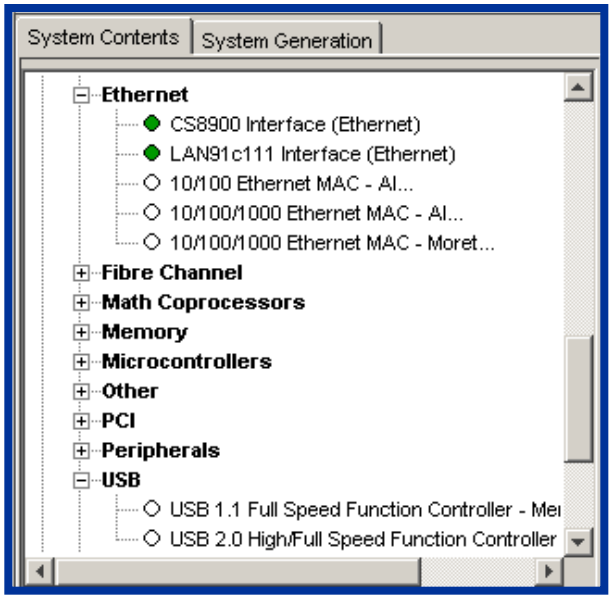
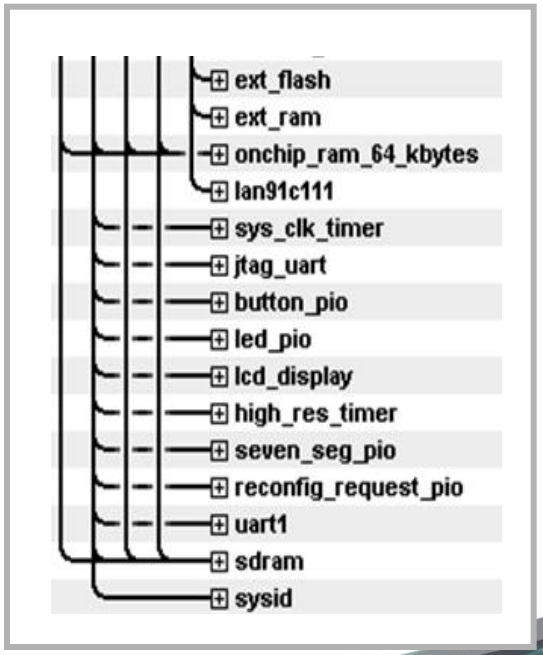
Design Flow

1. Select IP



2. Select Connections



3. Generate System

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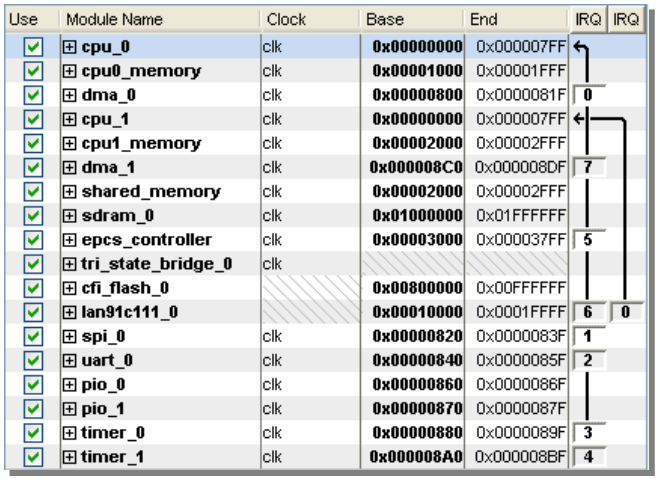
Integrated Hardware/Software Flow

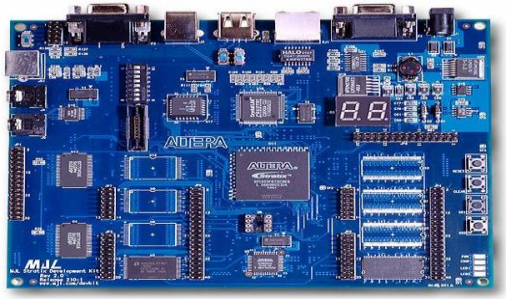


SOPC Builder

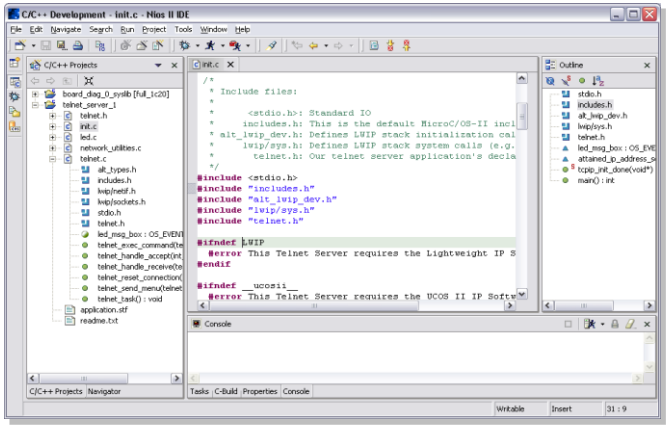
System RTL

QUARTUS® II

Hardware Image



System Description File



Software Image

- Application creation
- Custom library

Nios II Integrated Development Environment (IDE)

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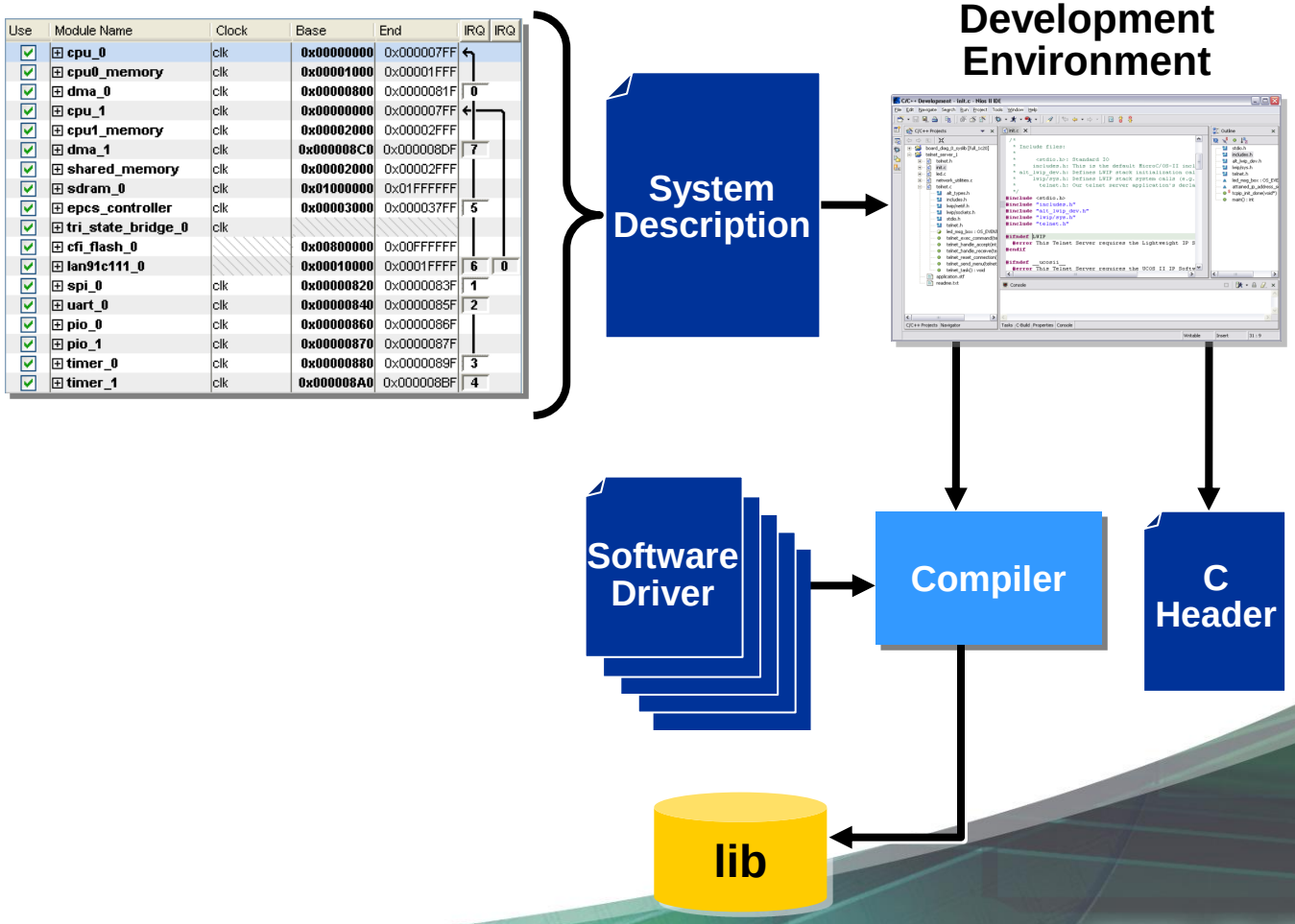
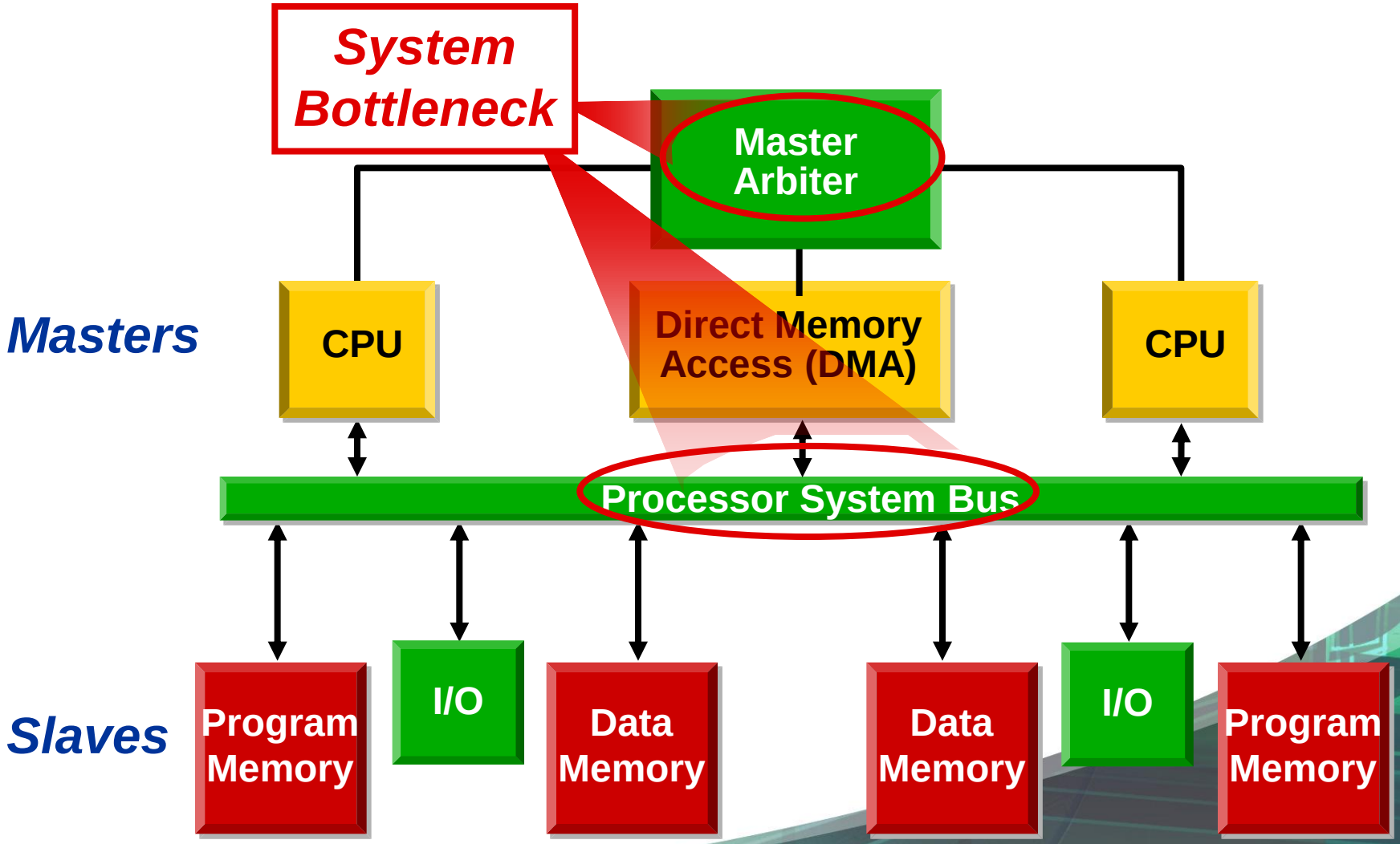
Automatic Board Support Package (BSP) Generation



Avalon® System Interconnect

- Automatically generated for system
- Switches connect components – not a bus
- Slave side arbitration
  - Enables concurrent accesses
- Avalon functions
  - Arbitration
  - Multiplexing
  - Address decoding
  - Wait-state generation
  - Dynamic bus sizing

Traditional Bus Interconnect



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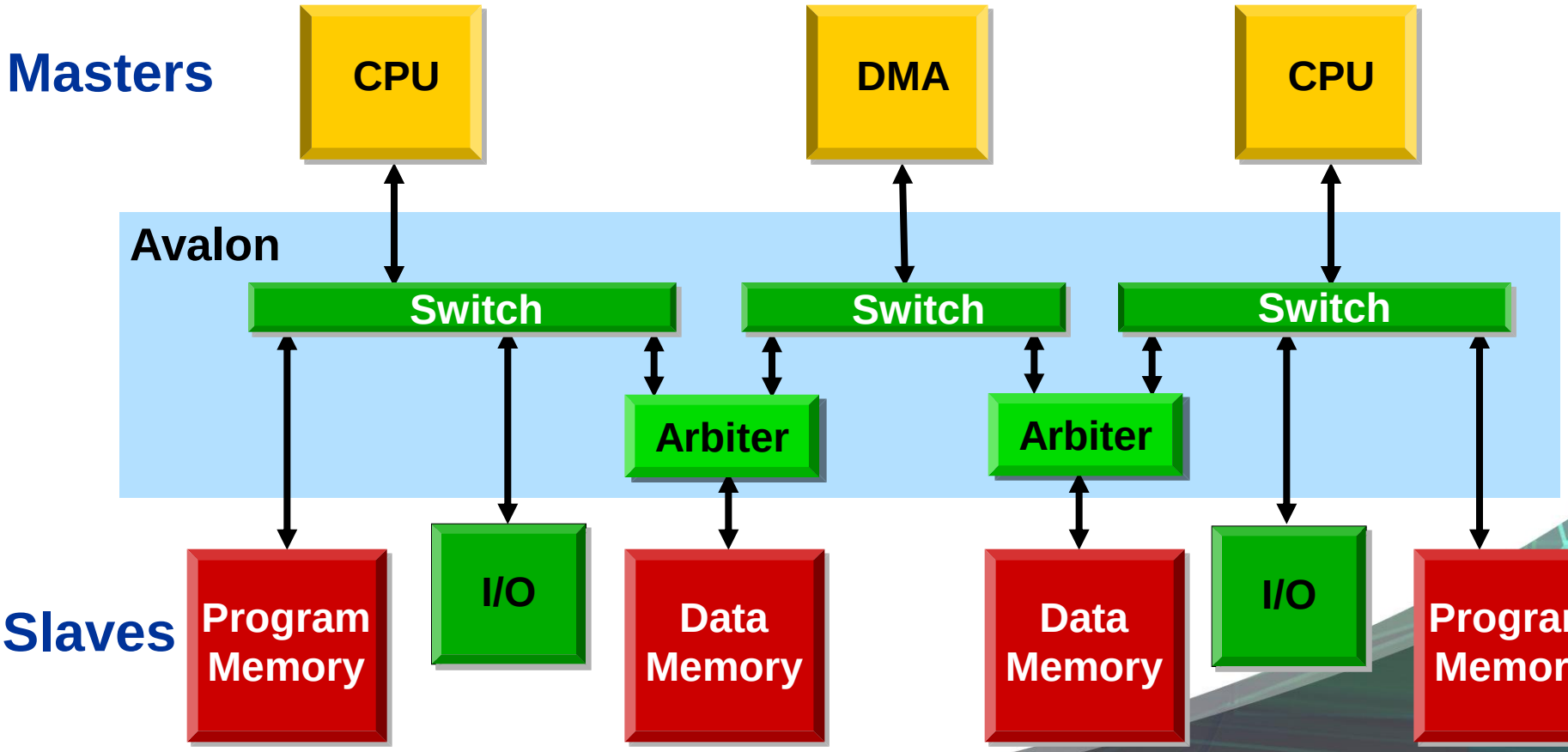
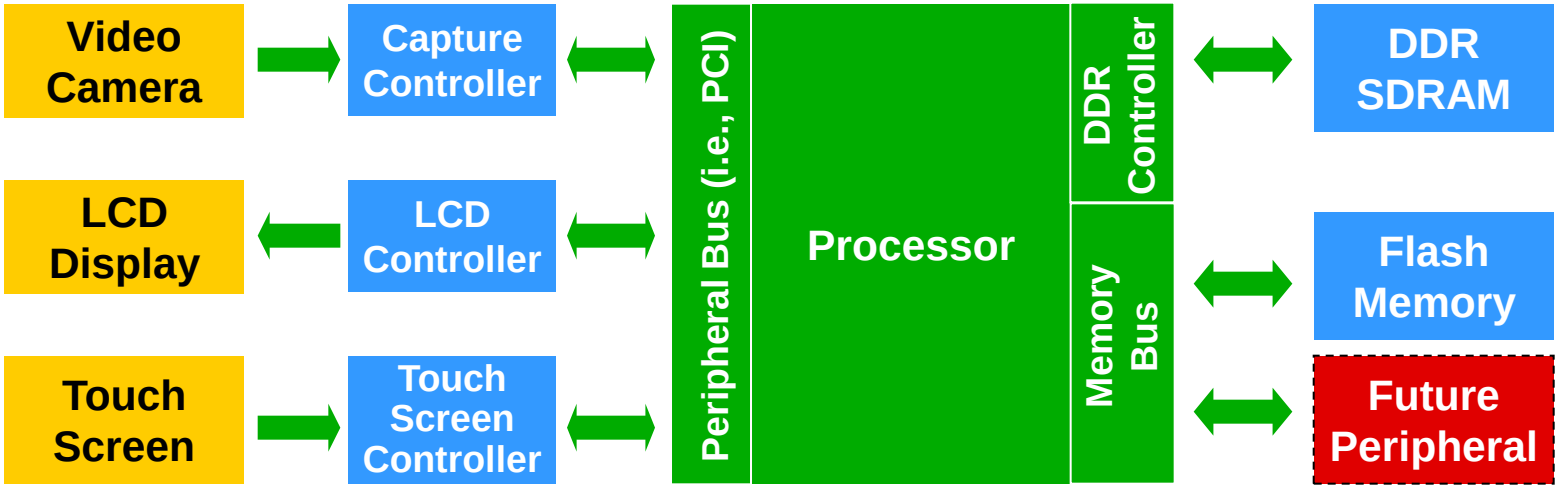
System Interconnect



Video System Built "Conventionally"



- Typical system construction steps
  1. Specify external components and peripherals
  2. Select processor with right…
     - Performance needed for application
     - Peripheral controller bus for controllers (i.e., PCI, PCIX, etc.)
     - Memory controllers

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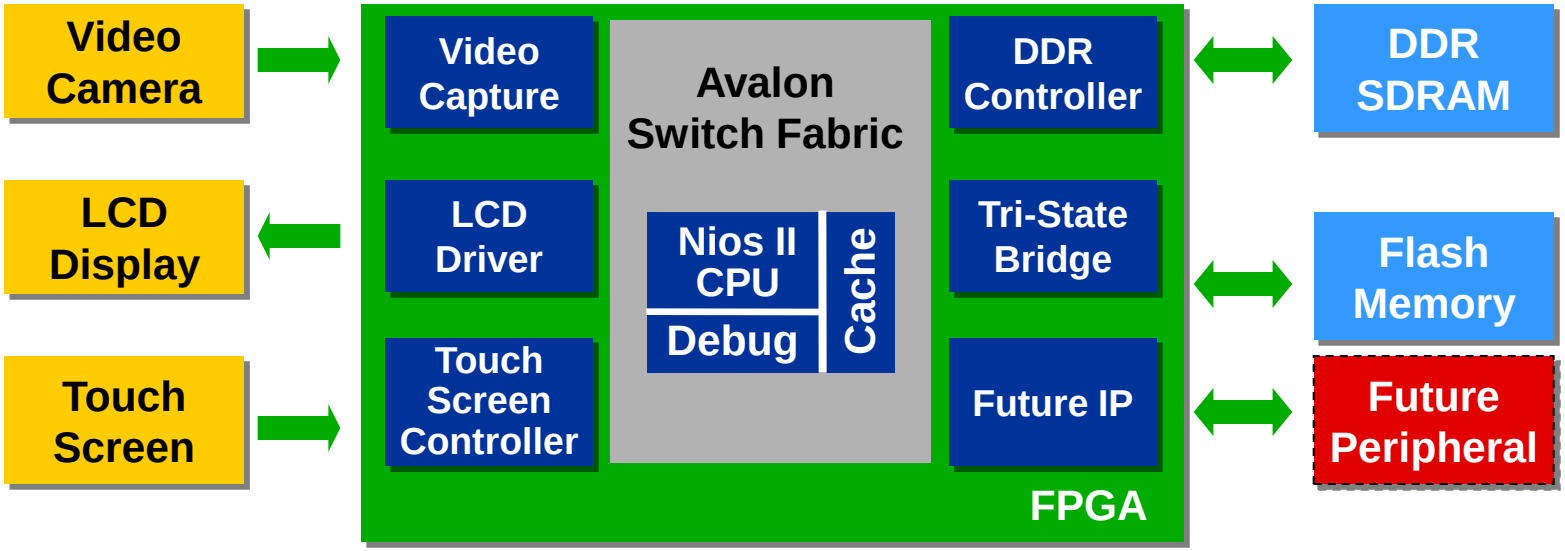
Video System Built With SOPC Builder



- SOPC Builder-based construction
  1. Specify external components and peripherals
  2. Use SOPC Builder to:
     - Add peripherals and memory controllers
     - Add Nios II CPU
     - Configure system for maximum performance

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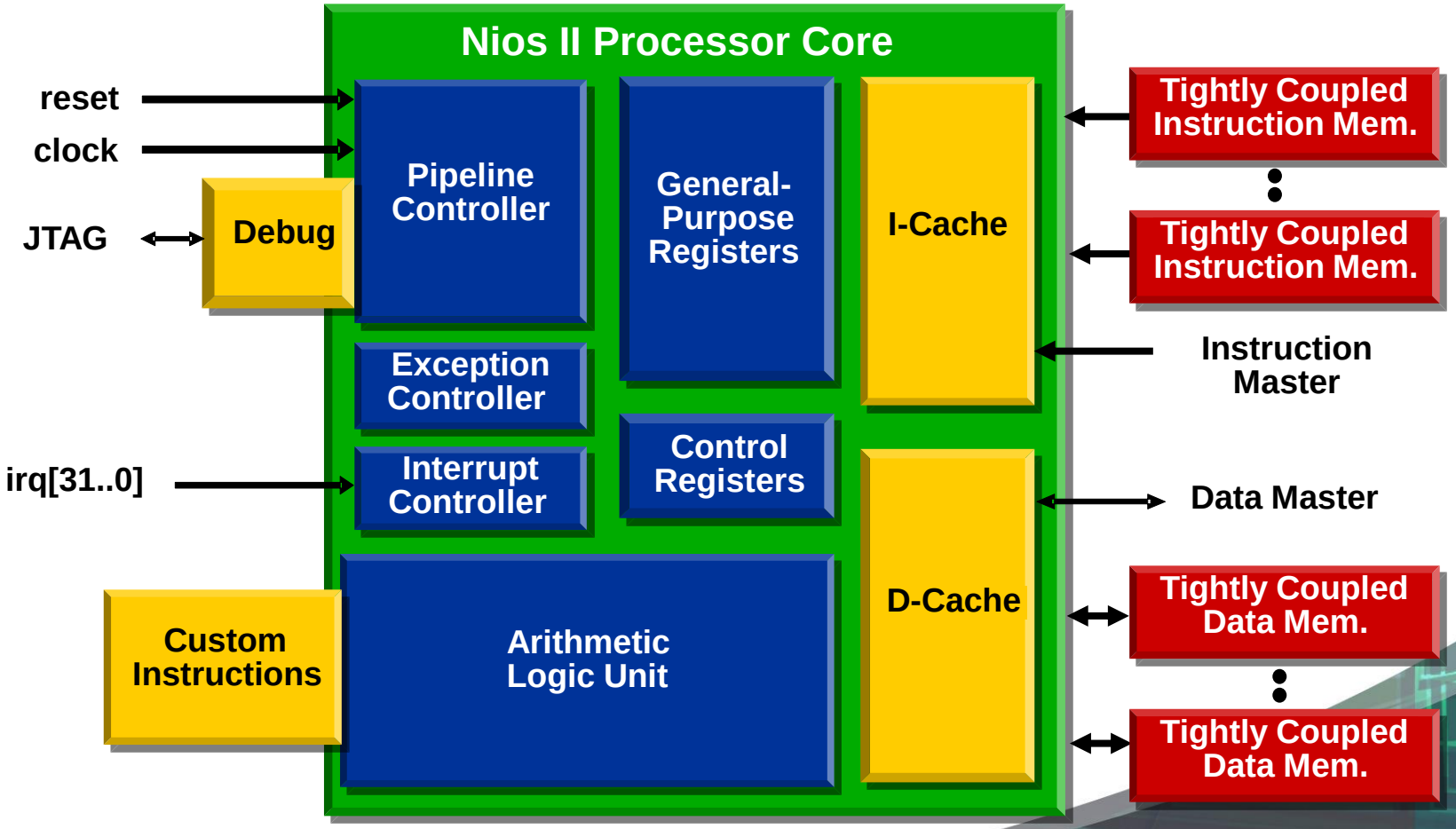
Nios II Processor Block Diagram



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Nios II: Classic RISC CPU

- Soft-core reconfigurable CPU
- Classic RISC architecture optimized for FPGA
  - 32-bit instruction set
  - 32-bit data path
  - 32 general-purpose registers
  - 3 instruction formats
  - 82 instructions
    - Instruction set is not configurable
    - Provides code compatibility for all implementations
  - Up to 256 custom instructions
  - 3 operand instructions (2 source, 1 destination)
  - Optional multiply and divide
- Strong performance (up to 225 DMIPS)

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NOW What We're Going to Do…

- Build a system with SOPC Builder
  - Add and parameterize peripherals
    - Nios II processor
    - Memory (DDR SDRAM)
    - Timer
    - JTAG UART
    - Pulse width modulator (custom peripheral)
  - Connect peripherals with Avalon switch fabric
  - Configure system for operation

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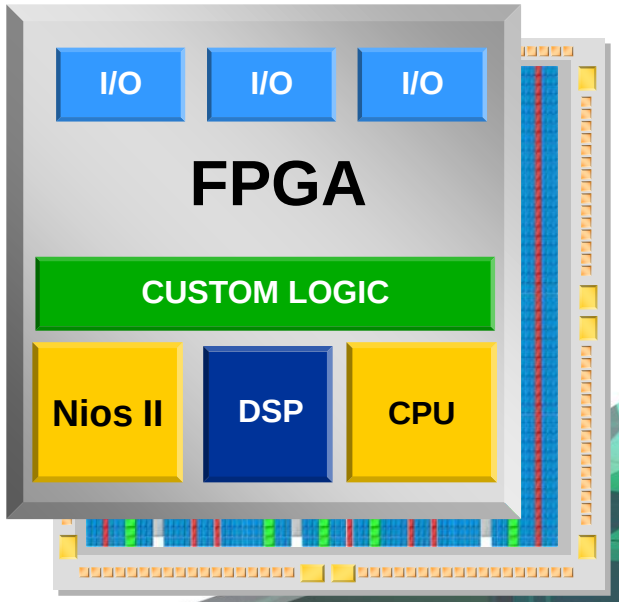
Benefits of FPGA-Based Embedded Systems

- FPGA hardware, configurable processor and automated system generation deliver:
  - Fast development time
  - Reduced costs
  - Product differentiation
    - High performance
    - New features
  - Product life management
    - Protection against obsolescence
    - In-field upgrades



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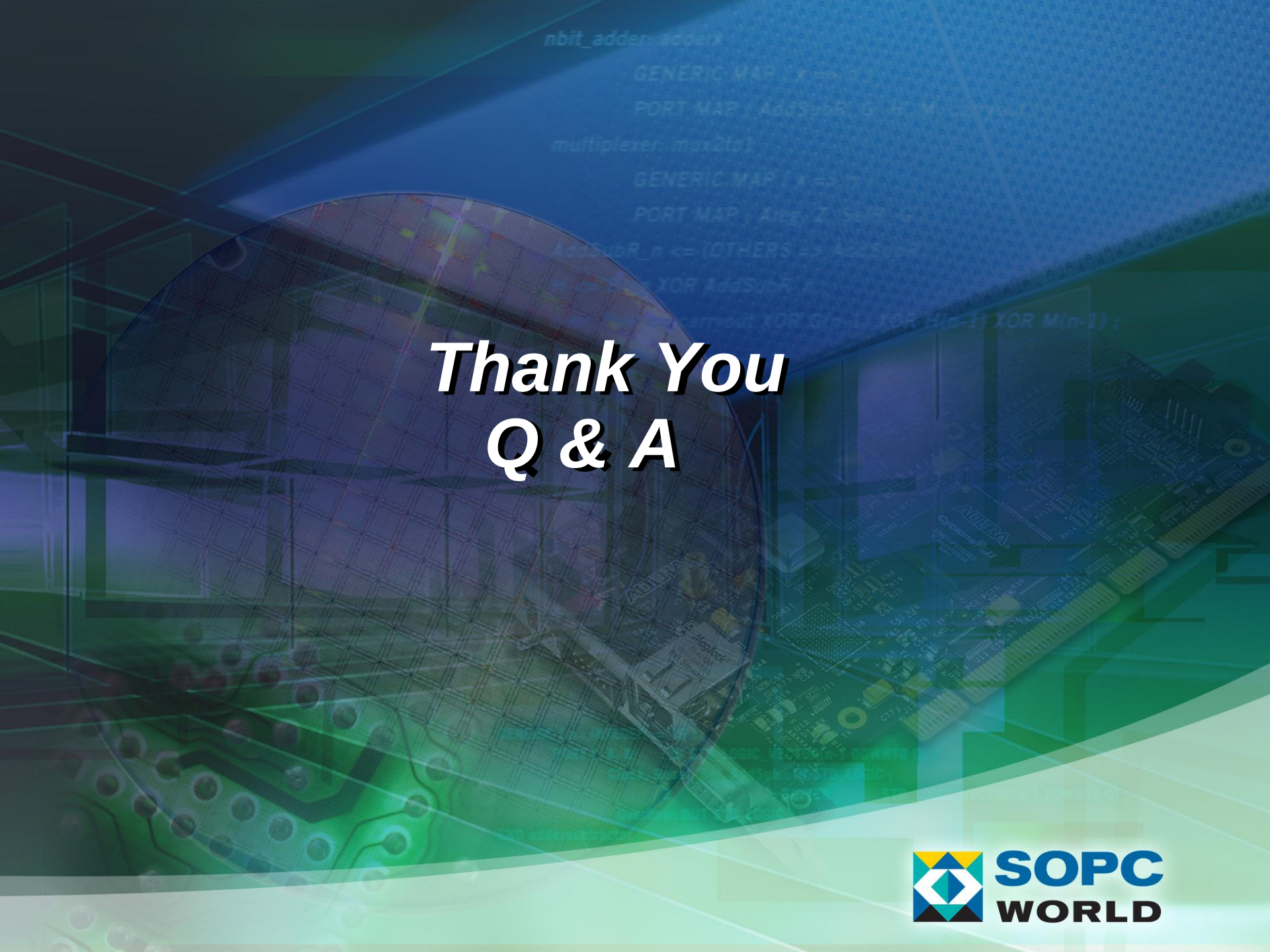
Thank You
Q & A
SOPC
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