The New Frontier of System Design

How to Efficiently Conquer All Your Design Needs

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The Designer's Environment

challenges

- Meeting functionality specifications
- Meeting power targets
- Meeting performance targets
- Staying on schedule and on budget
- Needing to design different products–high end, low cost

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Things You Know…

starting a project

- Specifications
- Cost target
- Schedule requirements

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But Do You Really Know….

what's behind the scenes?

- Will marketing make last-minute changes to the specification?
- Will the competitive landscape change?
  - New entrants
  - Disruptive technologies
- Will customer requirements change?

…….Will you be able to meet your schedule and budget?

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What If…

- You had the flexibility to react to market changes and evolving specifications while still meeting your schedule?
- You could lower your development cost, yet maintain your differentiation?
- You could significantly increase your system performance while staying within the power budget?
- You could move from prototyping to low-cost production in a risk-free and cost-effective way?
- You could use one development software tool for all your design needs?

the perfect scenario

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flexibility

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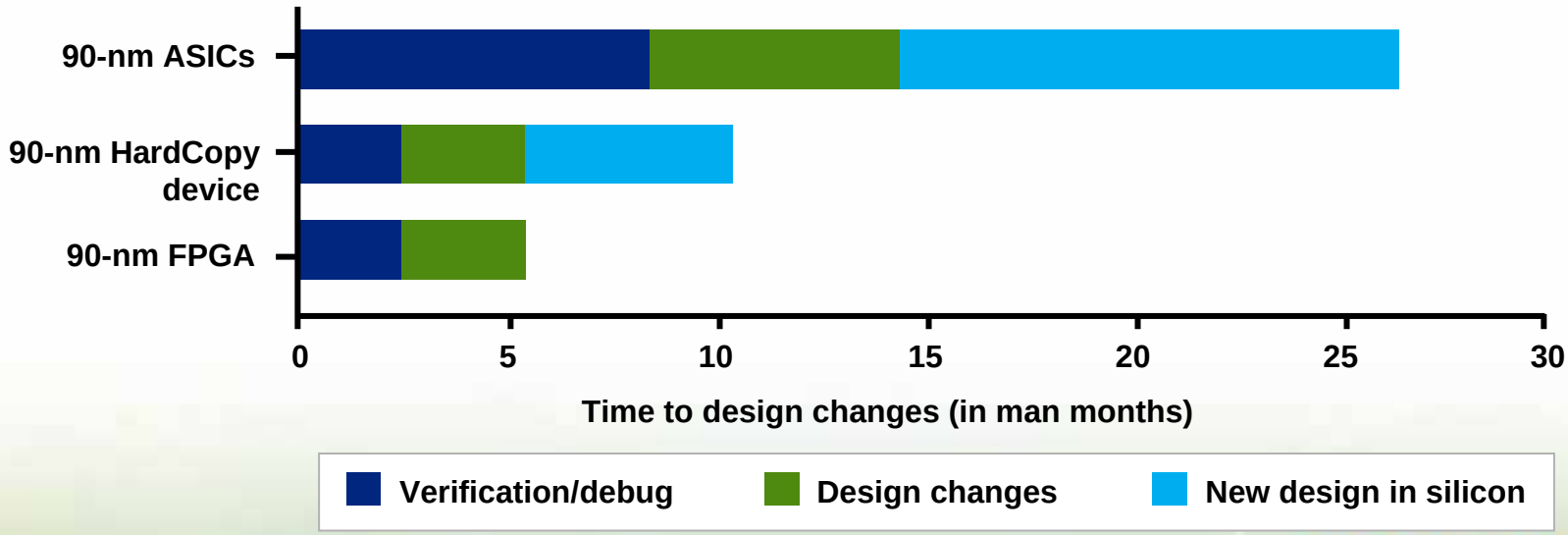
Timeline for Design Changes

	90-nm FPGA*	90-nm HardCopy® Device*	90-nm ASICs*
Verification/Debug	2	2	8
Design Changes	3	3	6
New Design in Silicon	0	5	12
Accomodating design changes	~5	~10	~27

* All values are in man months



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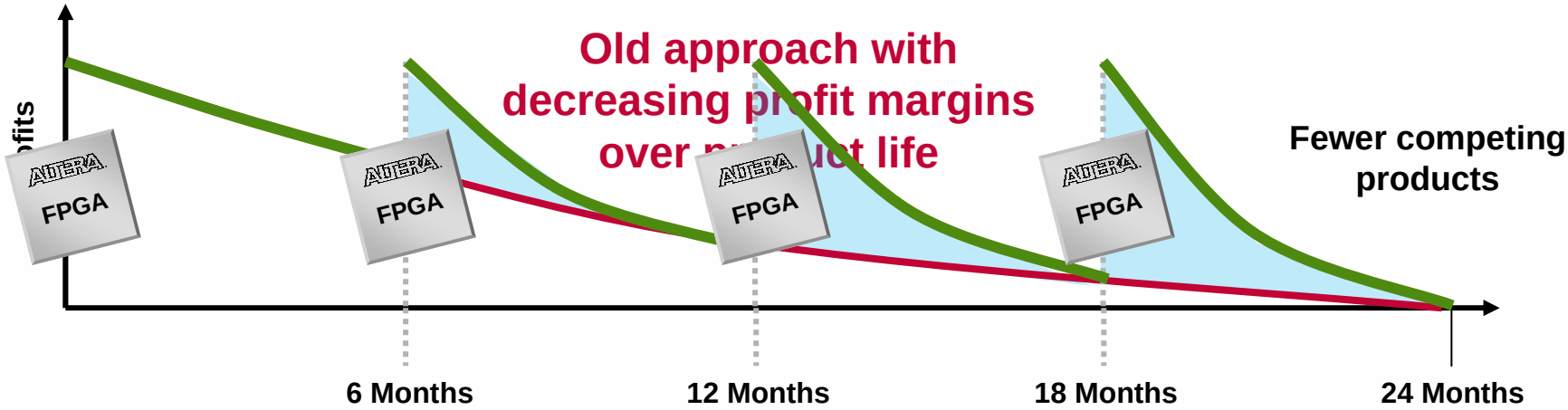
Solving the Development Dilemma

New product generation 1

Add new features and enhance profit margins

Enhance profit margins generation 2

Add new features and enhance profit margins



Design a Single Platform for Multiple Sizes and Resolutions

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development cost

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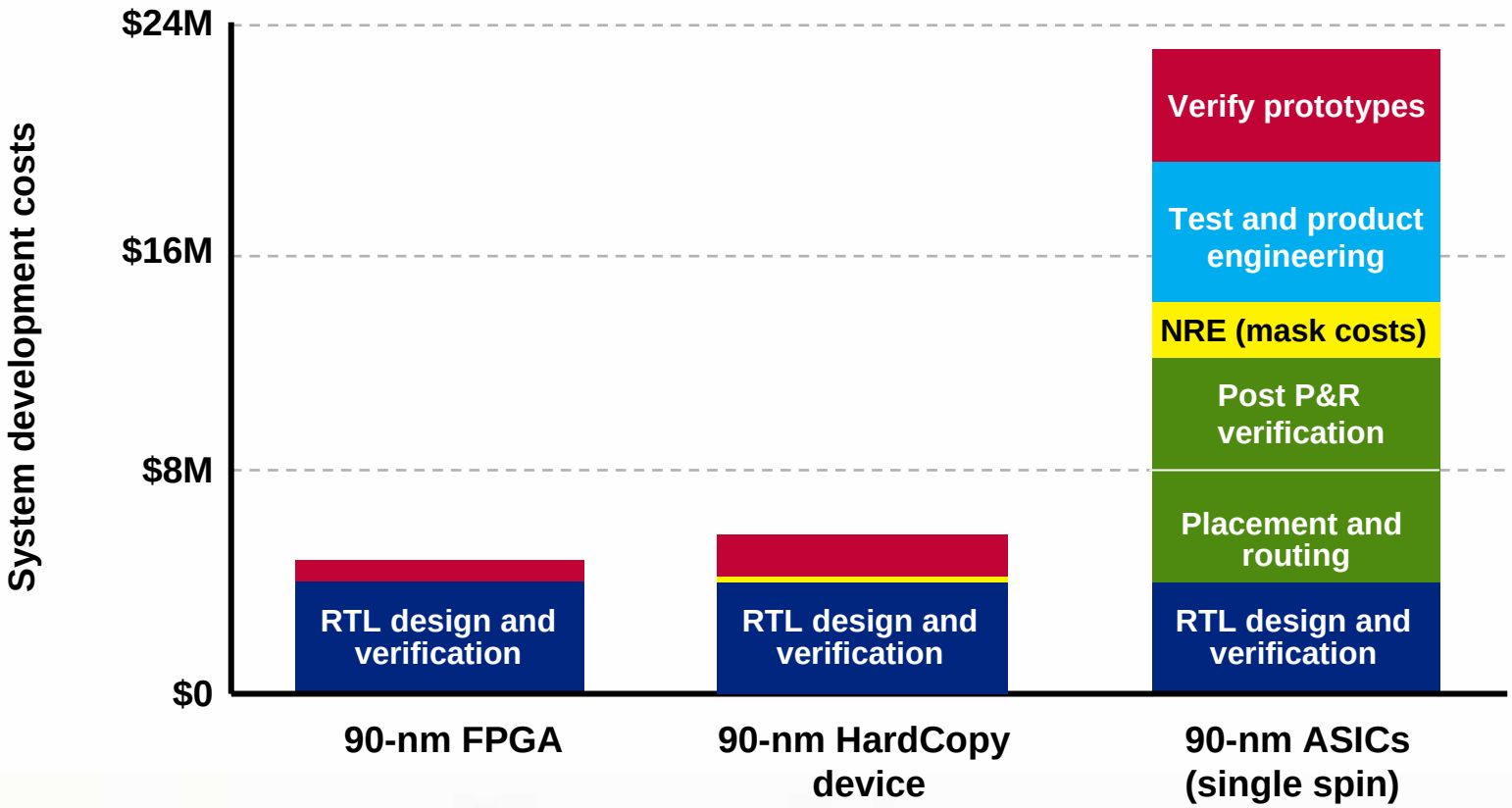
System Development Cost



75% Lower System Development Costs With FPGAs

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performance/power

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Stratix III FPGAs: Power & Performance Advantage

- Stratix® III performance advantage
  - 25 percent faster than nearest competing FPGAs
  - Maximum internal clock speed: 600 MHz
  - On-chip RAM: 600 MHz
  - Digital signal processing (DSP) blocks @ 550 MHz
  - Supports 400-MHz DDR3 and DDR2 external memory
  - Supports 1.25-Gbps LVDS
- Stratix III power advantage
  - Programmable Power Technology
  - Selectable core voltage
  - Quartus® II PowerPlay power analysis and optimization tool

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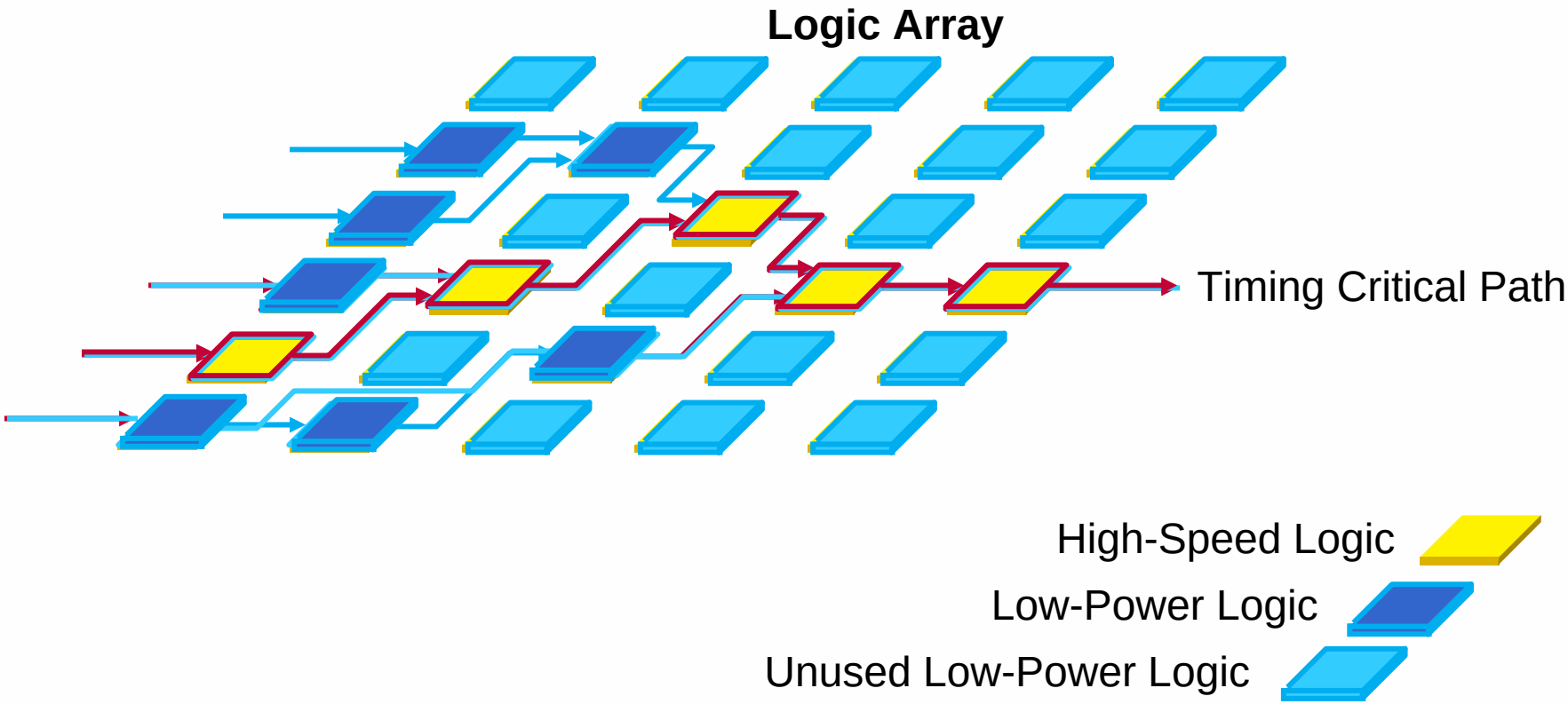
Programmable Power Technology



Performance Where You Need It, Lowest Power Everywhere Else

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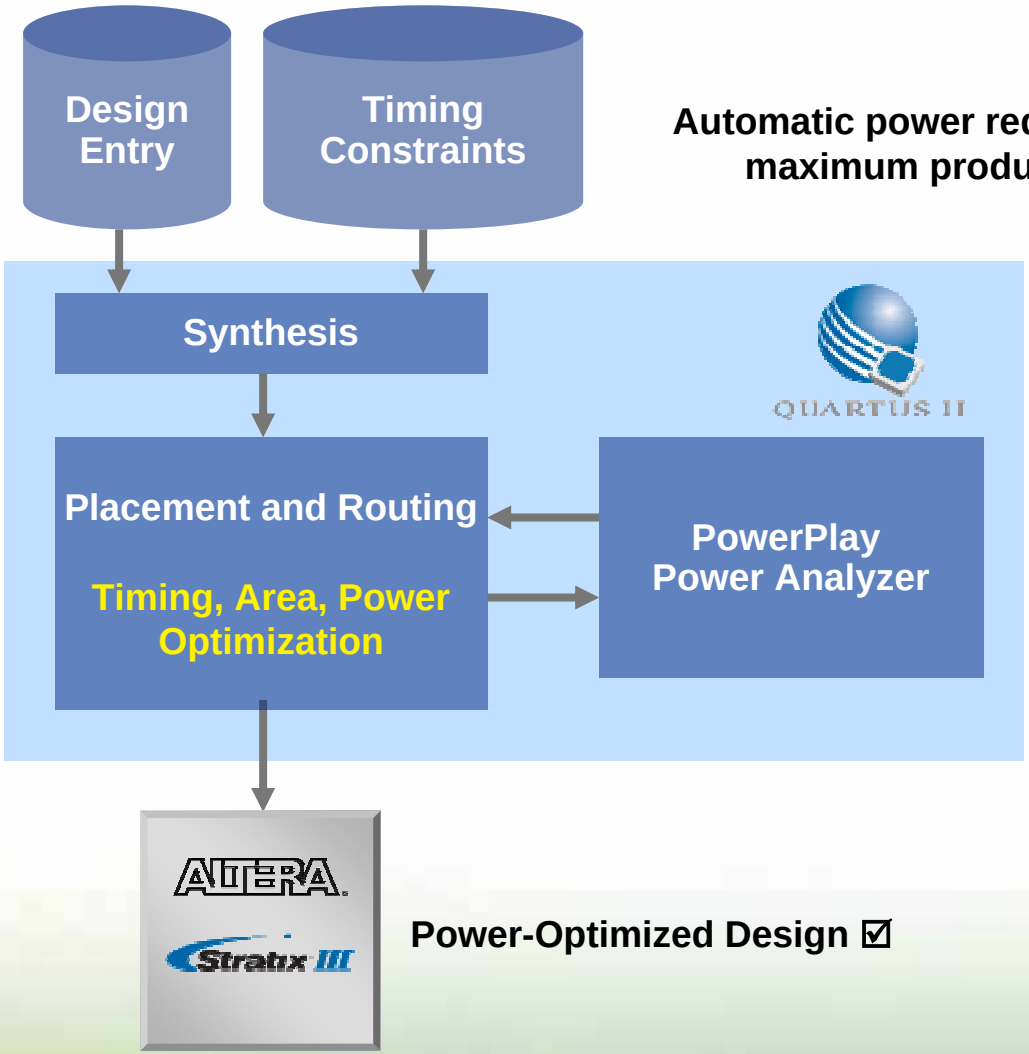
Automated by Quartus II Software



Automatic power reduction for maximum productivity

Timing is always met, then power optimizations are implemented

Power-Optimized Design ☑

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production

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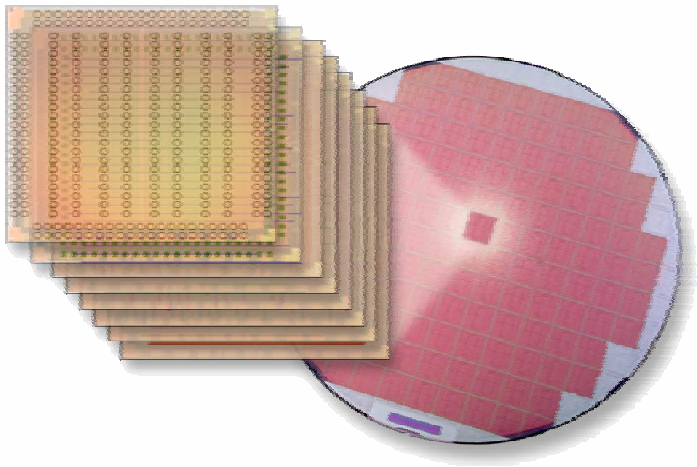
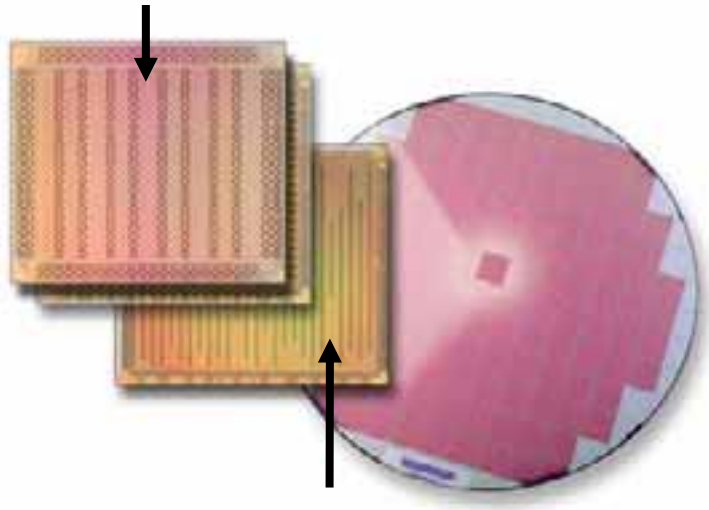
Benefits of a Structured ASIC

Standard cell ASIC:
All layers are custom



Full set of masks
for standard-cell ASIC

Structured ASIC:
Customization through top layers



Base layer

Structured ASICs Minimize NRE and Turnaround Times

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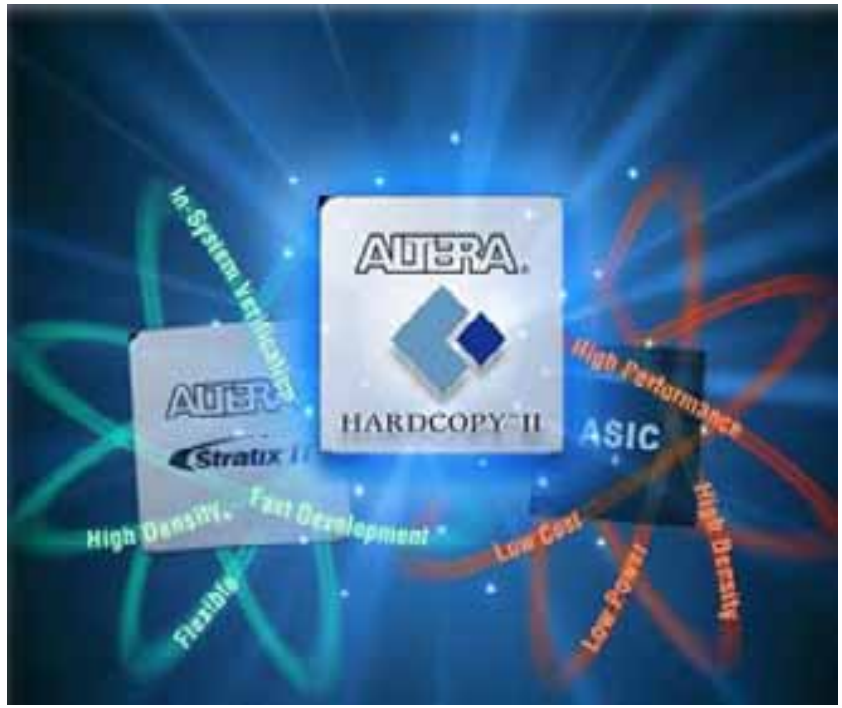
HardCopy Structured ASICs

- Advanced process (90 nm) delivers dramatically lower cost
  - $15 for 1M ASIC gates
  - Up to 90% cost reduction
- Dramatic power reduction
  - Up to 90% lower static power
  - Up to 50% lower active power
- Up to 2.2M ASIC gates
- Seamless migration from Stratix series FPGA



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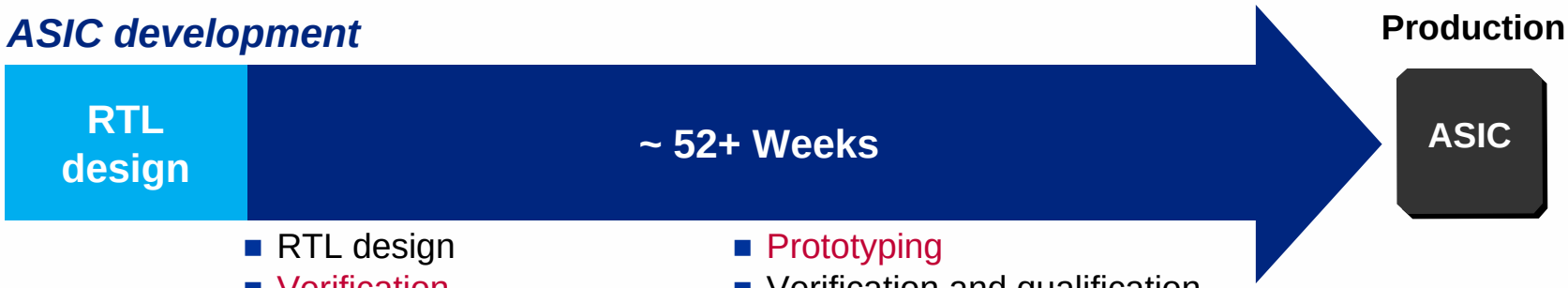
Faster Time-to-Market, Period

ASIC development



- RTL design
- Verification
- Placement and routing + final verification

- Prototyping
- Verification and qualification
- Production

HardCopy development

- RTL design
- Migration
- Prototyping

***With in-system verification**

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tools

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Quartus II Design Software

- Everything you need to design for Altera® programmable logic devices
- #1 design software for performance and productivity
- Only complete development package supporting FPGA, CPLD, and structured ASICs
- Delivering *fastest* time to market
  - Easiest to use
  - Best-in-class technology
  - Partnerships with industry leaders

Easiest Path From Design Ideas to Reality

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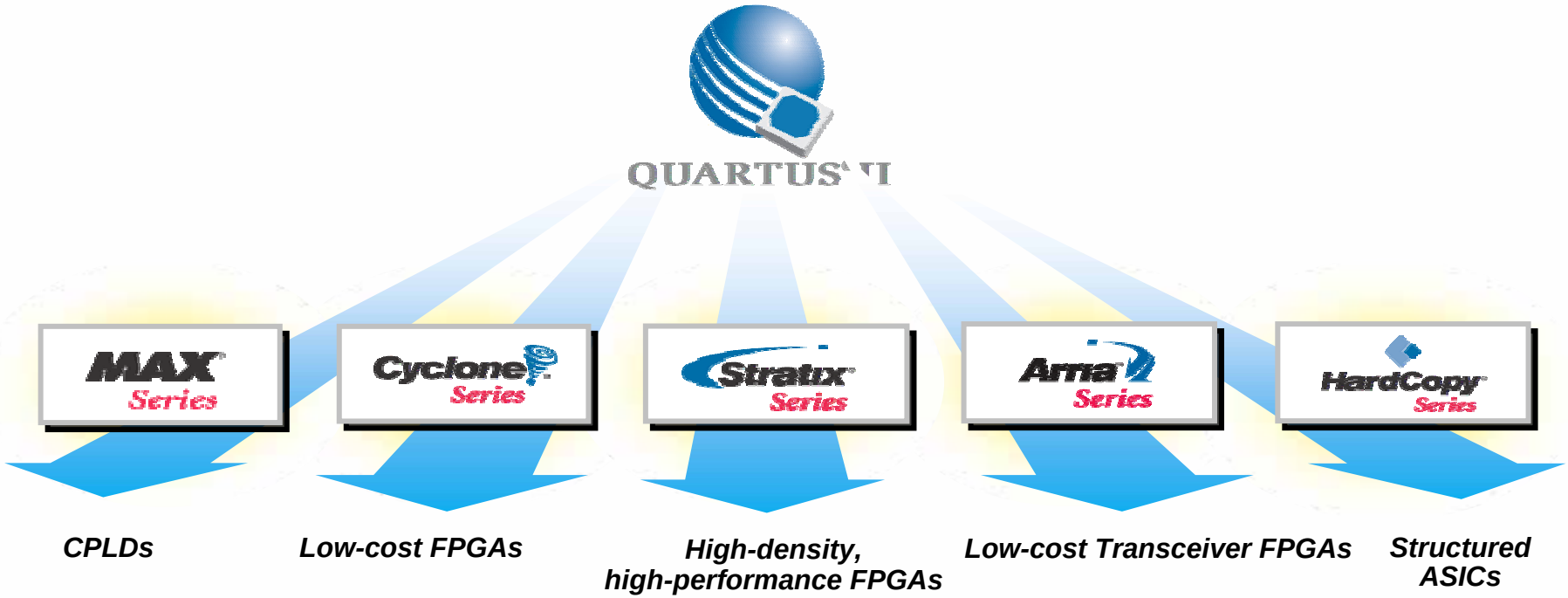
One Tool for All Your Design Needs



Low Development Cost. Improved Productivity

productivity

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MAX II Devices: CPLDs for Simple Applications

- Innovative CPLD architecture delivers the lowest cost
- Cost-saving features
  - 8-Kbit user flash memory
  - Built-In voltage regulator
  - On-chip oscillator
  - Real-time in-system programming
- Non-volatile, instant-on
- 1/10th the power of previous MAX® devices
- Supports 3.3-, 2.5- and 1.8-V supply voltages
- Supported by Quartus II software

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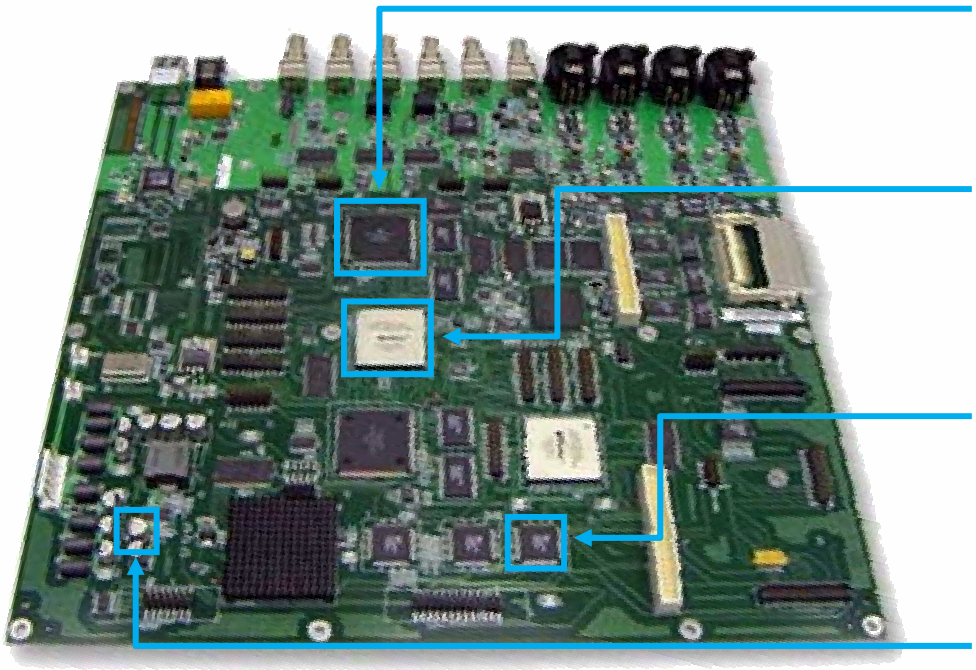
MAX II Target Applications



- Interface bridging
  - Bus protocol translation
  - Serial-to-parallel data conversion
- System configuration
  - ASIC/ASSP/FPGA configuration management
  - Flash controller
- I/O expansion
  - Control signal distribution
  - Address decoding
  - LED activity control
- Power-up sequencing
  - Multi-voltage system power-up management
  - System reset and chip select generation

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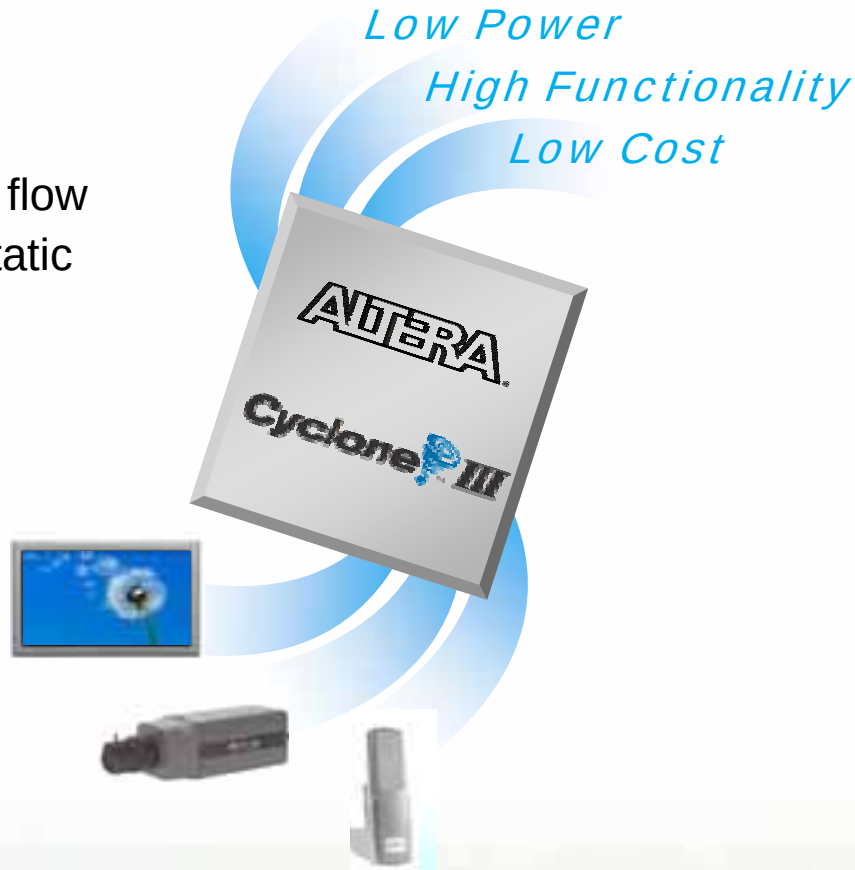
Cyclone III Low-Cost FPGAs for High-Volume Designs

- Low power
  - TSMC 65-nm low-power (LP) process
  - Quartus II software power-aware design flow
  - 120K logic elements (LEs) under ½ W static
- High functionality
  - Densities ranging from 5K to 120K LEs
  - Up to 4 Mbits of embedded memory
  - Up to 288 embedded multipliers for DSP
- Low cost
  - First low-cost 65-nm FPGA
  - Free Quartus II Web Edition software
  - Prices starting as low as $4.00



Turn Your Ideas Into Revenue Faster

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Stratix II GX FPGAs for High-End Transceiver Designs

- Up to 20 transceivers operating between 600 Mbps and 6.375 Gbps
- Lowest-power FPGA with embedded transceivers
- Best-in-class signal integrity solution includes pre-emphasis and equalization
- Complete protocol solution including software support, intellectual property, system models, and reference designs

Transceivers With Optimal Signal Integrity

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Complete Protocol Solutions

- Hard protocol intellectual property (IP), IP functions, reference designs
- Signal integrity modeling
- Protocol-specific development boards
  - PCI Express and SDI
- Evaluation board
- Compliance testing
- System validation reports
- Characterization reports
- Supported by Quartus II software

Dramatically Increase Ease of Design

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Arria GX FPGAs for Low-Cost Transceiver Designs

- Risk-free, low-cost, transceiver-based FPGA family
- Support for mainstream protocols at 1.25 and 2.5 Gbps
  - PCI Express (x1 and x4)
  - Gigabit Ethernet
  - Serial RapidIO® (1x and 4x)
- 5 family members ranging from 21,580 to 90,220 logic elements with up to 4.5 Mbits of memory and 12 transceivers
- 50K LEs for $50 (25Ku)
- Supported by Quartus II software

Device	Transceiver channels	Equivalent logic elements
EP1AGX20	4	21,582
EP1AGX35	4	33,514
	8	
EP1AGX50	4	50,165
	8	
EP1AGX60	4	60,108
	8	
	12	
EP1AGX90	12	90,220

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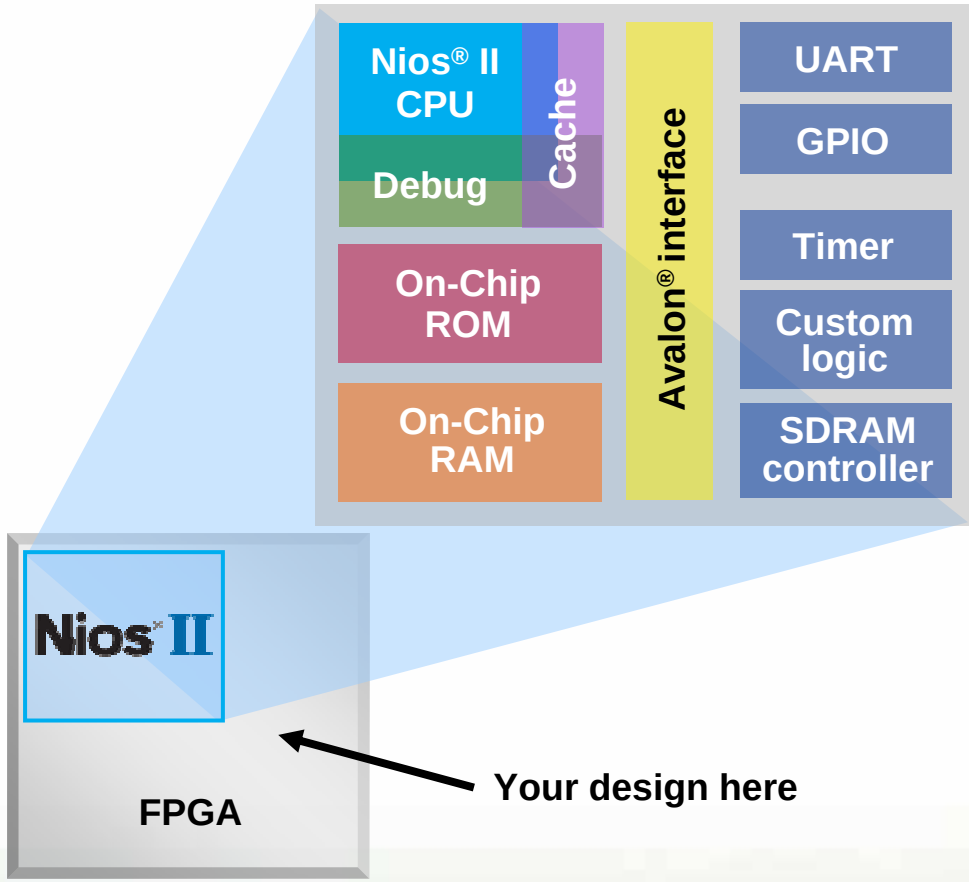
Nios II Processor Overview

- Family of configurable 32-bit RISC processors
- Automated processor configuration and integration of peripherals via SOPC Builder
- Integrate custom logic to add custom features and boost performance
- Performance up to 300 DMIPs (/f, Stratix III FPGA)
- Cost as low as 25¢ of logic (/e, Cyclone III FPGA)



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Why 20K+ Developers Choose Nios II Processors

- Custom fit to users' application
  - Fills gaps inherent in off-the-shelf devices
  - Abundant IP
  - Allows users to use their own innovation
- Works with all Altera FPGA devices
  - Low-cost, high-density, transceivers
  - Structured ASIC (lowest cost)
- Scalable performance
  - Multi-core
  - Custom instructions
  - Hardware accelerators
- Deliver the right product at the right price in the shortest time
  - From concept to system in minutes

Cyclone Series

HardCopy Series

Stratix Series

Arria Series

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Why Altera: End-Market Focus to Align with Customers

Consumer Broadcast Automotive

Entertainment
Broadband
Audio/video
Video display

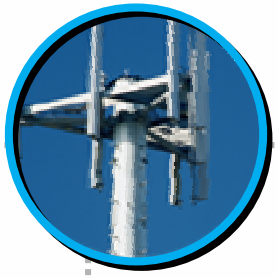
Broadcast
Studio
Satellite
Broadcasting

Automotive
Navigation
Entertainment

Test, Measurement and Medical

Instrumentation
Medical
Test equipment
Manufacturing

Communications



Wireless
Cellular
Basestations
Wireless LAN

Networking
Switches
Routers

Wireline
Optical
Metro
Access

Military and Industrial

Military
Secure comm.
Radar
Guidance and control

Security and Energy Management
Card readers
Control systems
ATM

Computer and Storage

Computers
Servers
Mainframe

Storage
RAID
SAN

Office Automation
Copiers
Printers
MFP

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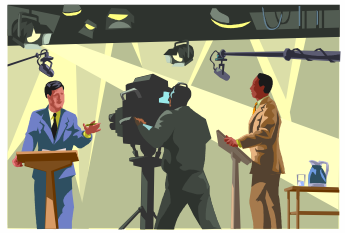
Broadcast Value Proposition

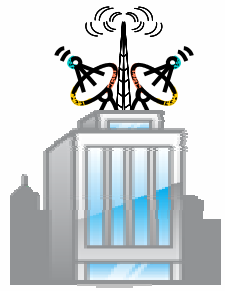
- Quality, affordability, productivity
  - Solutions and kits: defined by customer partners, characterized and proven, facilitates adoption, system integration and studio/head-end interoperability
  - Devices: superior performance, lower power and higher integration ideal for broadcast equipment needs
  - Tools: multimedia framework, open interfaces and Quartus II provides ease of use and higher productivity

Triple-rate SDI *1080p processing* *Audio SRC*

Format Conversion *MPEG-2* *H.264* *Video/IP*



Studios
Contribution



Head-ends
Distribution

Consumers

Today's recognized FPGA vendor of choice for Broadcast

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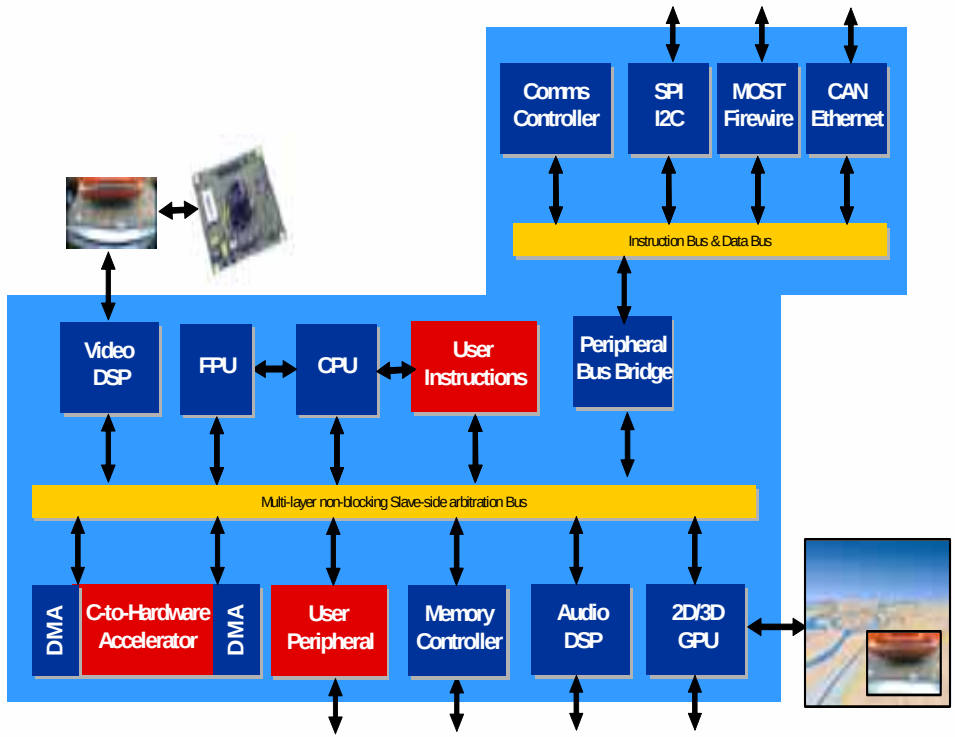
Automotive Value Proposition

- Flexible microcontroller based infotainment system
  - Enables comprehensive design methodology by incorporating hardware, IP, and software onto a single platform
  - Reduces development time at customers
- Fully scalable and cost effective platform
- Seamless ASIC migration
  - HardCopy device with fixed content (equivalent to ASSP)



Target Applications: Next generation car Infotainment and telematics systems

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With Altera You Can..

face your challenges

- Business and technical goals
- Functionality specifications
- Power targets
- Performance targets
- Schedule and budget requirements
- All of your design needs, from high end to low cost

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Altera: The Perfect Partner

- Corporate strategy: *Customer Productivity; Risk Reduction*
- Comprehensive product portfolio
  - CPLDs, FPGAs, and structured ASICs
  - Extensive IP portfolio, including Nios II processor
  - One design tool for all your design needs
- History of operational excellence
  - 13-year sole partnership with TSMC, world's #1 foundry
  - First time right silicon; risk reduction for our customers
- Worldwide support
  - Online support at www.altera.com
  - 24-hour customer service and support
  - Service centers in China, Japan, Europe, USA
- Ecosystem
  - Partnership with best-in-class EDA, IP, and supply chain vendors

high productivity: low risk

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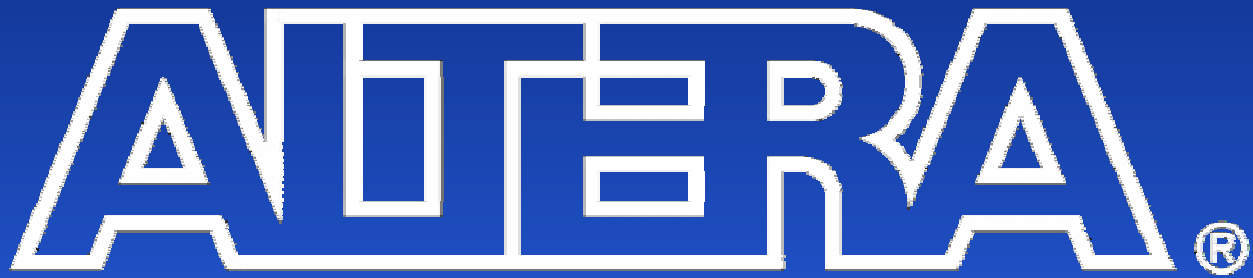
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