Enabling New Low-Cost Embedded System Using Cyclone® III FPGAs

Unprecedented combination of low power, high functionality, and low cost to enable your new designs

Agenda

- Historical perceptions of FPGAs and current FPGA value proposition
- Hardware and software basis for making low-cost embedded system
- Embedded system design flow using FPGA
- Implementation examples and resources available
- Conclusion

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Historical Perceptions of FPGAs

- In the past FPGAs have...
  - ...been too expensive
  - ...not offered enough performance
  - ...only been offered in low densities
  - ...consumed too much power
  - ...been challenging for which to design

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FPGA Value Proposition

Value	Example end markets	Reason
Performance-to-price ratio	Video and medical imaging	■ Parallel processing
Low cost and power per channel	Video surveillance, wireline, wireless	■ Parallel processing
Flexibility	Consumer, video and imaging, wireline, wireless	■ Changing standards ■ Feature differentiation ■ Competitive response
Obsolescence-proof	Medical imaging, military, wireline, wireless	■ Longevity vs. ASSPs

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Hardware and Software Basis for Making Low-Cost Embedded System

A Complete Solution

Nios® II

Embedded soft-core processors

Intellectual property (IP)

QUARTUS® II

Design software

Orderable Now - Only $199!

Development kits

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Unprecedented Combination

- Low power
  - TSMC 65-nm low-power (LP) process
  - Quartus® II software power-aware design flow
  - 120K logic elements (LEs) under ½ W static
- High functionality
  - Densities ranging from 5K to 120K LEs
  - Up to 4 Mbits of embedded memory
  - Up to 288 embedded multipliers for digital signal processing (DSP)
- Low cost
  - First low-cost 65-nm FPGA
  - Free Quartus II Web Edition software
  - Prices starting as low as $4.00

Turn Your Ideas Into Revenue Faster

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Meeting the Needs of Emerging High-Volume Applications

- *2 – 20K logic elements (LEs)*
- *295-Kbits embedded RAM*
- *DDR support*
- *Nios® embedded processor*

2002

- *5 – 70K LEs*
- *1.1-Mbits embedded RAM*
- *150 18 x 18 multipliers for DSP*
- *DDR2 support*
- *Nios II embedded processor*

2004

- *50% lower power vs. Cyclone® II FPGAs*
- *5 – 120K LEs*
- *4-Mbits embedded RAM*
- *288 18 x 18 multipliers for DSP*
- *Higher performance DDR2 support*
- *Nios II embedded processor*

2007

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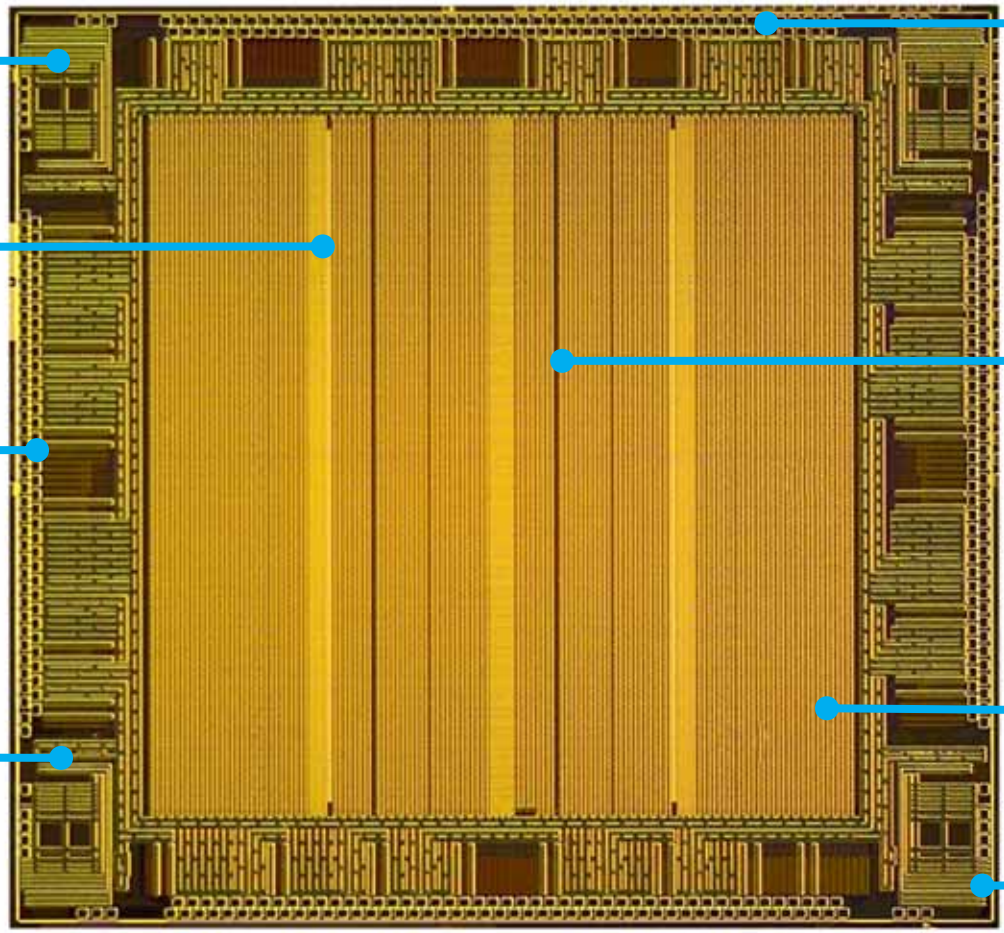
Cyclone III Key Architectural Features



65-nm low-power process

Up to 4-Mbit embedded memory

Up to 535 flexible user I/O pins

Parallel and serial configuration with new remote update feature

400-Mbps external memory interfaces

Up to 288 embedded multipliers for high-throughput DSP

5 – 120K LEs

Dynamically configurable phase-locked loops (PLLs)

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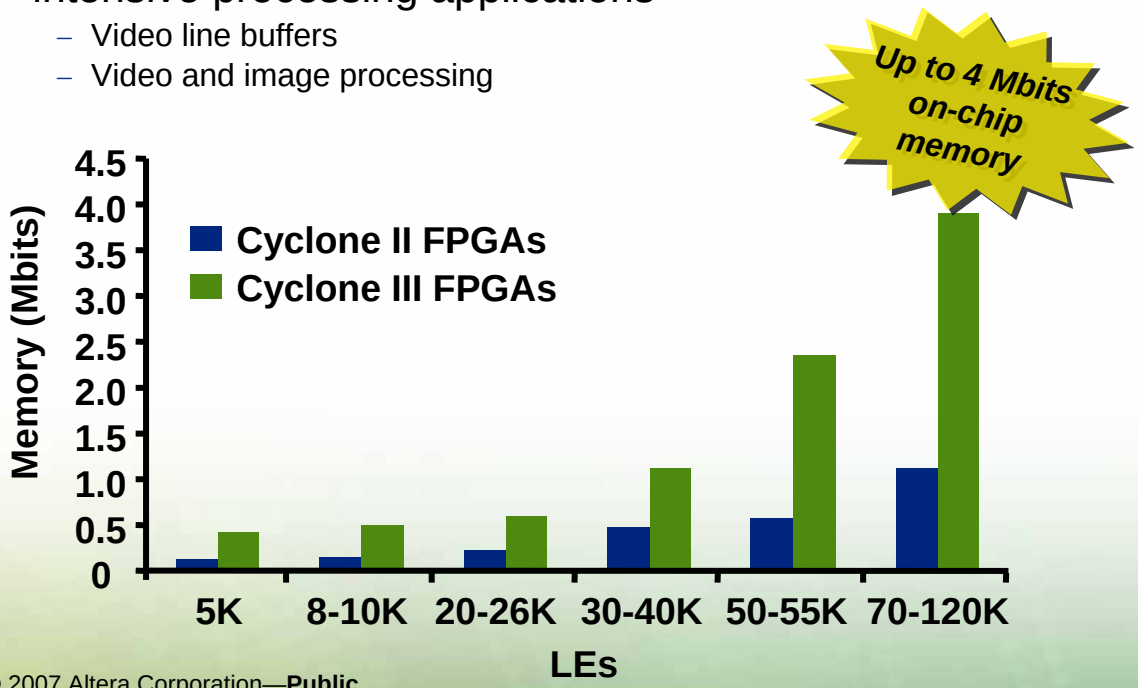
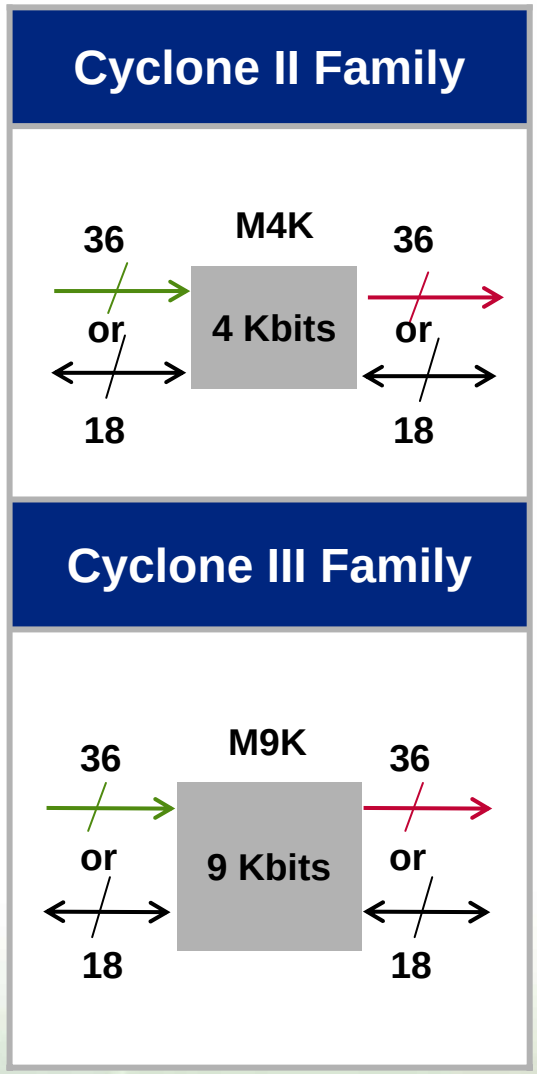
Memory Optimizations

- Increased memory block size
  - Allows for increased memory capacity
- Higher memory-to-logic ratio
  - Implement packet buffers
  - Integrate larger data and instruction caches for embedded processors
  - Integrate larger FIFO buffers
- Optimized memory-to-multiplier ratio for intensive processing applications
  - Video line buffers
  - Video and image processing





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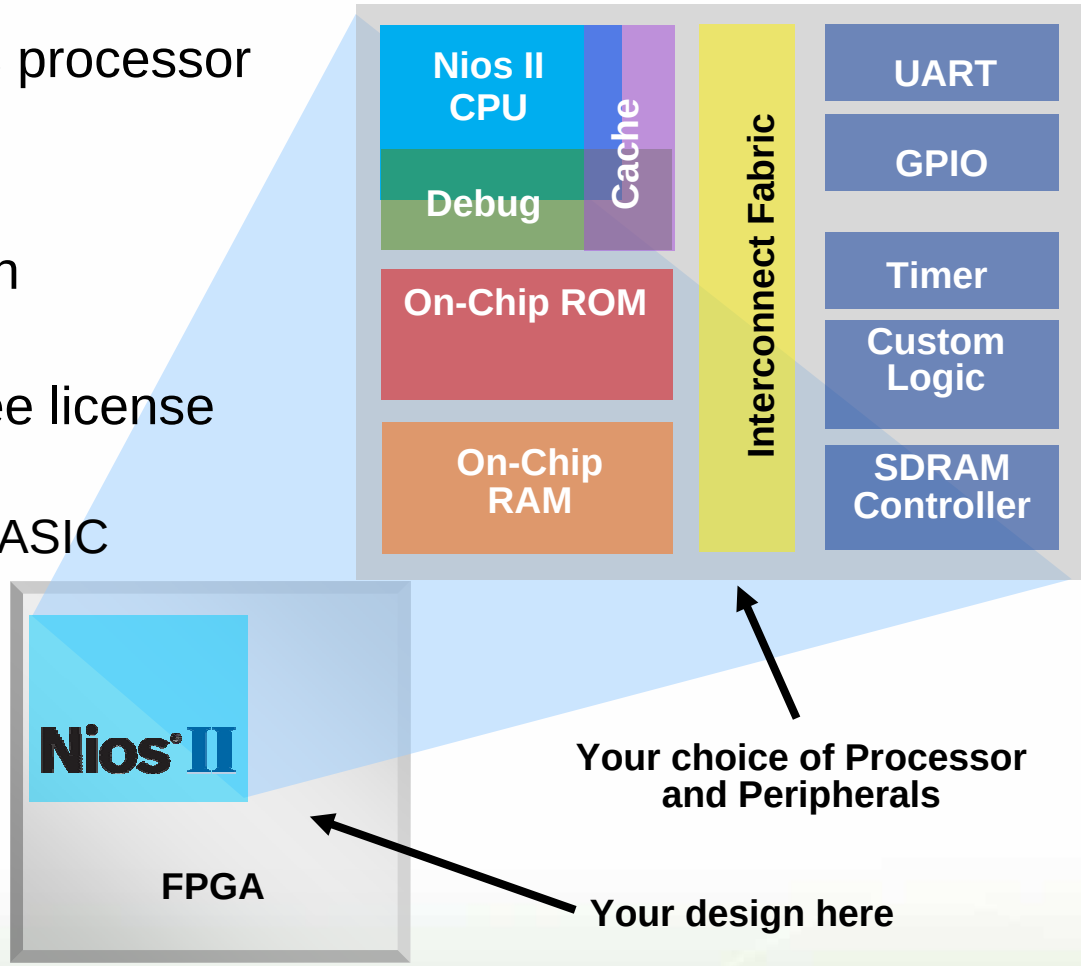
Nios II Embedded Processor

- Configurable 32-bit RISC processor
- 3 members – choose for performance or size
- Library of peripherals with software support
- Perpetual use, royalty-free license
  - Altera® FPGA
  - HardCopy® structured ASIC



Implement a Processor in $0.25 of Logic

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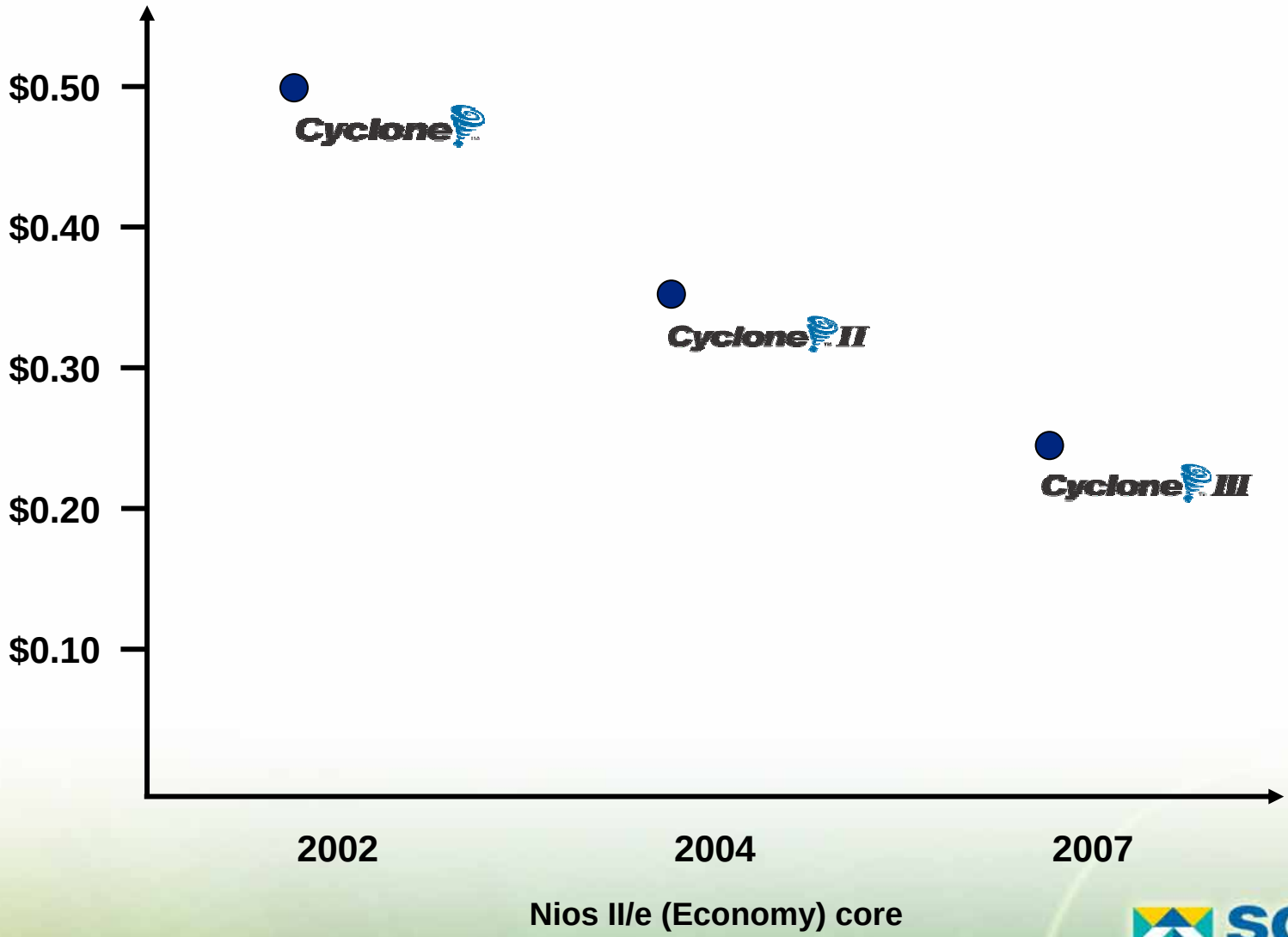
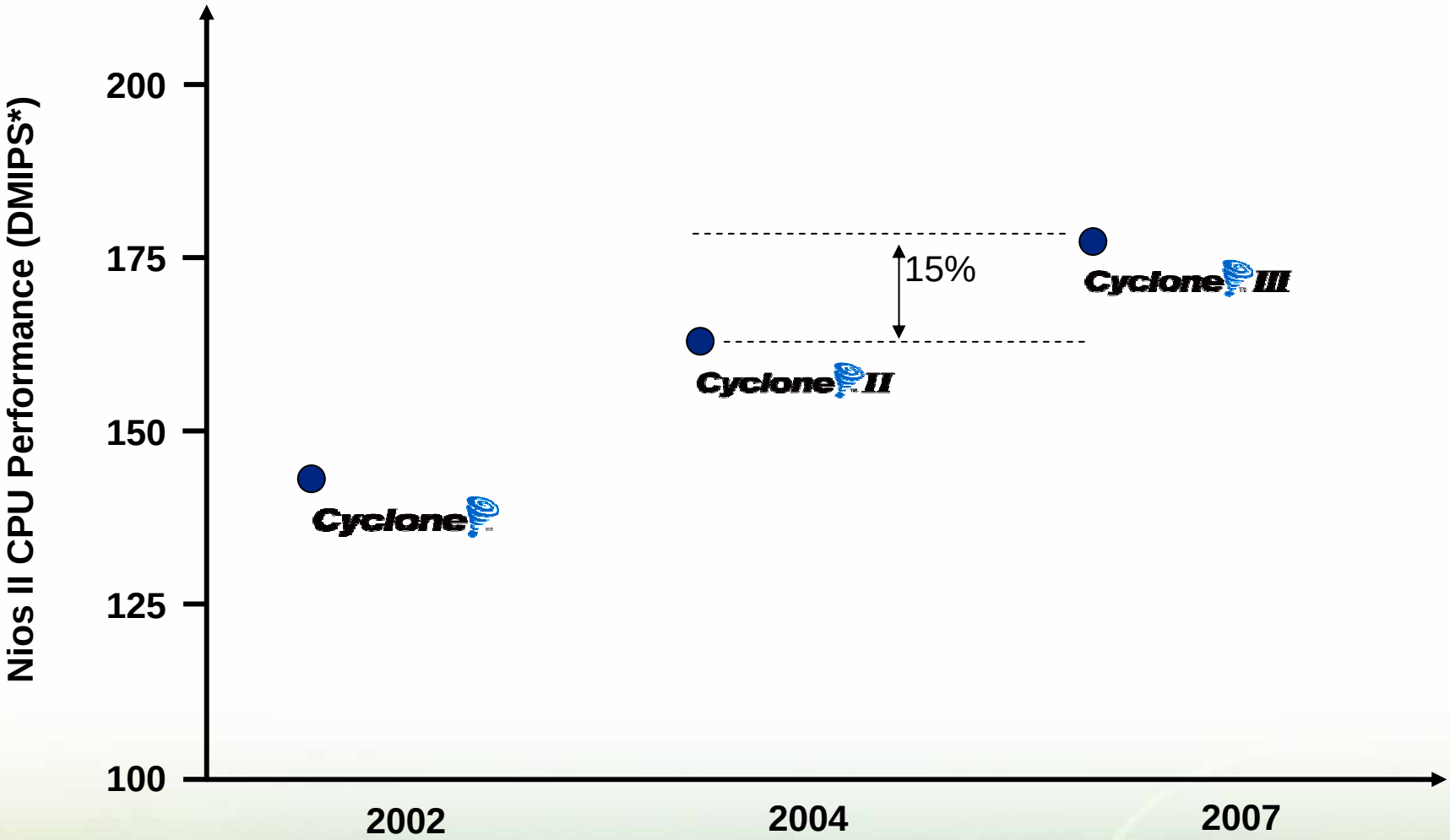
Processor Cost Reduction in Cyclone III FPGAs



Processor Performance Boost in 65-nm Devices



*** Dhrystone 2.1 benchmark**

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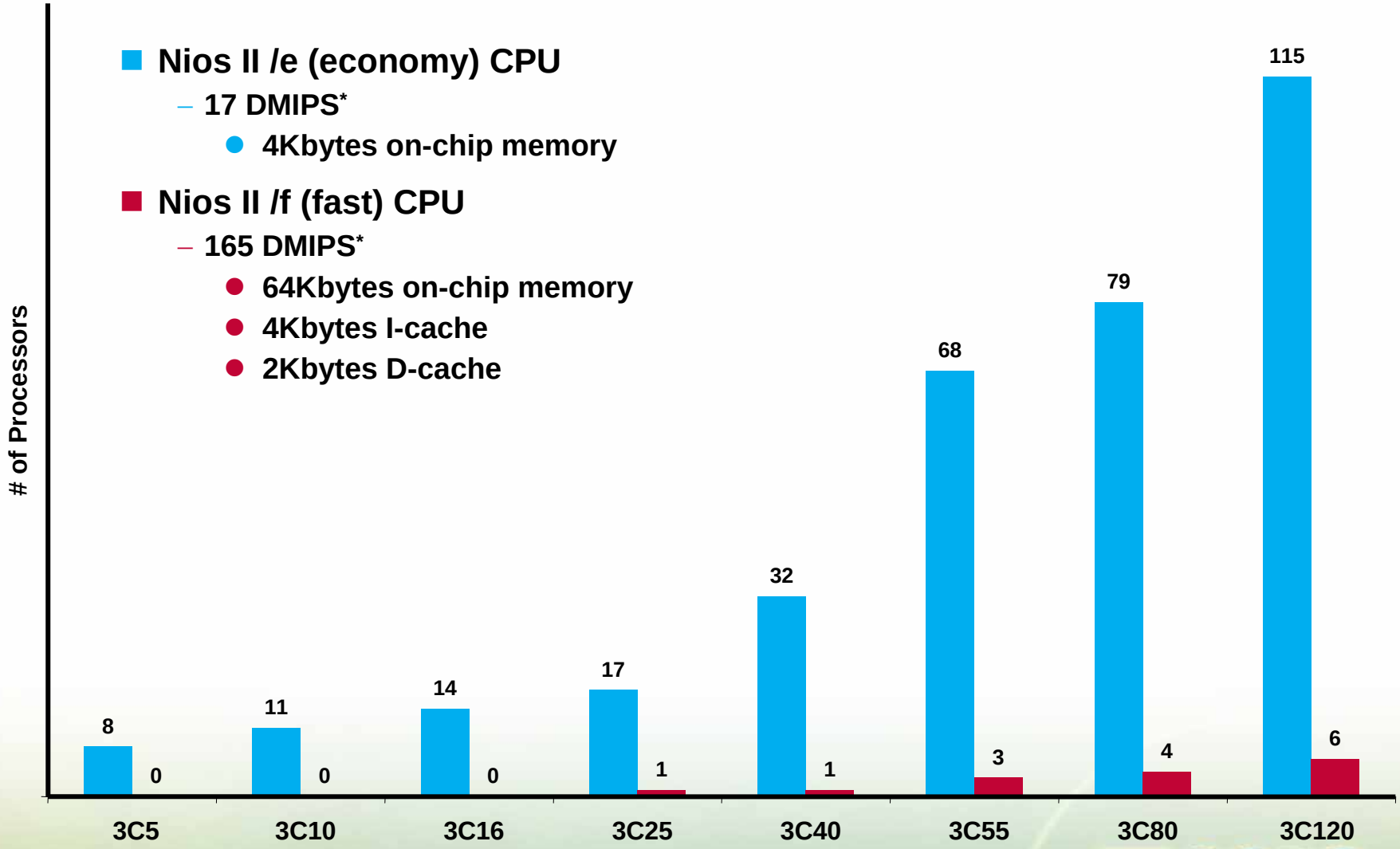
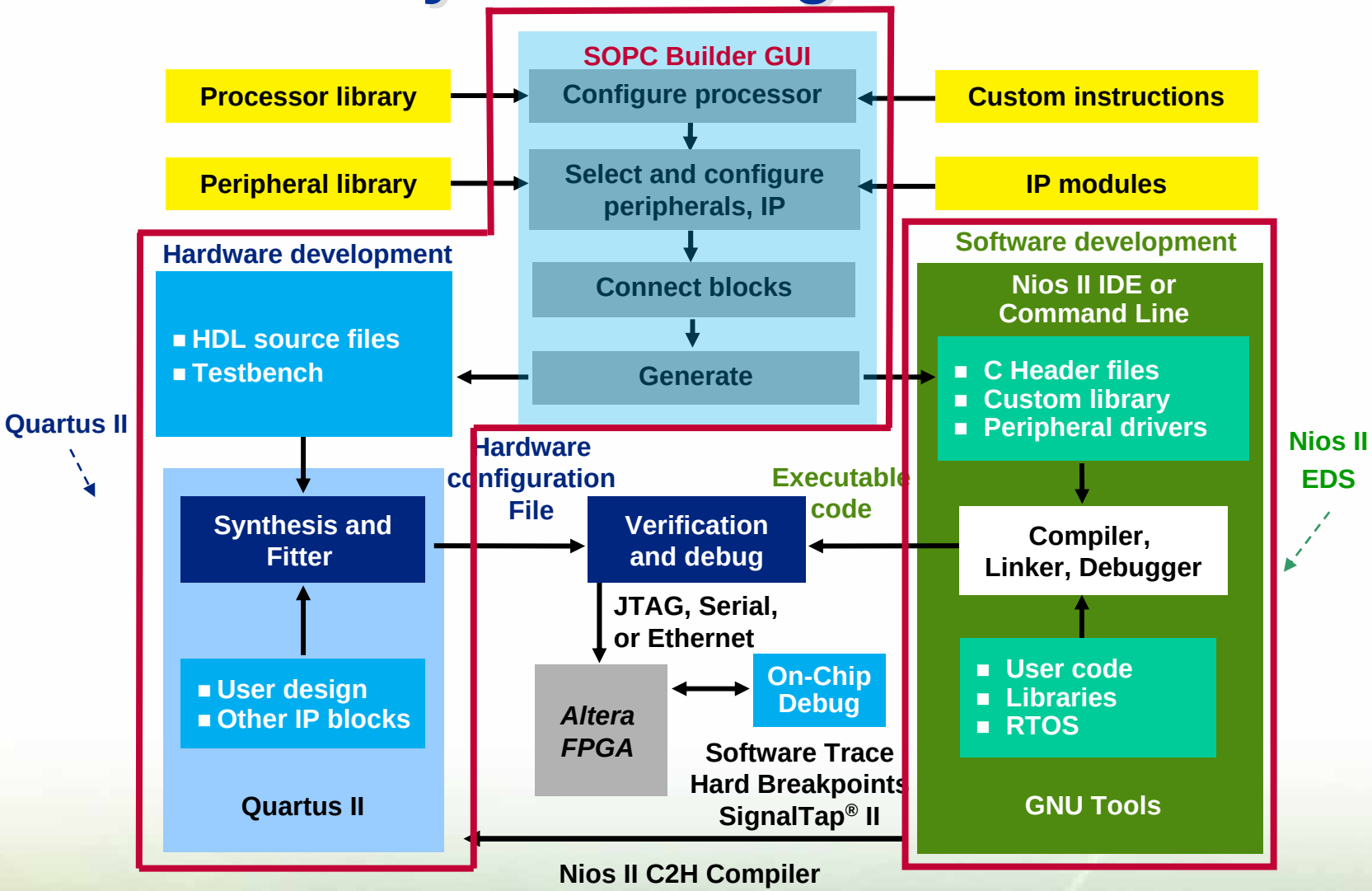
Multi-Core Designs in Cyclone III FPGAs



* Dhrystone 2.1 benchmark

Embedded System Design Flow Using FPGAs

Embedded System Design Flow



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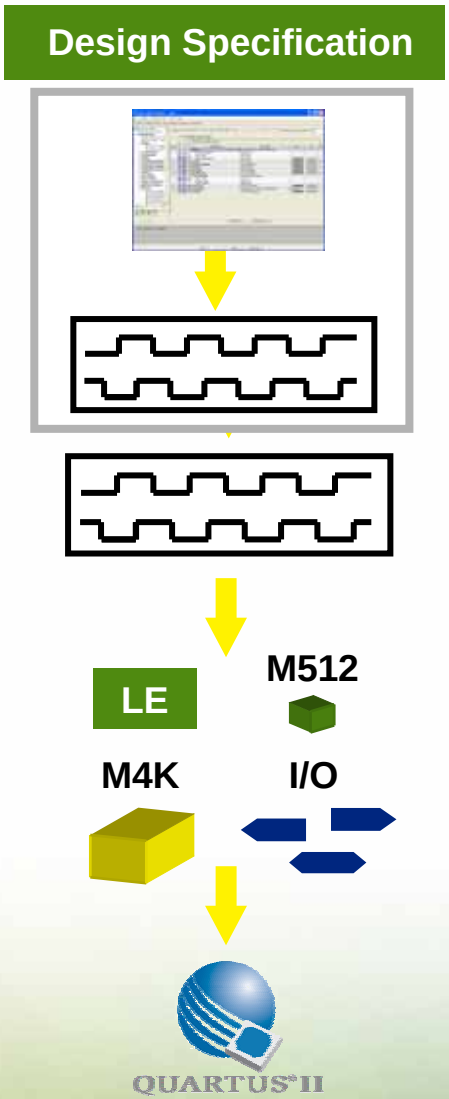
FPGA Hardware Development Design Flow



- **SOPC Builder**
  - Functional simulation (ModelSim®, Quartus II tools)
  - Verify logic model and data flow (no timing delays)
- **Design entry/register transfer level (RTL) coding**
  - Behavioral or structural description of design
- **RTL simulation**
  - Functional simulation (ModelSim, Quartus II tools)
  - Verify logic model and data flow (no timing delays)
- **Synthesis**
  - Translate design into device-specific primitives
  - Optimization to meet required area and performance constraints
  - Spectrum, Synplify, Quartus II software
- **Placement and routing**
  - Map primitives to specific locations inside target technology with reference to area performance constraints
  - Specify routing resources to be used

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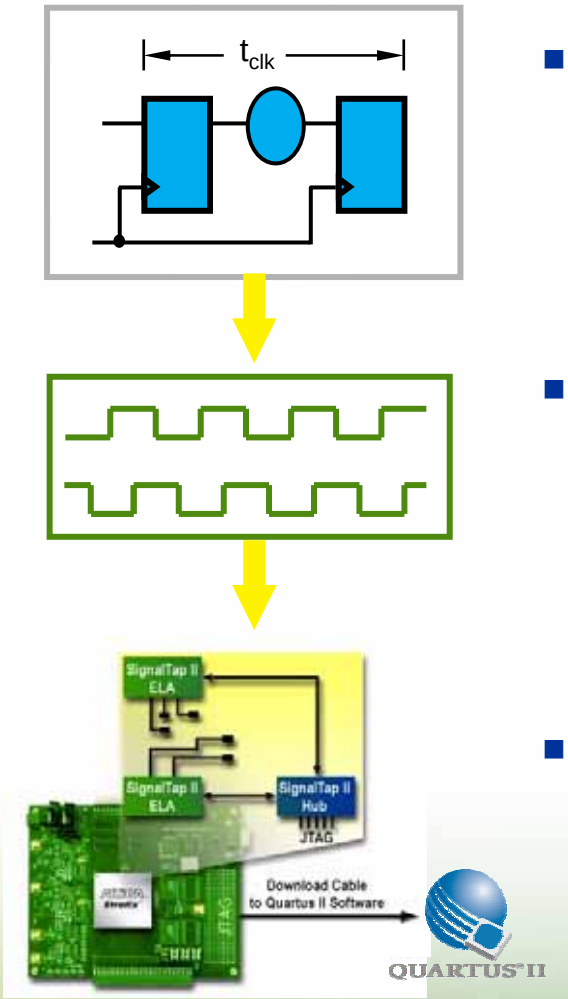
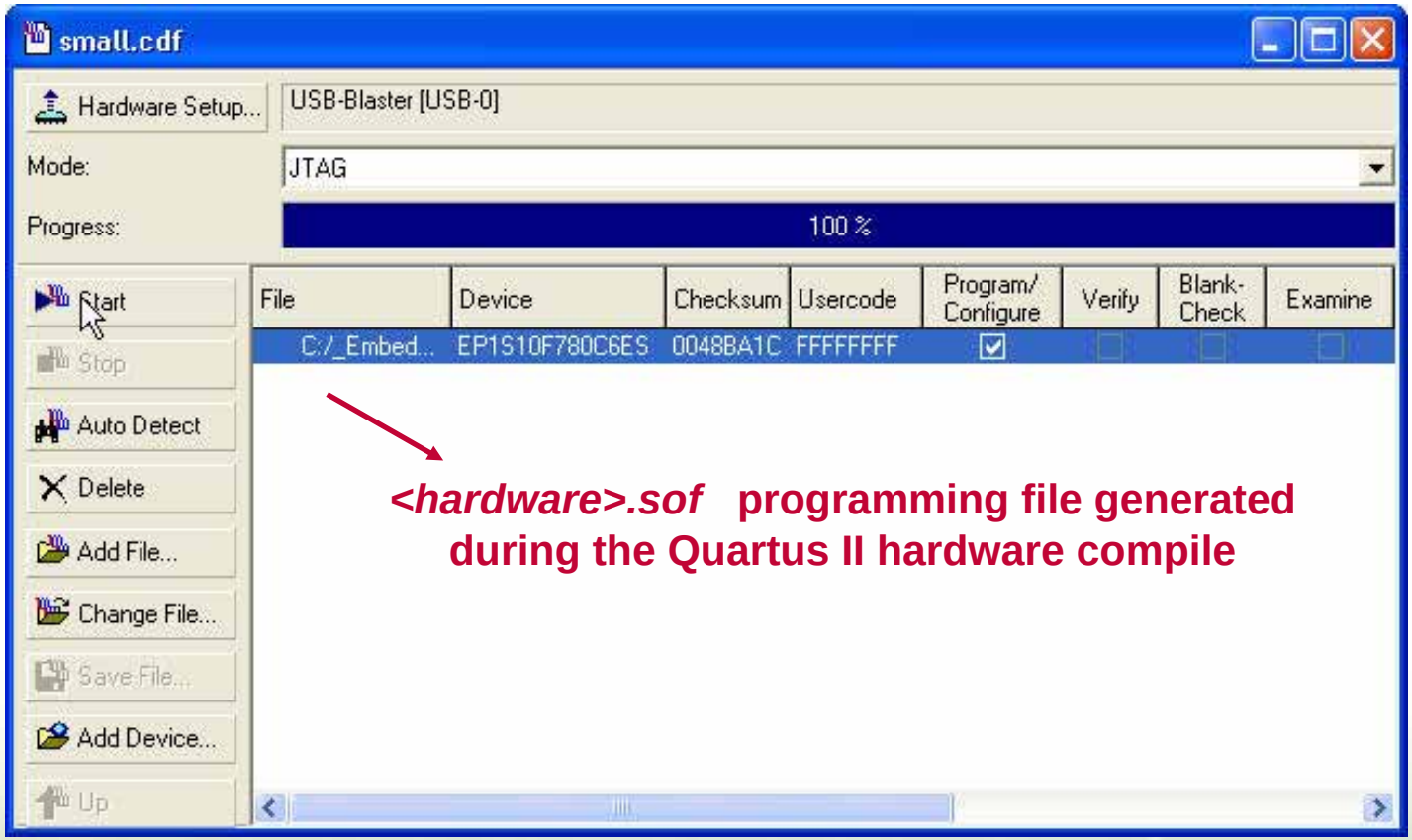
FPGA Hardware Development Hardware Design Flow



- **Timing analysis**
  - Verify performance specifications were met
  - Static timing analysis
- **Gate-level simulation**
  - Timing simulation
  - Verify design will work in target technology
- **Test FPGA on PC board**
  - Program and test device on board
  - Use SignalTap II logic analyzer and SignalProbe for debugging
    - Discussed in depth in advanced Quartus II software class

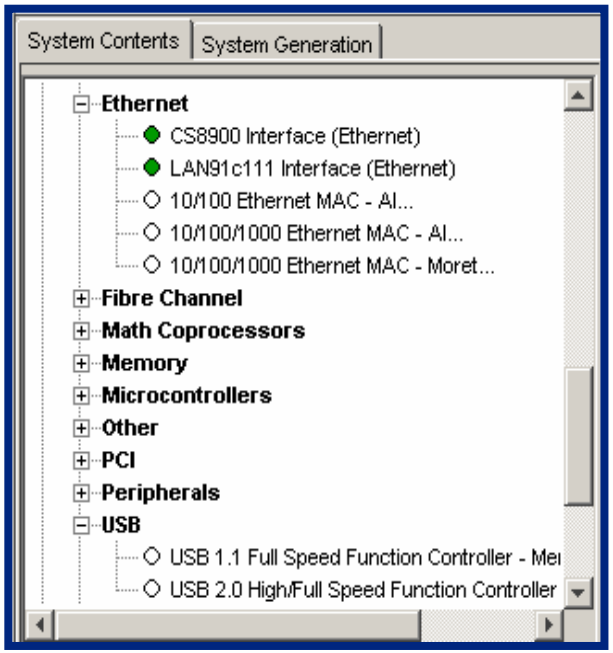
Using Quartus II Programmer

- Launch from Quartus II design software after compiling to program FPGA

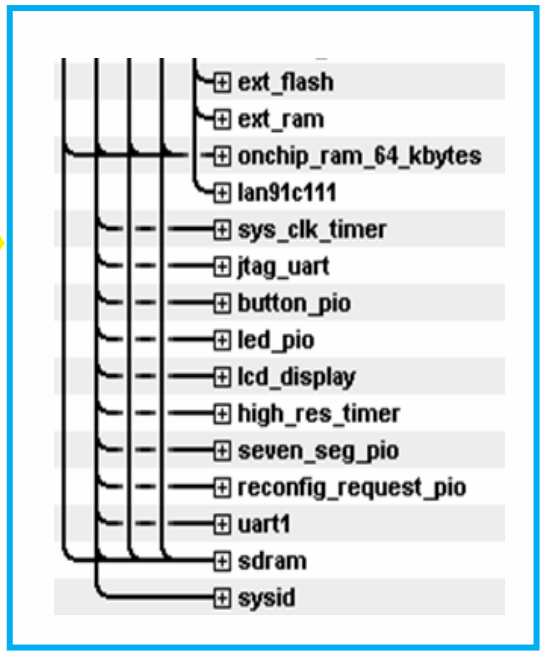


SOPC Builder System Design Software

1. Select and configure IP



2. Select connections



3. Generate system

QUARTUS® II

HDL Simulator

ALTERA Cyclone III

Easy, Flexible, Fast

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Nios II IDE (Integrated Development Environment)*

- Leading-edge software development tool in the Nios II Embedded Design Suite
- Target connections
  - Hardware (JTAG)
  - Instruction set simulator
  - ModelSim-Altera software
- Advanced hardware debug features
  - Software and hardware breakpoints, data triggers, trace
- Flash memory and Quartus II programming support

*** Based on Eclipse 3.2/CDT 3.1**

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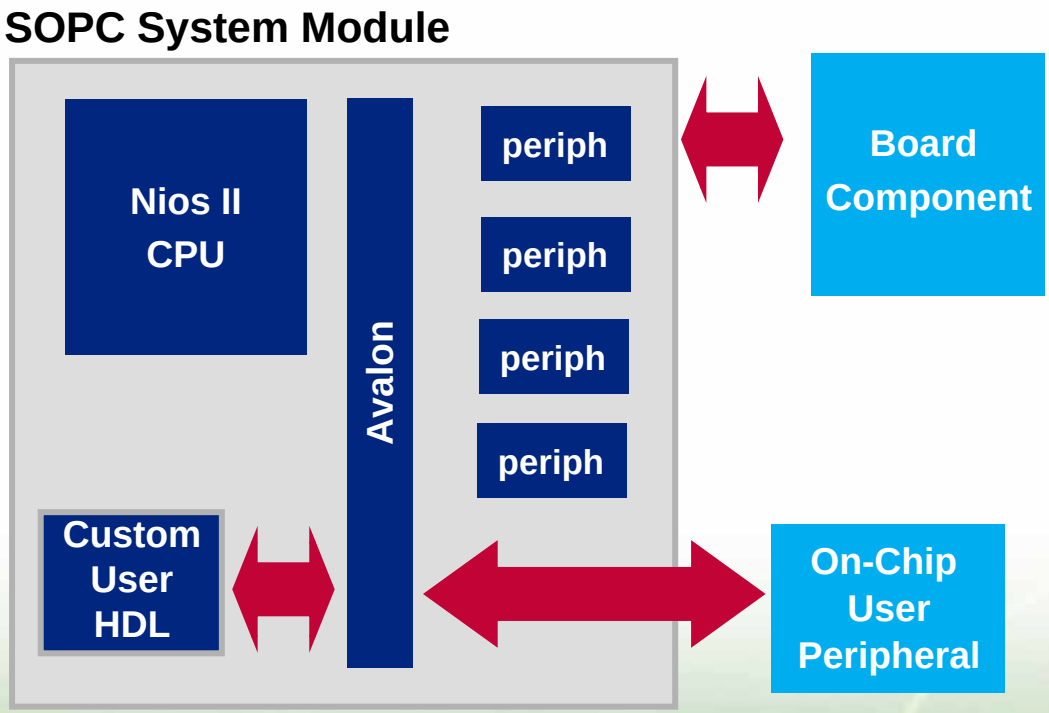
User-Defined Custom Peripherals

- Add a peripheral not included with the Nios II system
  - To perform some kind of proprietary function or perhaps a standard function that is not yet included as part of the Nios II kit
  - To expand or accelerate system capabilities
- You are now going to learn how to connect your own design directly to the Nios II system via the Avalon™-Memory Mapped interconnect
  - *Note:* As many peripherals contain registers, you could *also* have chosen to use a programmed input/output (PIO) rather than connect directly to the bus

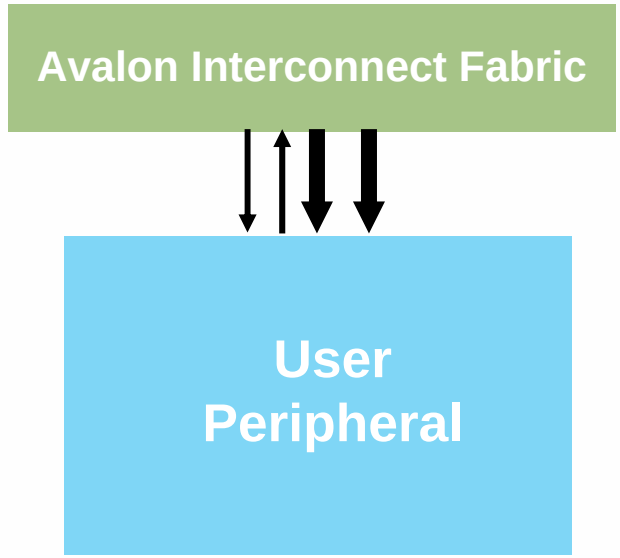
Custom Peripherals

- Map into Nios II memory space
- Can be on-chip or off-chip
  - HDL code or an external component on your board
    - HDL code can map inside SOPC Builder system or out



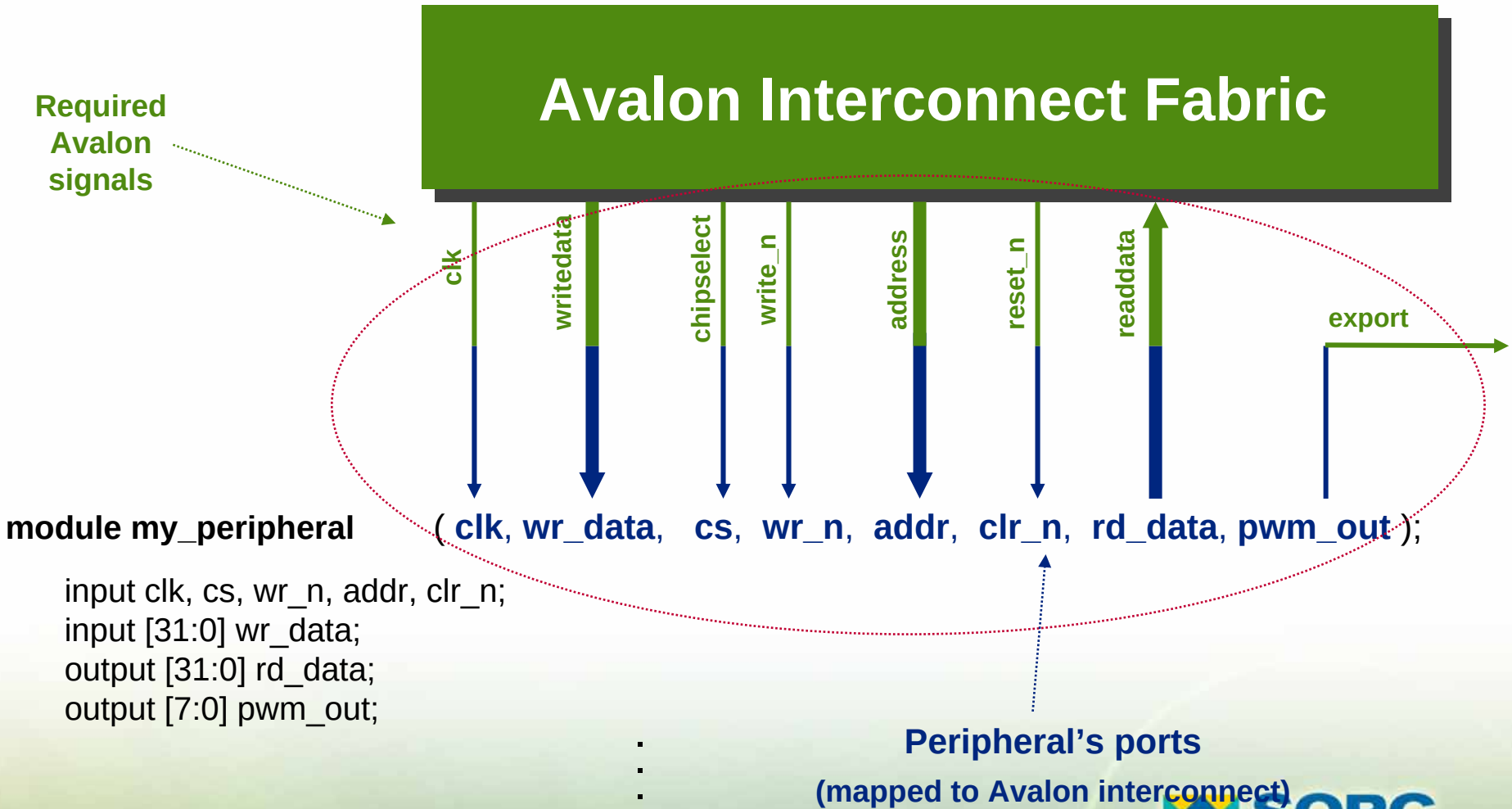
Creating Avalon Peripherals

- No need to worry about creating the bus interface to Avalon Interconnect inside your peripheral
  - Implement only the signals you need
  - Avalon Memory Mapped Interconnect will adapt to connect to the peripheral's ports
  - Timing handled automatically
  - Fabric created for you
  - Arbiters generated as needed

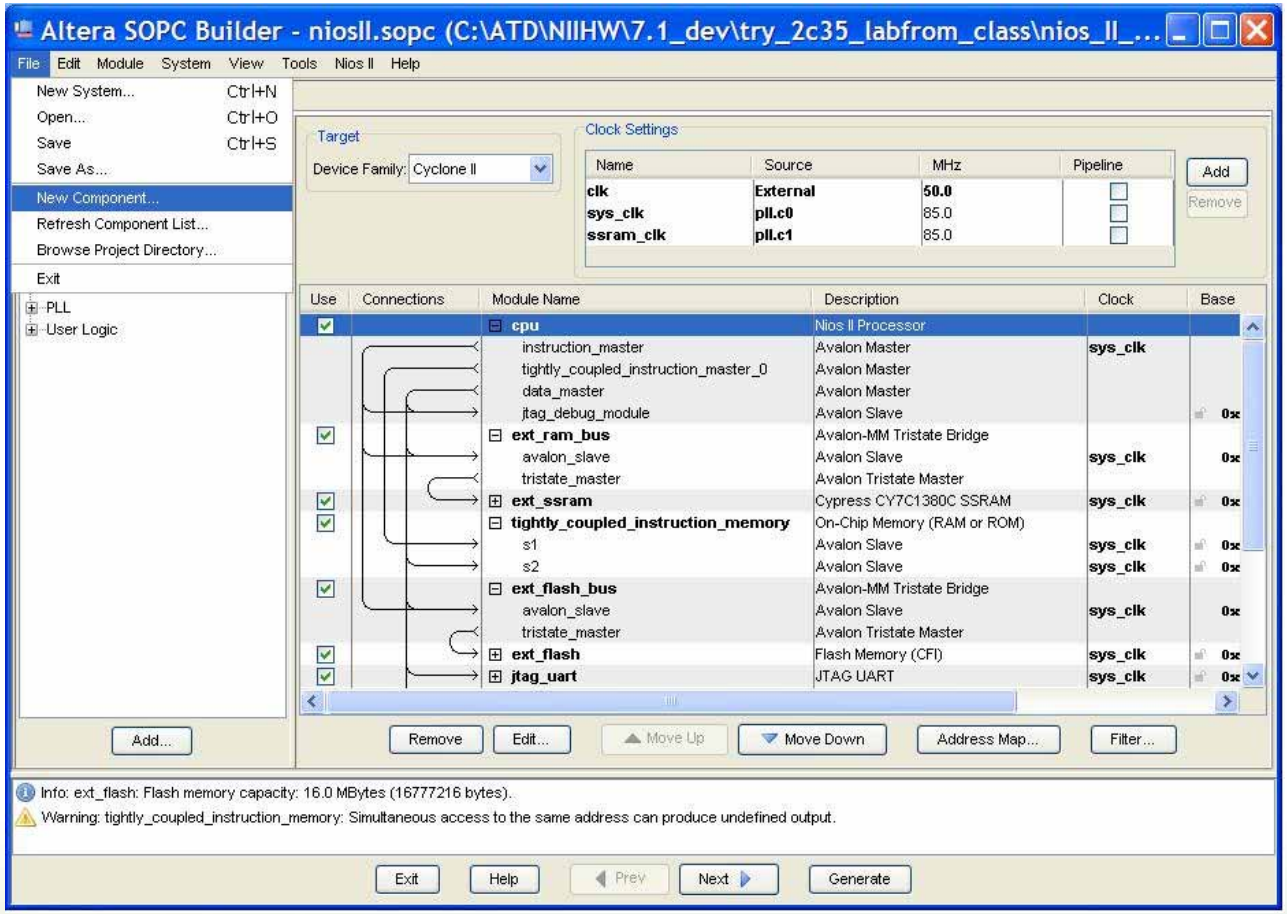


Concentrate Effort on Peripheral Functionality!

Map Ports to Avalon Signal Types



Component Editor

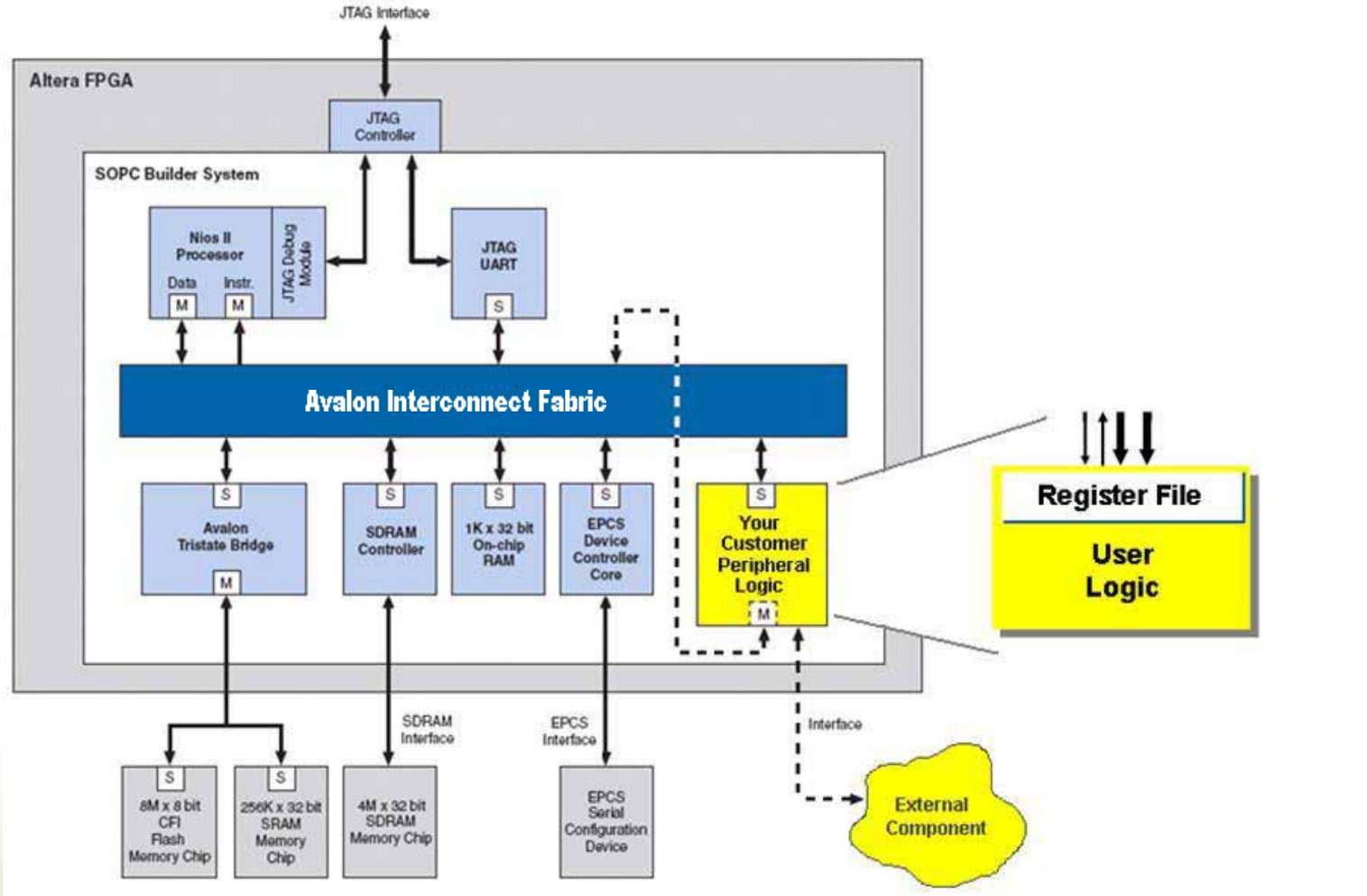


Two Uses:

1. Create a wrapper file that connects Avalon bus to peripheral living outside SOPC system *(on- or off-chip)*

2. Create direct *on-chip* connection between Avalon bus and user HDL code

Custom Peripheral Integration Into Avalon



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SOPC Builder - Component Scripting

- Component Editor
  - Writes a TCL script file instead of proprietary class.ptf file

```
# TCL File Generated by Component Editor on:
# Wed Jan 17 10:18:07 PST 2007
# DO NOT MODIFY

set_source_file "/data/korthner/SPR/230791/tb_sopc/my_onchip_mem.vhd"
set_module "my_onchip_mem"
set_module_description ""
set_module_property instantiateInSystemModule true
set_module_property version 1.0
set_module_property group ""
set_module_property editable true
set_module_property libraries "altera.altera_europa_support_lib.all,a

# Module parameters

# Interface avalon_slave_0
add_interface "avalon_slave_0" "avalon" "slave" "asynchronous"
set_interface_property "avalon_slave_0" "interleaveBursts" "false"
set_interface_property "avalon_slave_0" "addressAlignment" "DYNAMIC"
set_interface_property "avalon_slave_0" "isNonVolatileStorage" "false
```

- Scripting interface
  - Well-defined TCL API to describe components and their interfaces
  - Build your own TCL-defined components
    - Automatically found by SOPC Builder

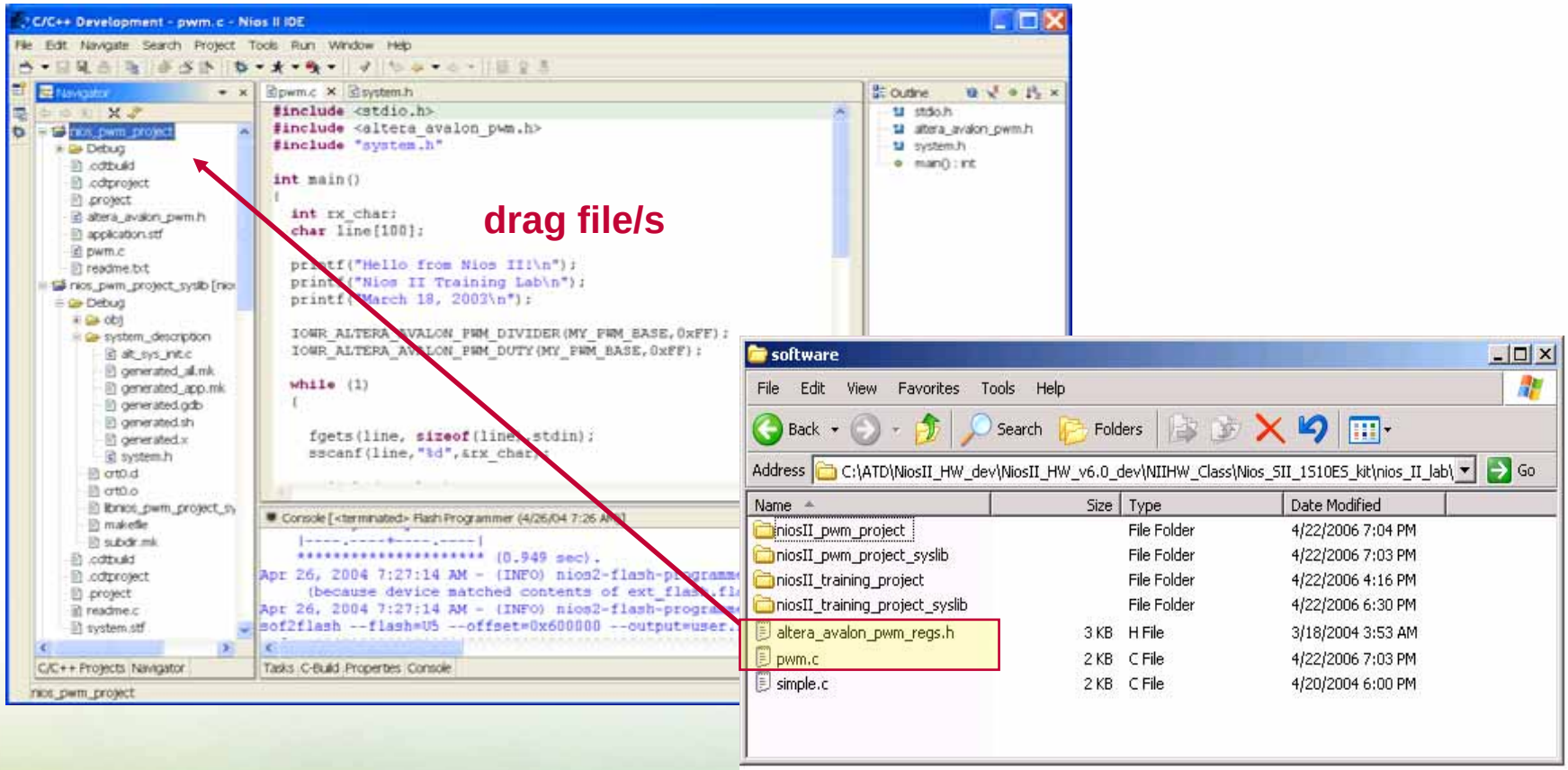
Device Driver for PWM Peripheral

- "avalon_pwm_regs.h"
  - Manually add to software project
  - Loads peripheral registers to run **pwm**

```
#ifndef __ALTERA_AVALON_PWM_REGS_H__
#define __ALTERA_AVALON_PWM_REGS_H__

#include <io.h>

#define IORD_ALTERA_AVALON_PWM_DIVIDER(base)           IORD(base, 0)
#define IOWR_ALTERA_AVALON_PWM_DIVIDER(base, data)     IOWR(base, 0, data)

#define IORD_ALTERA_AVALON_PWM_DUTY(base)           IORD(base, 1)
#define IOWR_ALTERA_AVALON_PWM_DUTY(base, data)     IOWR(base, 1, data)

#endif /* __ALTERA_AVALON_PWM_REGS_H__ */
```

Manually Add Driver Code to Project

- Using same method as adding application code



Custom Instructions

- Add custom functionality to the Nios II design
  - To take full advantage of the flexibility of FPGA
- Dramatically boost processing performance
  - With no increase in f_{MAX} required
- Application examples
  - Data stream processing (e.g. network applications)
  - Application-specific processing (e.g. MP3 audio decode)
  - Software inner loop optimization

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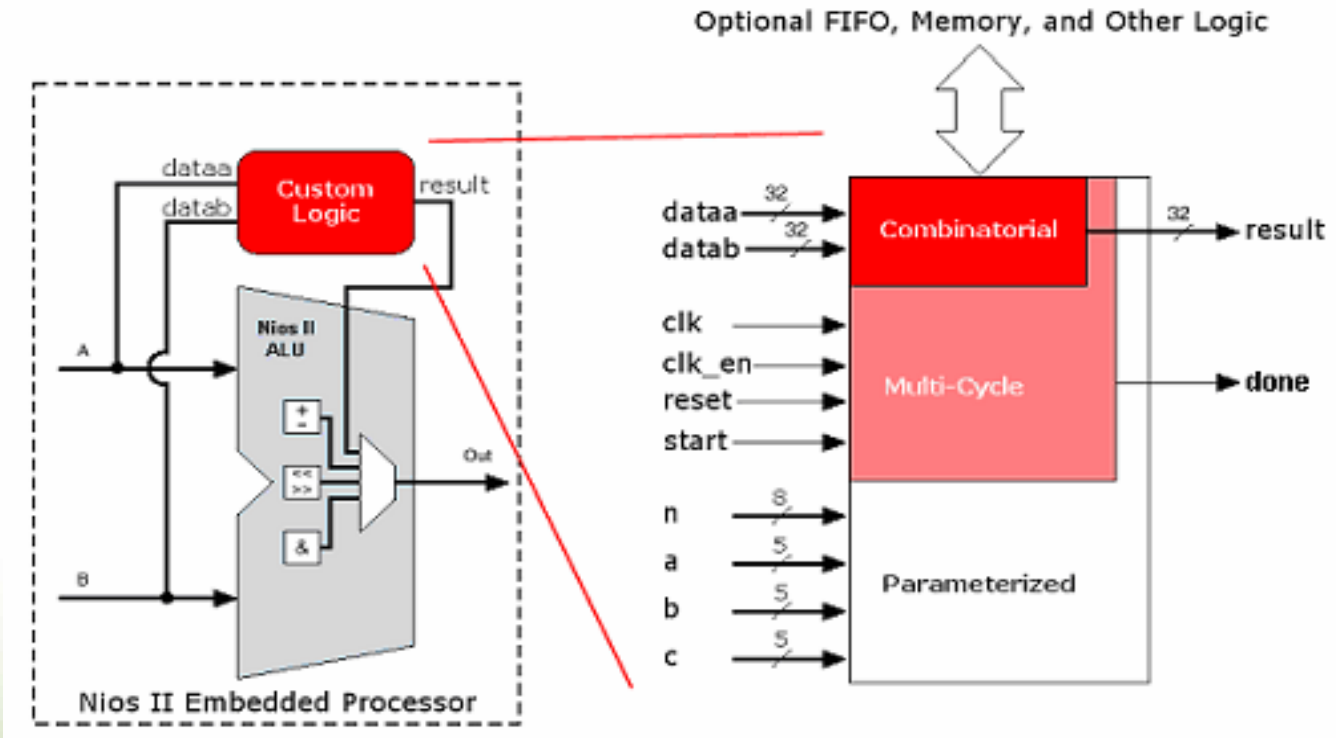
Custom Instructions

- Augment Nios II instruction set
  - Multiplexing user logic into arithmetic logic unit (ALU) path of processor pipeline

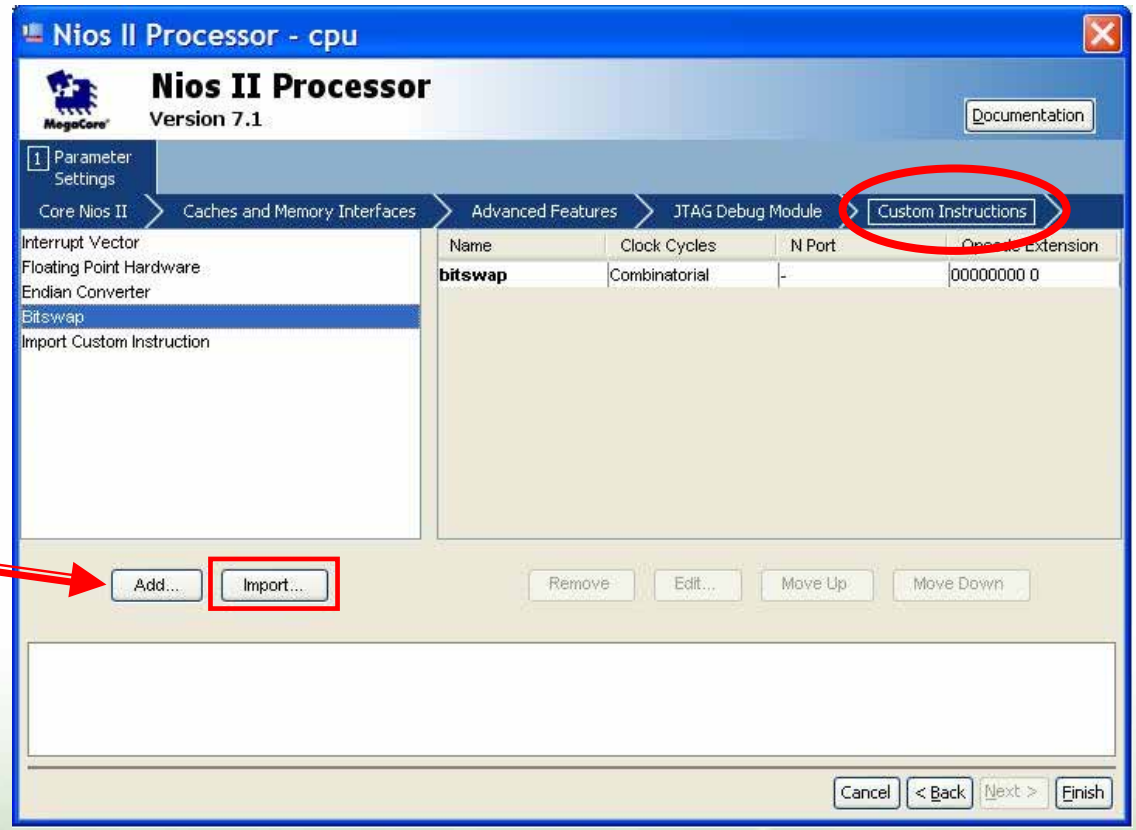


Custom Instructions Tab

- Enabled from the **Custom Instructions** tab in the Nios II CPU Wizard in SOPC Builder

Add a custom instruction from built-in library

Or import your own user logic



C Language Software Interface

- Nios II IDE generates macros automatically during build process
- Macros defined in **system.h** file

  #define ALT_CI_<your instruction_name>(instruction arguments)

- Example of user C-code that references Bitswap custom instruction:

```
#include "system.h"
int main (void)
{
    int a = 0x12345678;
    int a_swap = 0;

    a_swap = ALT_CI_BSWAP(a);
    return 0;
}
```

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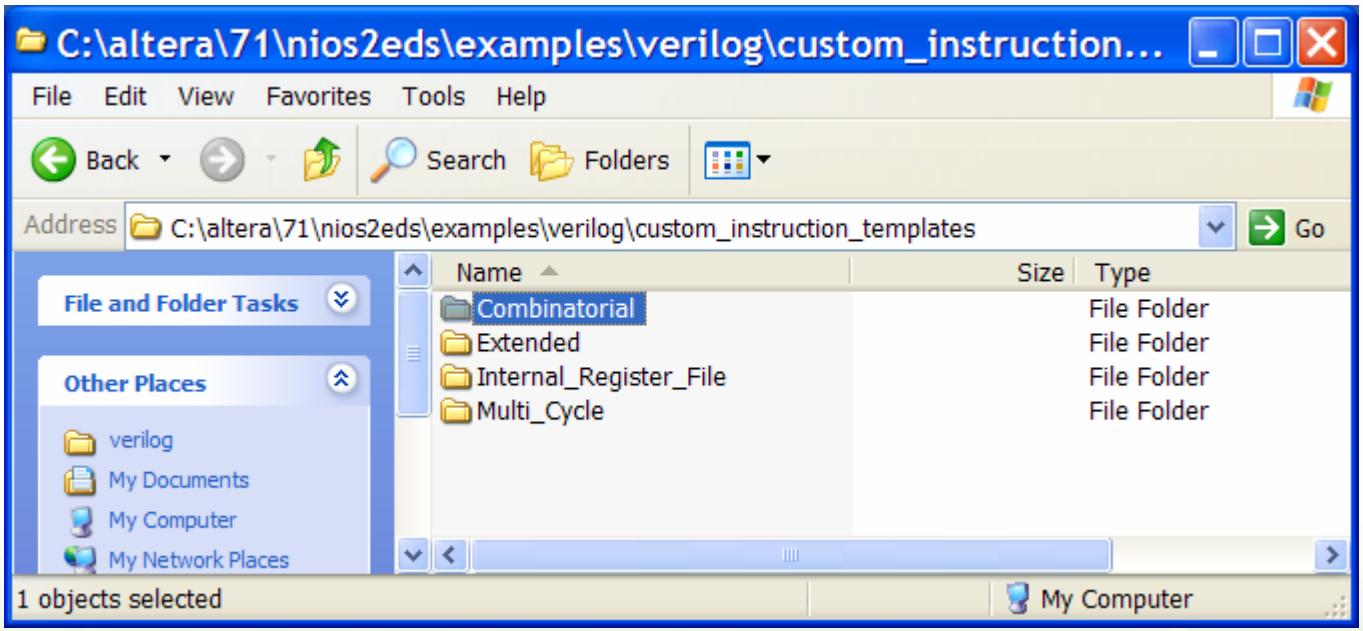
Verilog and VHDL Templates Available

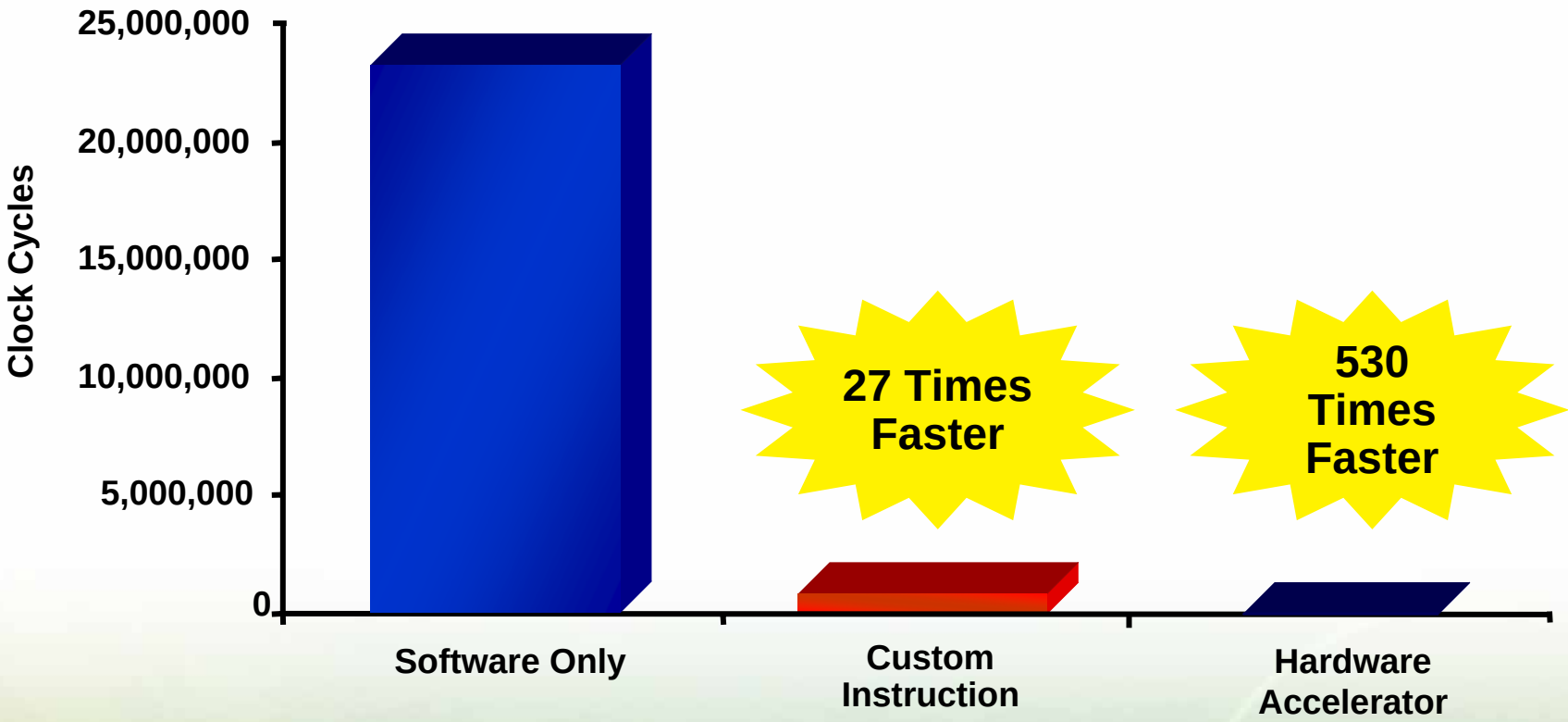
C:\altera*<ver#>*\nios2eds\examples\verilog\custom_instruction_template

C:\altera*<ver#>*\nios2eds\examples\VHDL\custom_instruction_template



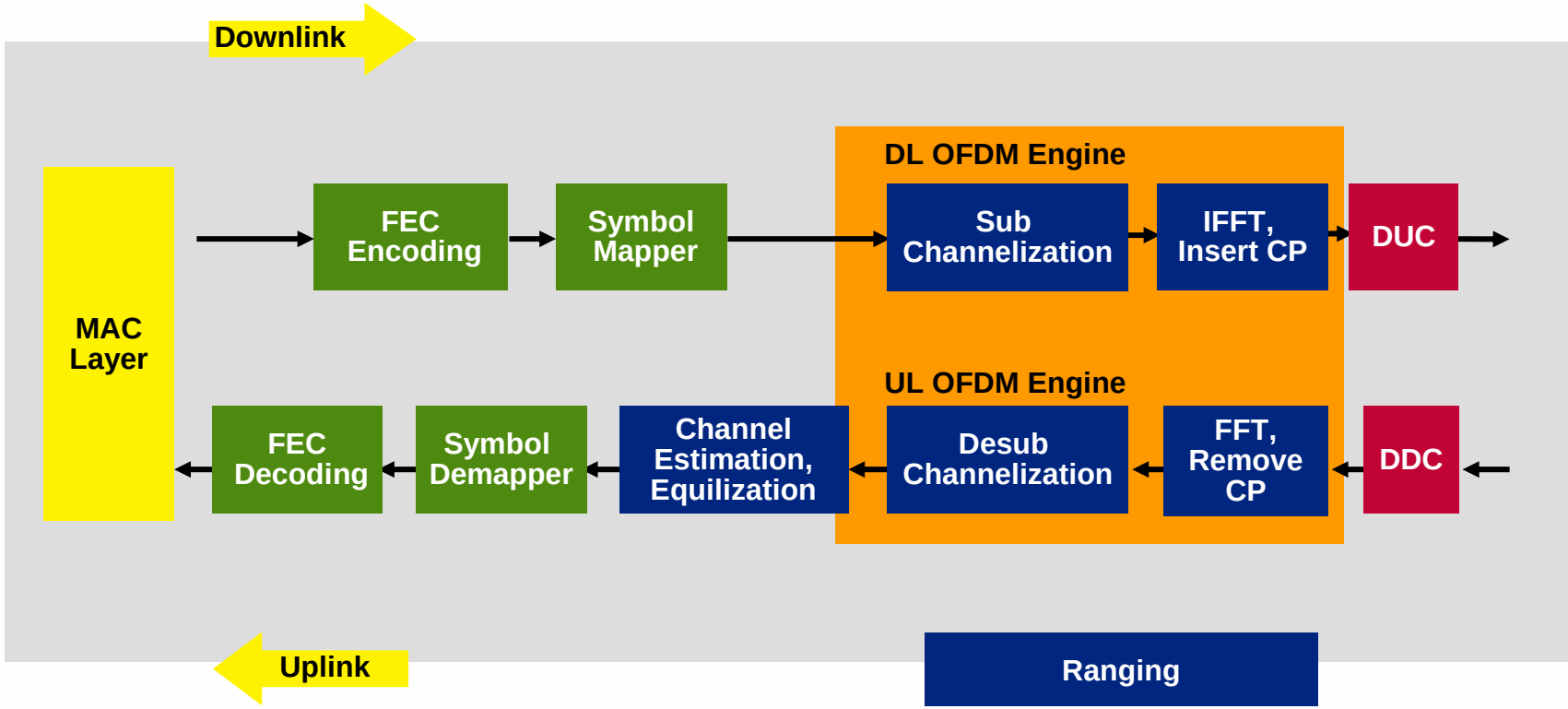
Accelerate Software Execution

- Example: CRC Algorithm (64 Kbytes)

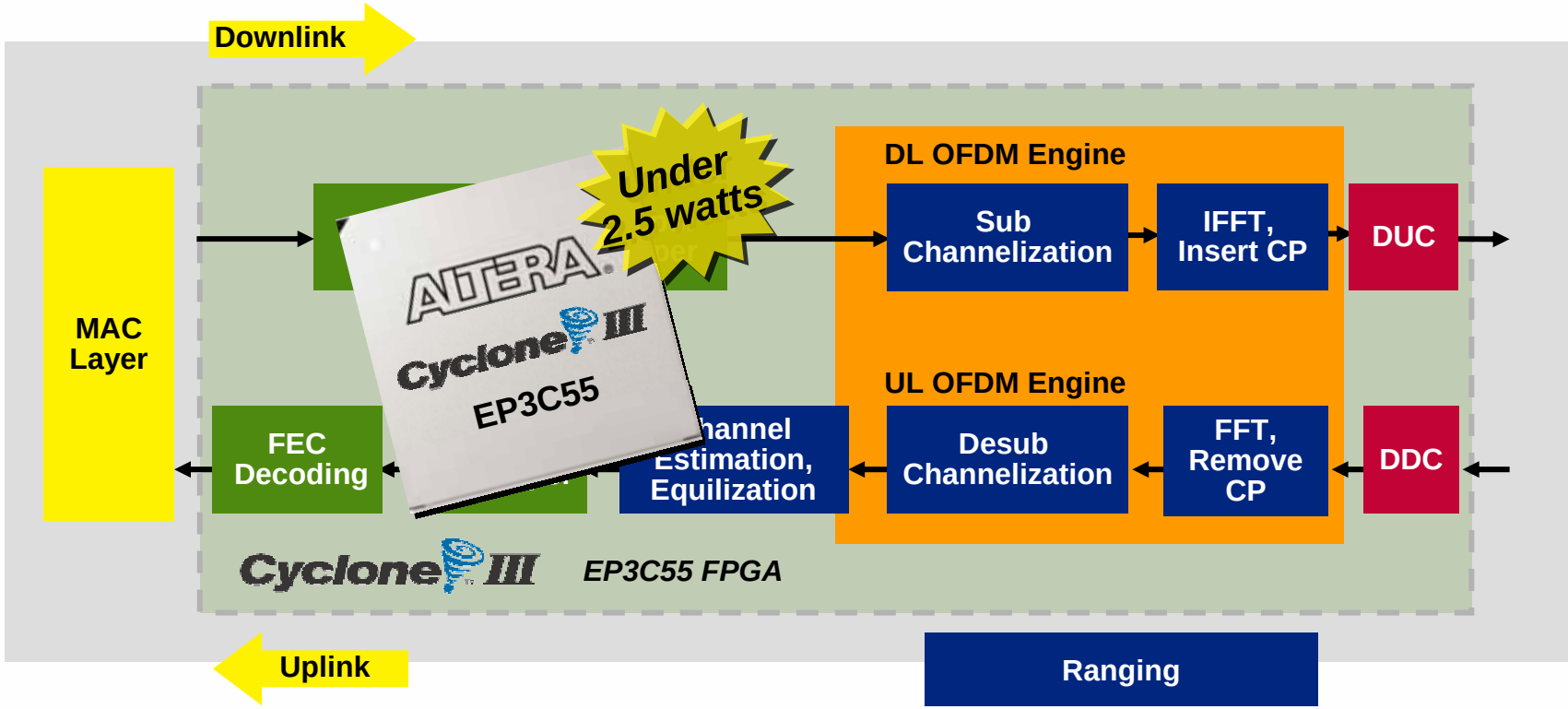


Implementation Examples and Resources Available

WiMAX Pico-Cell Base Transceiver Station



Enabling the Highest Integration



Abundant Memory, Multipliers, and Logic To Do More For Less

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Wireless Applications Resources

- Altera and partner intellectual property (IP) cores
  - FEC, FFT/IFFT, FIR, NCO, CIC, and more
- Low-cost FPGA Starter Kit, Cyclone III Edition
- *Design Low-Cost, Low-Power Wireless Systems with New FPGAs* QuickCast
- *Using Cyclone III FPGAs for Emerging Wireless Applications* white paper

www.altera.com/cyclone3-markets

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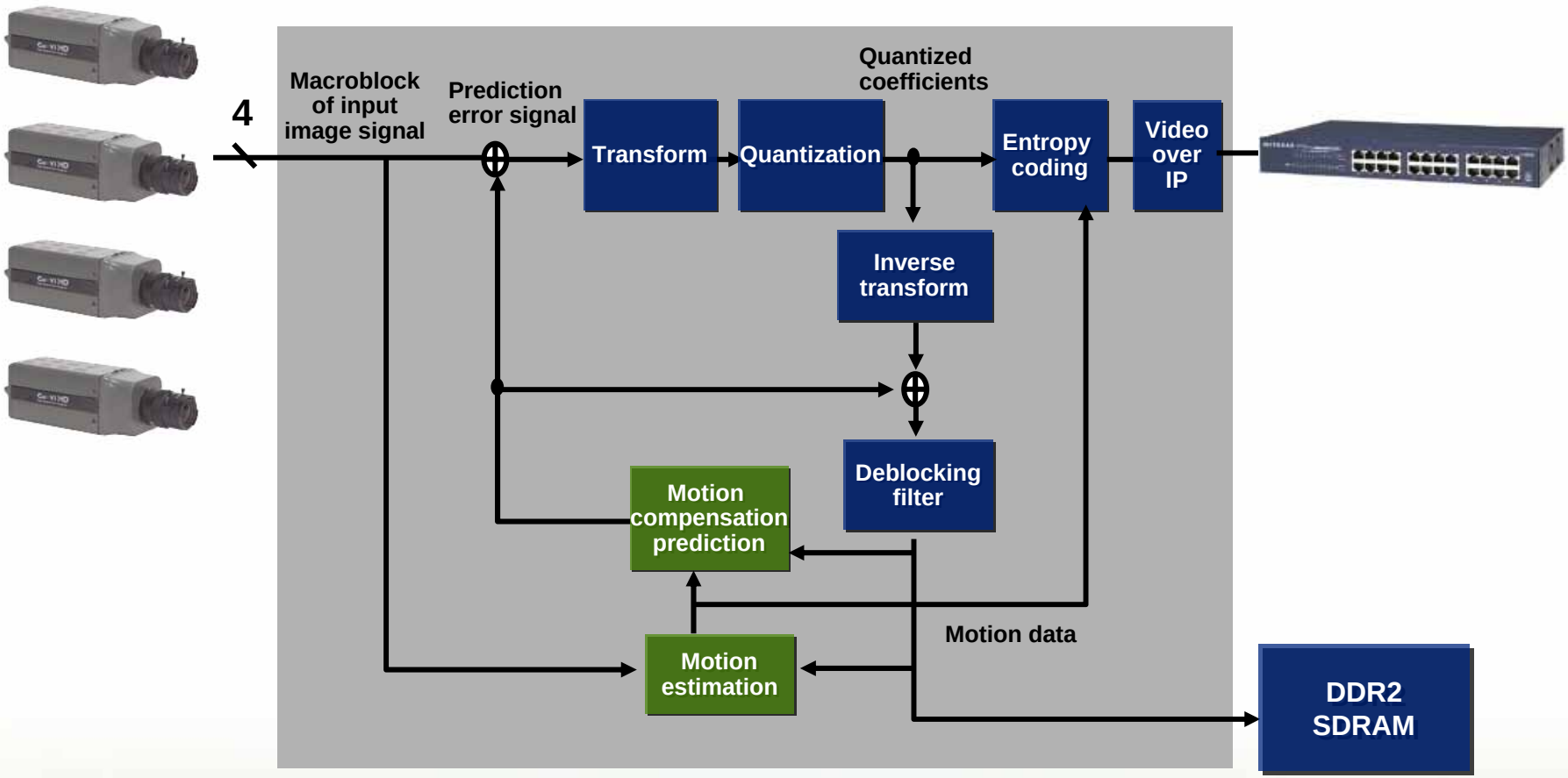
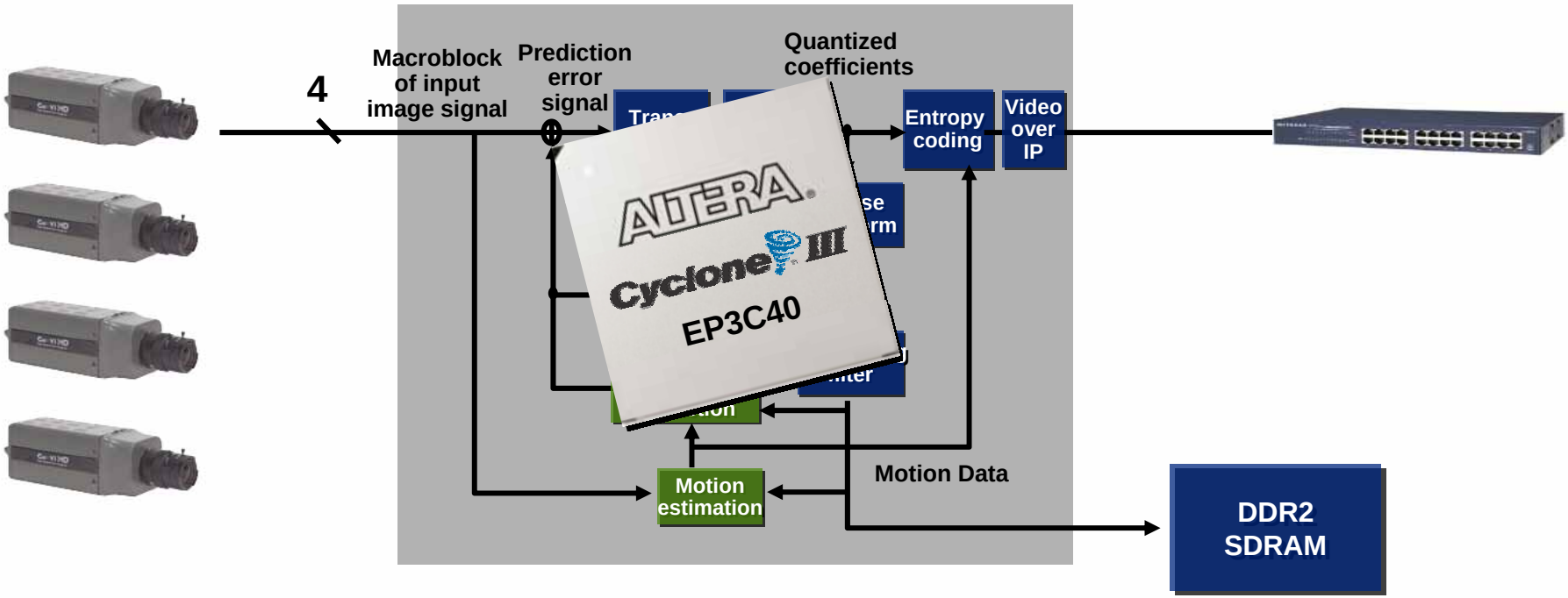
H.264 Encoder Block Diagram



Processing-intensive blocks

Enable Low-Cost H.264 Encoding



Processing-intensive blocks

Implement SD H.264 Encoder in a Single Device for Under ¼ W and $5 Per Channel

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Video and Image Processing Resources

- Video and image processing IP
  - Library of nine common video and image processing functions from Altera
  - Compression IP available from Altera partners including ATEME, Barco, 4i2i, and CAST
- Video processing reference design
- Video training course
  - Advanced DSP design: using FPGAs to architect and optimize a video and image processing system
- Low-cost FPGA Starter Kit, Cyclone III Edition
- Video daughtercard
- *Design Video and Image Processing Systems with Low-Cost Cyclone III FPGAs* QuickCast
- White papers
  - *Video and Image Processing Design Using FPGAs*
  - *Video Surveillance Implementation Using FPGAs*
  - *Medical Imaging Implementation Using FPGAs*

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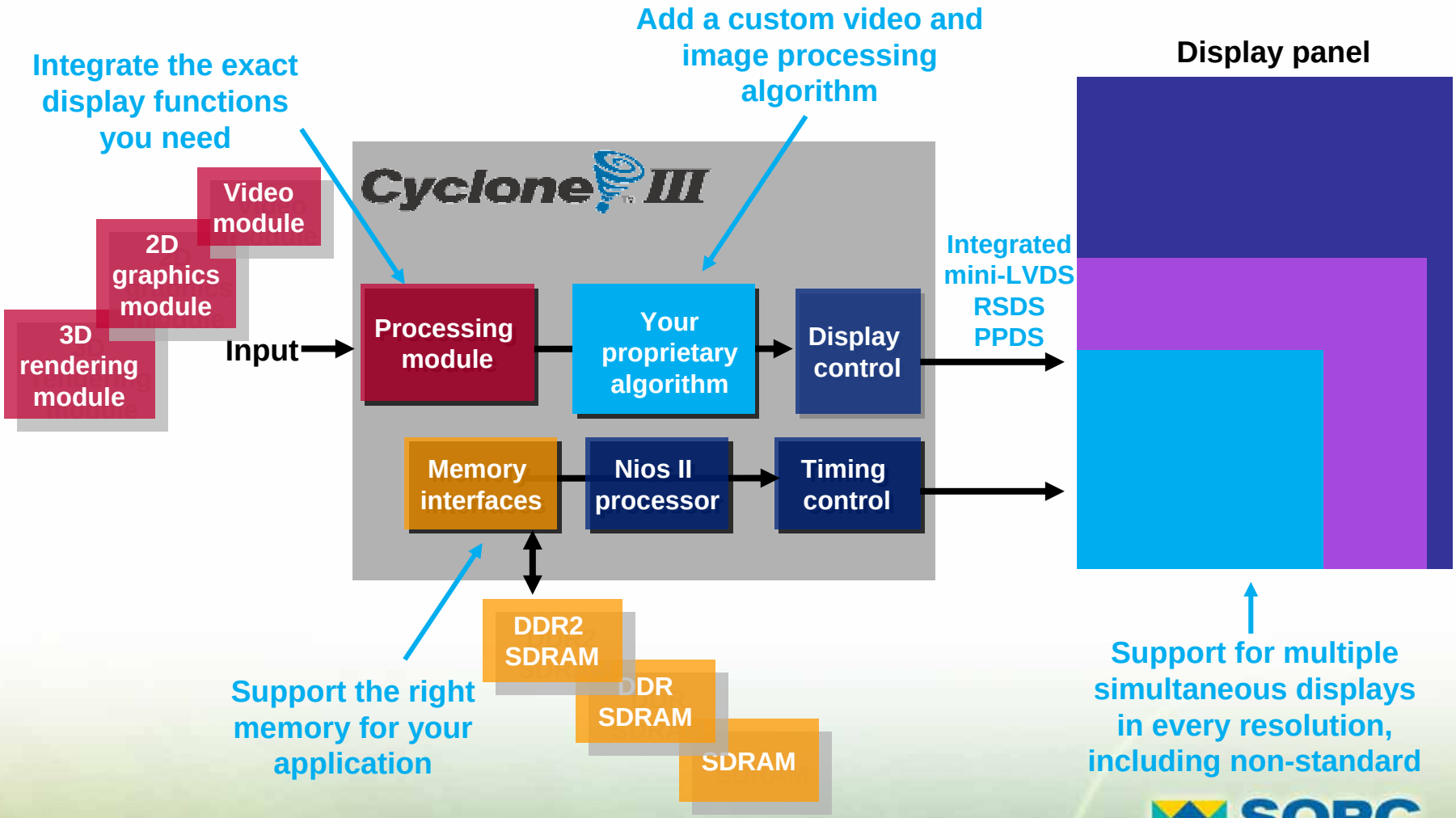
Universal, Flexible, and Scalable Display Controller



Display Application Resources

- Video and image processing IP suite
  - Library of nine common video and image processing functions optimized for Altera FPGAs
- Video processing reference design
- Low-Cost FPGA Starter Kit, Cyclone III Edition
- Microtronix ViClaro II HD Video Enhancement Development Platform
- *Develop a Display System Using Low-Cost Cyclone III FPGAs* QuickCast
- White papers
  - *Cyclone III FPGAs Enable a New Class of LCD HDTVs*
  - *A Flexible Architecture to Drive Sharp Two-Way Viewing Angle and Standard LCDs*
  - *Satisfy the Demand for Rapid Feature Enhancement in Consumer Display Products*

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eCos RTOS

- Commercial port from eCosCentric
  - Open source RTOS
    - Designed for deeply embedded applications
    - Configurable down to 10s of Kbytes
    - Commercially supported and maintained
      - Support and maintenance contract in place for Nios II embedded processor v7.1 and v7.2

eCosPro Starter Kit (Free Version)

- Available for download from eCosCentric website
- Features:
  - eCos kernel and hardware abstraction layer (HAL)
  - ISO C and math libraries
  - Memory-based file systems
  - RedBoot bootloader
  - BSP support for on-board LAN91C111 Ethernet, RS232, and flash devices (Cyclone II and Stratix® II kits)
  - Debug connections: USB Blaster (JTAG), Ethernet, and serial
  - eCos RTOS graphical configuration tool
  - Windows and Linux host development support
  - POSIX compatibility layer

eCosPro Developer Kit (Paid Version)

eCosCentric

- Includes all the eCosPro Starter Kit features plus:
  - Product support
    - Incident support (bug fixes)
    - Advice line service (email support)
  - Additional peripherals
    - Triple speed Ethernet media access control (TSE MAC)
    - Watchdog timer
  - Additional software
    - JFFS2 journaling flash file system
- Additional fee-based services
  - Device driver/BSP development
  - Application consulting
  - On-site training

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Conclusion

Conclusion

- Altera FPGAs adding value to external processors
  - Focus in most common interface cores
  - Support coprocessing and peripheral expansion
  - Drag-and-drop ease of use with SOPC Builder
- 65 nm + Nios II process expands Altera's embedded market
  - New device families reduce cost, increase performance
  - New ecosystem partners added per customer demand

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Thank You!