Deliver Femtocell Basestations Quickly and Cost Effectively with Altera HardCopy Structured ASICs

Agenda

- Femtocell overview
  - Benefits and challenges
- Enabling low-cost, low-risk, fast time-to-market femtocell designs
  - HardCopy® structured ASIC product overview
  - Femtocell design using HardCopy structured ASICs
  - Supporting intellectual property (IP) and reference designs
- Summary

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A Complete Solutions Portfolio

ALTERA.

MAX Series — *CPLDs*

Cyclone Series — *Low-cost FPGAs*

Stratix Series — *High-density, high-performance FPGAs*

Arria Series — *Low-cost Transceiver FPGAs*

HardCopy Series — *Structured ASICs*

Nios II — *Embedded soft processors*

 — *Intellectual Property (IP)*

QUARTUS II — *Design software*

 — *Development kits*

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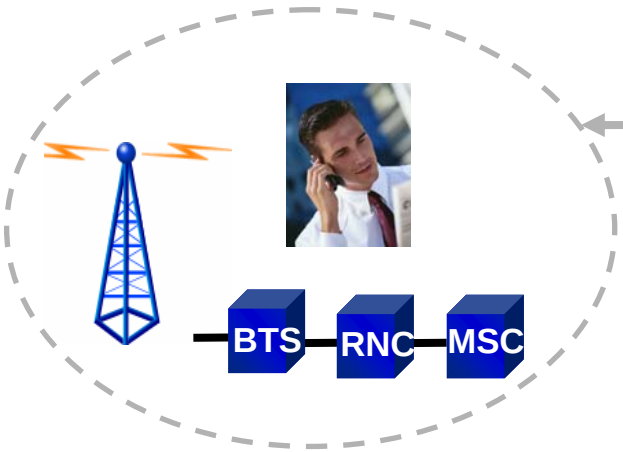
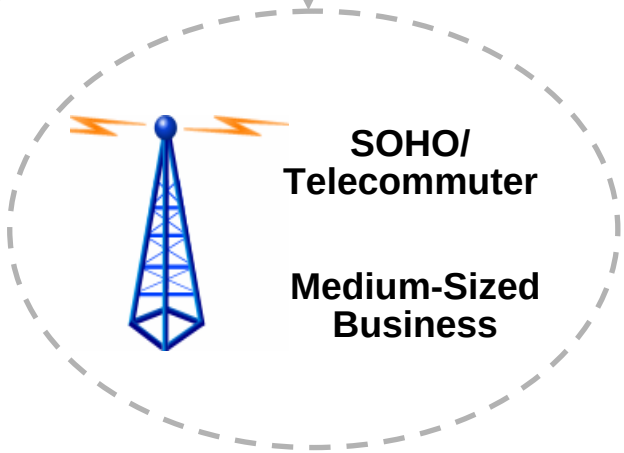
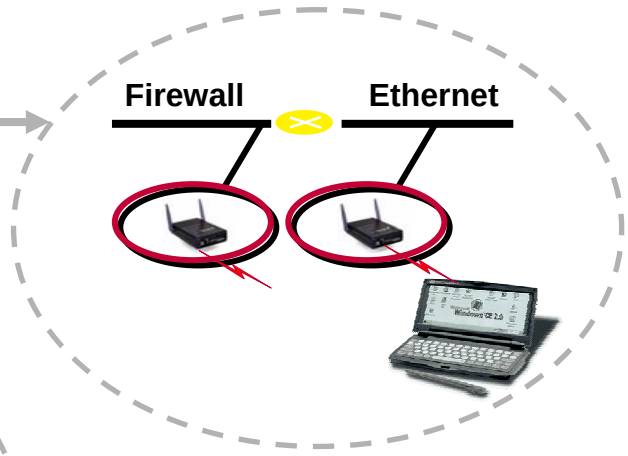
Altera's Wireless Market Focus







Mobile Infrastructure

- BTS/NodeB/AP
- BSC/RNC
- aGW
- SGSN, GGSN, MGW
- RRH

Broadband Wireless Access

- WiMAX basestations and CPE
- Broadband microwave

Indoor Coverage

- Femtocell access point
- Pico BTS

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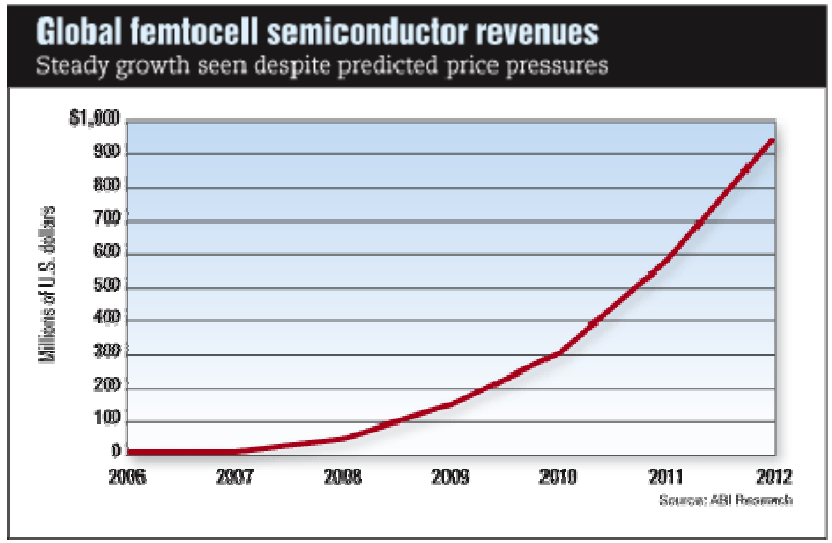
Femtocell Overview

- Femtocell benefits for mobile operators
  - Extend service coverage inside the home
  - Capture wireline minutes
  - Offload traffic off the macro network
  - Decrease backhaul costs
  - Stimulate 3G services uptake, ensure higher ARPU
  - Lower customer churn
  - Defend against VoIP erosion
  - Provide FMC services → bundling
  - Practical and attractive option for a fixed mobile convergence offering
  - Reuse existing 3G handsets (no need for dual-mode WiFi/3G handsets)



Source: ABI Research

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Challenges to Building a Femtocell

- Technical:
  - Small form factor for home use
  - Thermal engineering
    - Power is not an issue (plug into wall), but heat generation is
  - High performance within cost budget
  - Challenging network architecture
    - RF interference and power control
    - Network synchronization
    - Core network integration
- Business:
  - Emerging market
    - Uncertainty of adoption rate (how fast will it take off?)
  - Equipment costs (device pricing)
    - WiFi-like cost... $100 target pricing for residential customer
    - <$50 BOM in late 2008
  - Fast product launches and short development cycles
    - Suppliers race to capture contracts with carriers

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Addressing the Femtocell Design Challenges using HardCopy Structured ASIC Technology

The only FPGA company with structured ASICs

- Low price points
- High performance
- Low power

The only structured ASIC company with FPGAs

- Small up-front investment
- Fast turnaround time
- Guaranteed success

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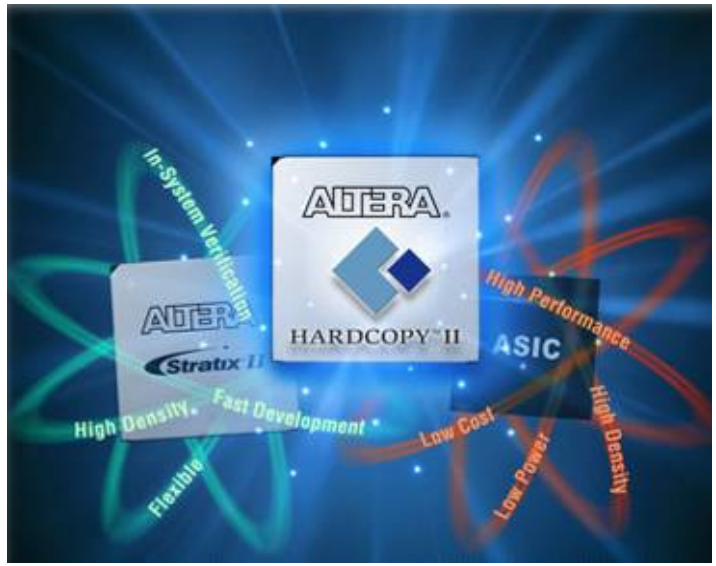
HardCopy II Structured ASICs—Built for Low Cost

- $15 for 1M ASIC gates
- 50%+ core power reduction from Stratix® II FPGA prototype
- Over 350-MHz system performance
- Up to 2.2M ASIC gates



Structured ASIC With Unique FPGA-Based Design Methodology

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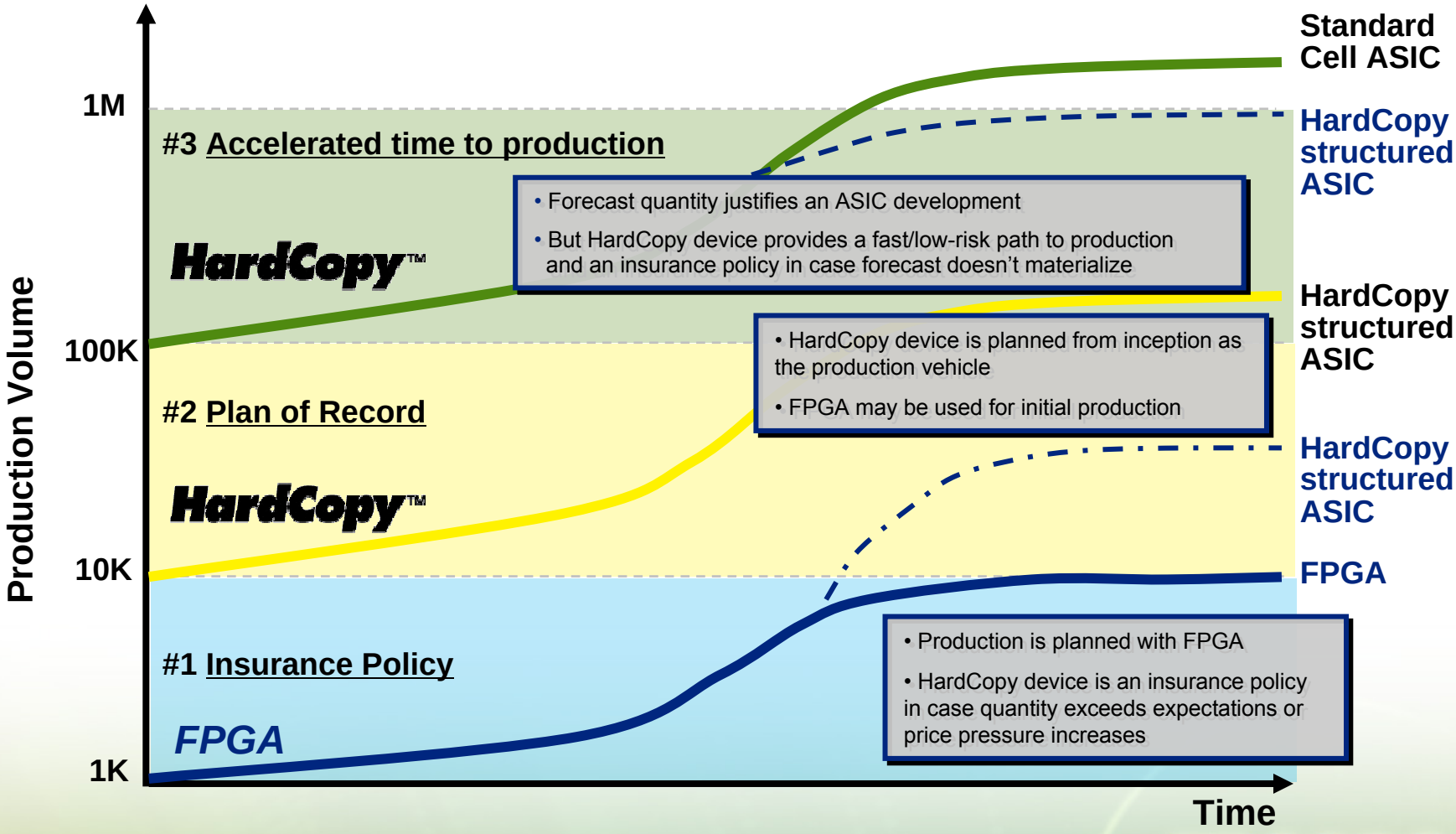
HardCopy Usage Models



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Fastest Time-to-Market

ASIC Development

- RTL design
- Verification
- Placement and routing + final verification
- Prototyping
- Verification and qualification
- Production

HardCopy Development

- Migration
- Prototyping

***With in-system verification**

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HardCopy Series Benefits

Silicon

- 50% faster than FPGA
- Up to 70% lower core power than the FPGA
- 60% to 85% smaller die

Packaging

- Pin-to-pin compatibility with FPGA
- Low-cost production packaging
- No printed circuit board respins

Software

- Unified FPGA and HardCopy design environment
- Power and performance management tools
- Inexpensive and easy to use

Turnkey Migration

- No test vectors
- No backend simulation or logic verification

Proven Methodology Minimizes Risk

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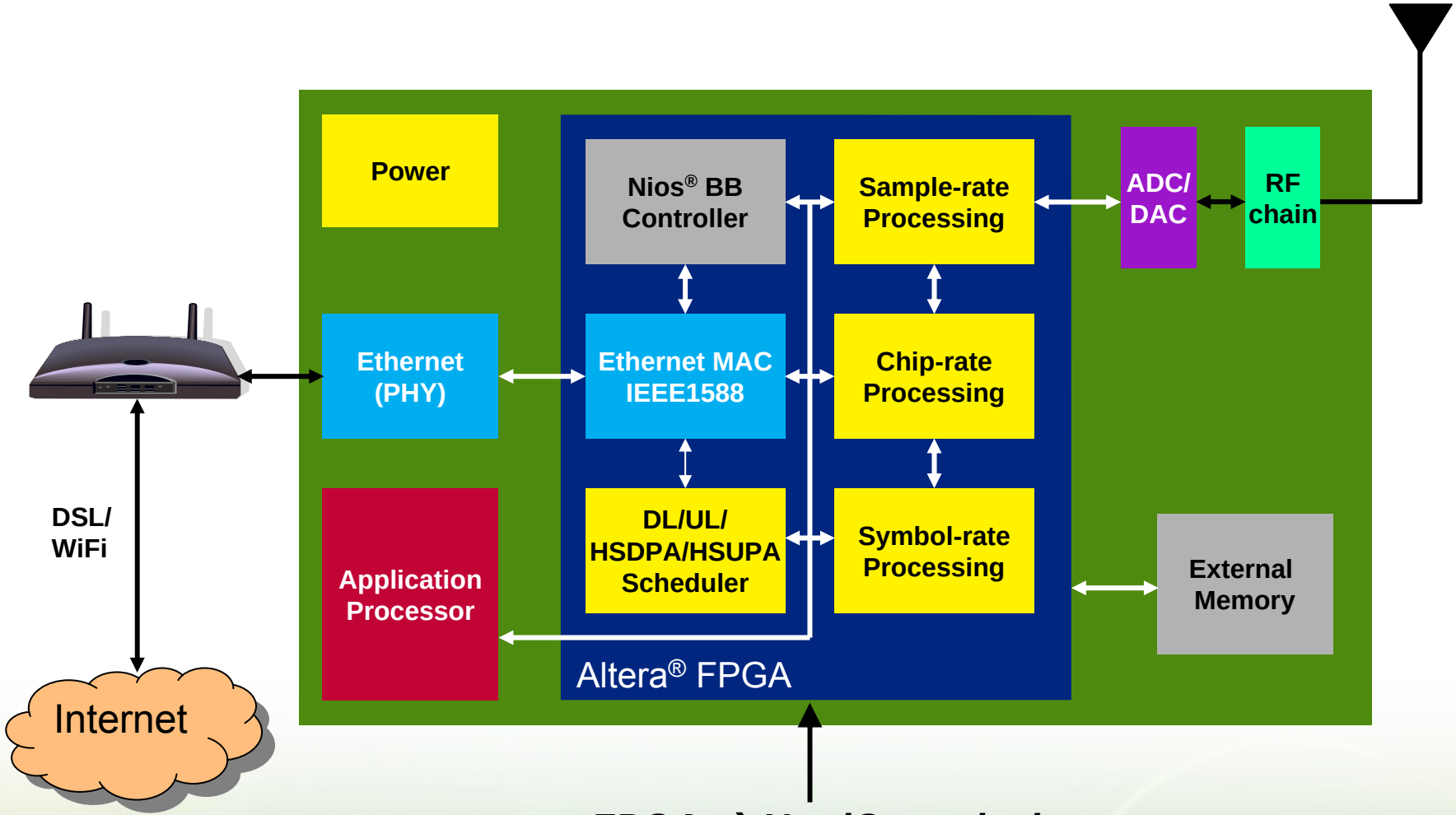
Femtocell Architecture Example –WCDMA/HSxPA



System Partitioning – 3GPP WCDMA/HSxPA

- FPGA/HardCopy structured ASIC
  - DUC, DDC, AGC, power meter
  - (De)-scrambling/spreading/modulation, including HSxPA
  - FEC: convolutional and turbo, including HSxPA
  - Rate matching
  - Physical channel mapping
  - Rake/searcher/MRC/channel estimation
  - DL/UL scheduling including HSxPA
  - IPSec enscryption accelerators/crypto-engines
  - Network timing synchronization (IEEE1588, NTP)
- Application processor
  - OAM
  - Frame protocol termination
  - Control-plane processing
  - IMS/SIP signalling and protocol handling
  - MAC/RLC/RRC/MSC/xGSN: collapsed stack processing

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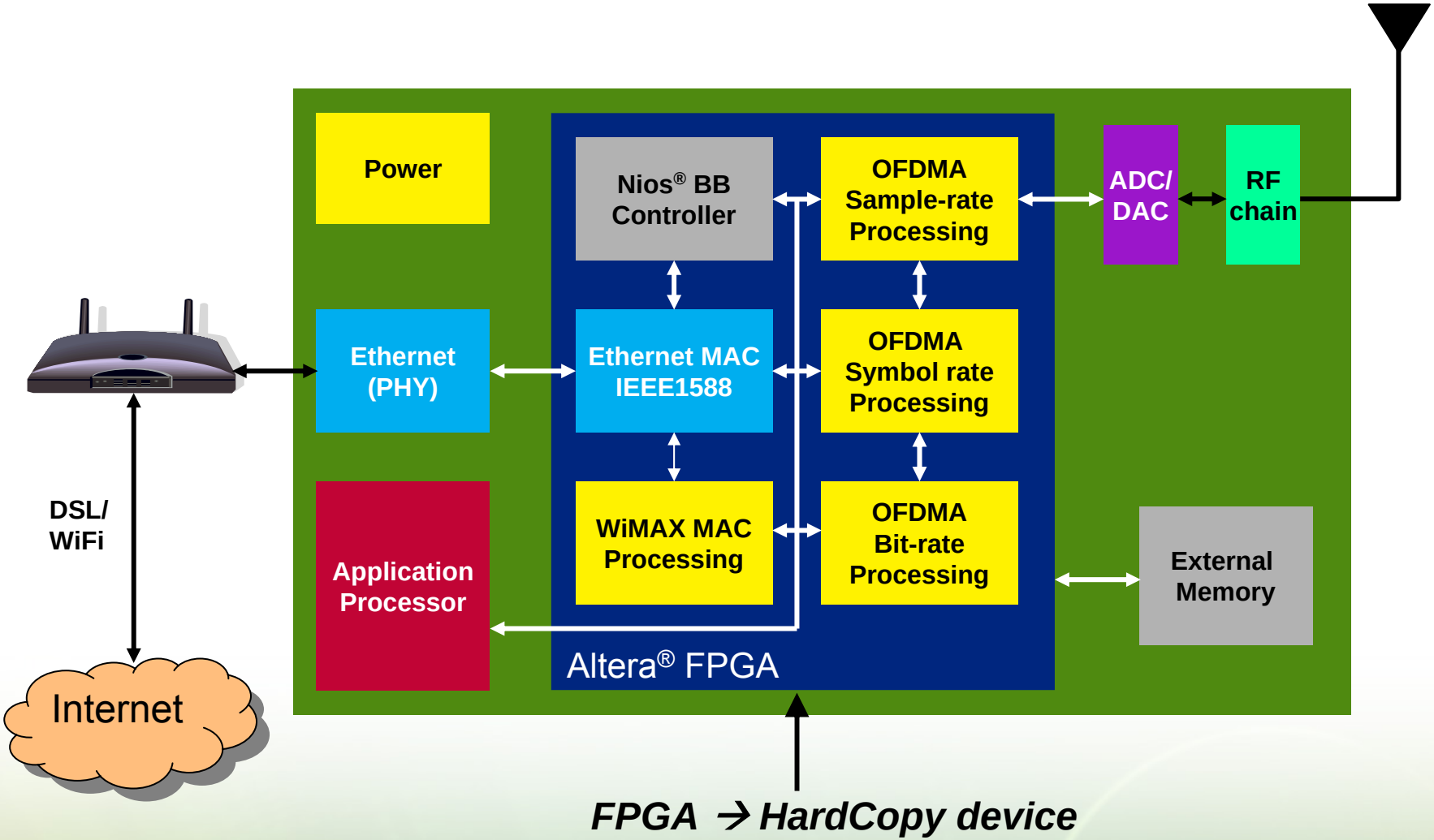
Femtocell Architecture Example – Wimax 802.16e



System Partitioning – Wimax 802.16e

- FPGA/HardCopy structured ASIC
  - DUC, DDC, AGC, power meter
  - Ranging
  - Channel estimation, channel equalization
  - OFDMA engine
    - Pilot insertion/extraction
    - Subchannelization/extraction
    - FFT/IFFT/CP
  - Symbol (de)-mapper
  - FEC
  - IPSec enscryption accelerators/crypto-engines
  - Lower MAC
  - Network timing synchronization (IEEE1588, NTP)
- Application processor
  - OAM
  - Host processing
  - Access controller
  - IMS/SIP signalling and protocol handling (VoIP – SIM/IMS)
  - TCP/UDP
  - Upper MAC/scheduler

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Significant CDMA and OFDMA IP Expertise

Standard	Altera IP and reference designs	Partner IP and reference designs
3GPP Release 6	■ HSDPA and HSUPA channel coding coprocessor ■ WCDMA DUC and DDC for macro, Pico BTS	■ HSDPA and HSUPA turbo encoder and decoder ■ Connectivity: CPRI 2.0, OBSAI RP3-01 ■ Radio card: crest factor reduction, digital predistortion
WiMAX	■ Reed-Solomon encoder/decoder ■ Viterbi decoder ■ CORDIC ■ FFT/IFFT compiler ■ Scalable OFDMA engine ■ Channel estimation ■ Channel equalization ■ OFDMA ranging ■ Symbol mapper/demapper ■ Single and multi antenna DUC and DDC ■ PAPR reduction, i.e CFR	■ Turbo convolutional code ■ Turbo product code ■ Complete 802.16e PHY and MAC ■ CPRI 2.0 ■ OBSAI RP3-01

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Other IP Offerings: Altera and Ecosystem

IP type	IP description	Offered by
Processor	Nios II embedded processor	Altera
	Network stack: TCP/IP NicheStack Network Stack, Nios II edition	Altera/InterNiche
	OS: MicroC/OS RTOS	Micrium
Memory controller	DDR2 memory controller (up to 266 MHz integrated PHY and controller)	Altera
	DDR2 high performance controller (up to 333 MHz)	Altera
Ethernet MAC	Low LE count Triple Speed Ethernet MAC (configurable to only 10/100)	Altera
	10/100 1000 1588 Ethernet MAC	MorethanIP
Filtering	FIR Filter Compiler	Altera
	FIR Filter Compiler	Altera
Modulation/ Demodulation	IFFT/FFT	Altera
	Numerical Control Oscillator	Altera
Error detection and correction	Reed-Solomon Encoder/Decoder	Altera
	Viterbi Low Speed Serial Compiler	Altera
	Viterbi High Speed Parallel Compiler	Altera
Encryption/Decryption	AES cryptoprocessor	CAST, Inc
	DES cryptoprocessor	CAST, Inc
	Secure hash algorithm cryptoprocessor	CAST, Inc
Network synchronization and circuit emulation	Hybrid timing generator	AimValley
	Circuit emulation with CESoPSN or SAToP	AimValley

Summary

- Femto market is nascent
  - Market uncertainty = risk
    - ASIC is high risk
  - Price expectation demands low-cost solutions
  - HardCopy technology is a strong contender
    - Low-risk, seamless migration from FPGA to low-cost structured ASIC
    - Allows quick turnaround for multiple product variants
- Reduce risk and capture a place in the femtocell market

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Thank You!