Develop a Display System Using New Low-Cost FPGAs

Agenda

- Display market dynamic and design challenge
- Key system diagrams
- Altera® Cyclone III is designed for display application
- Altera® design resources for display
- Conclusion

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Today's Displays

CRT

Rear / Front Projection:

CRT
LCD
DLP
LCOS

Thick

Thin

LCD

PDP
LCD

DLP
F-LCOS

< 40”

> 40”

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Trends in LCD TVs

- Larger (from 32” -> 50”)
- Higher resolution (from 480i -> 1080p)
- Wider color space (YCC -> xvYCC)

W-XGA+ 16:9
28”- 65”

W-XGA 15:9
17”- 32”

VGA 4:3
15”- 20”

- Flexibility for future features
- Differentiation by own brand imaging algorithm
- Competes with plasma and projection
- Goal: home theatre experience

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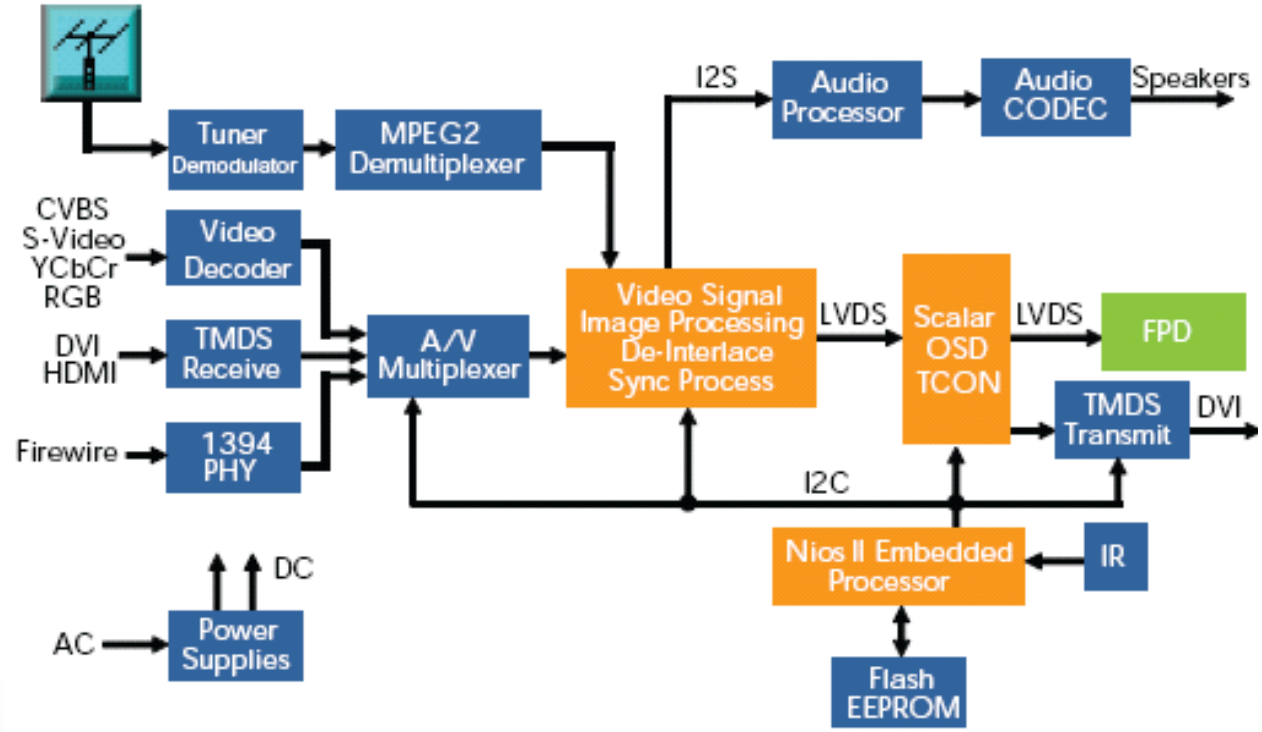
Display Design Challenges

- From SD to HD, from 32” to 60”, from YCC to xvYCC
  - → Need higher performance, low cost and lower power devices
  - → Higher flexibility for future upgrade
- How to differentiate your products?
  - → High competition in the market, a Me-too product only drive profit margin down
  - → Need to create value of imaging quality on video board to differentiate their products
  - → ASSP is not a solution here
- Should you use an FPGA or ASIC for a design?
  - Need to launch new features faster than competition
  - Uncertainty on market acceptance on new features
  - Short product life cycle

Key System Diagrams

LCD TV Block Diagram

ASSP Cyclone III FPGA



First Low-Cost FPGA that Meets 1080p HDTV Performance Requirements

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FPGA Application in FPD

- Dynamic backlight control
- Dynamic gamma correction
- Image up/down scaling
- Frame rate conversion
- De-interlacing
- Video format conversion
- LCD panel re-timing
- ….*and more*

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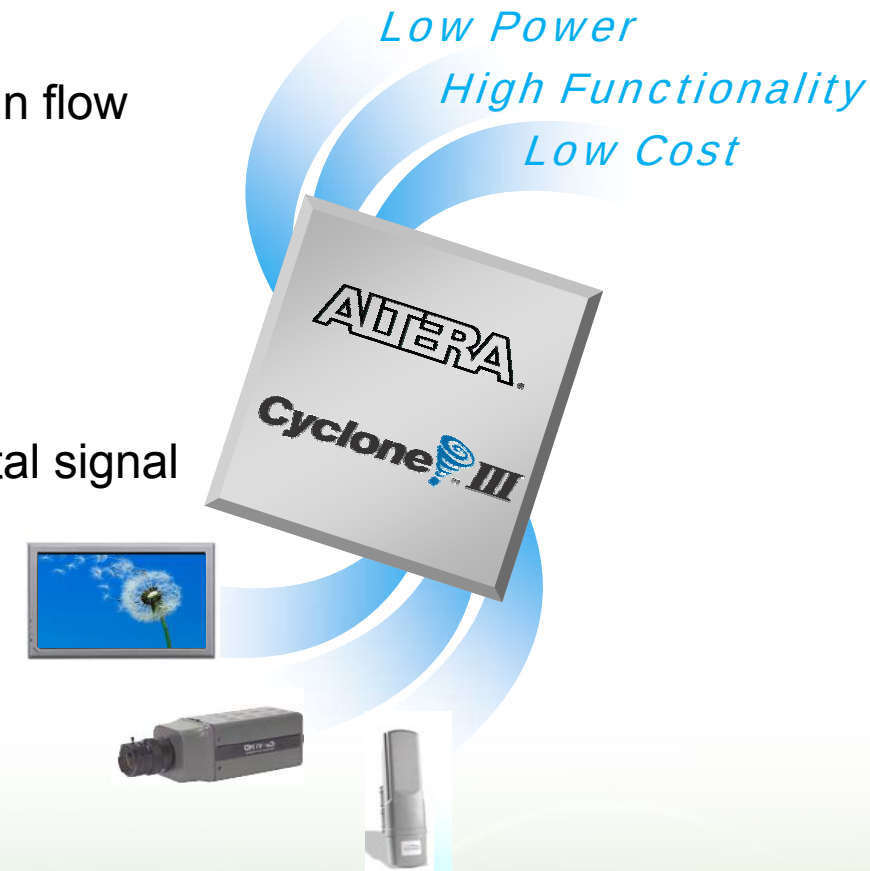
Cyclone III is Designed for Display Application

Unprecedented Combination

- Low power
  - TSMC 65-nm low-power (LP) process
  - Quartus® II software power-aware design flow
  - 120K logic elements (LEs) under ½ W
    - 1.4M equivalent ASIC gates
- High functionality
  - Densities ranging from 5K to 120K LEs
  - Up to 4 Mbits of embedded memory
  - Up to 288 embedded multipliers for digital signal processing (DSP)
- Low cost
  - First low-cost 65-nm FPGA
  - Free Quartus II Web Edition software
  - Prices starting as low as $4.00



Turn Your Ideas Into Revenue Faster

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Meeting the Needs of Emerging High-Volume Applications

- *2 – 20K logic elements (LEs)*
- *295-Kbits embedded RAM*
- *DDR support*
- *Nios® embedded processor*

2002

- *5 – 70K LEs*
- *1.1-Mbits embedded RAM*
- *150 18 x 18 multipliers for DSP*
- *DDR2 support*
- *Nios II embedded processor*

2004

- *50% lower power vs. Cyclone ® II FPGAs*
- *5 – 120K LEs*
- *4-Mbits embedded RAM*
- *288 18 x 18 multipliers for DSP*
- *Higher performance DDR2 support*
- *Nios II embedded processor*

2007

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Highest Functionality at the Lowest Cost

- Broadest range of low-cost FPGAs available
- Cyclone III FPGAs offer:
  - 2X the embedded memory
  - 2X the logic density
  - 2X the multipliers

  over the competition

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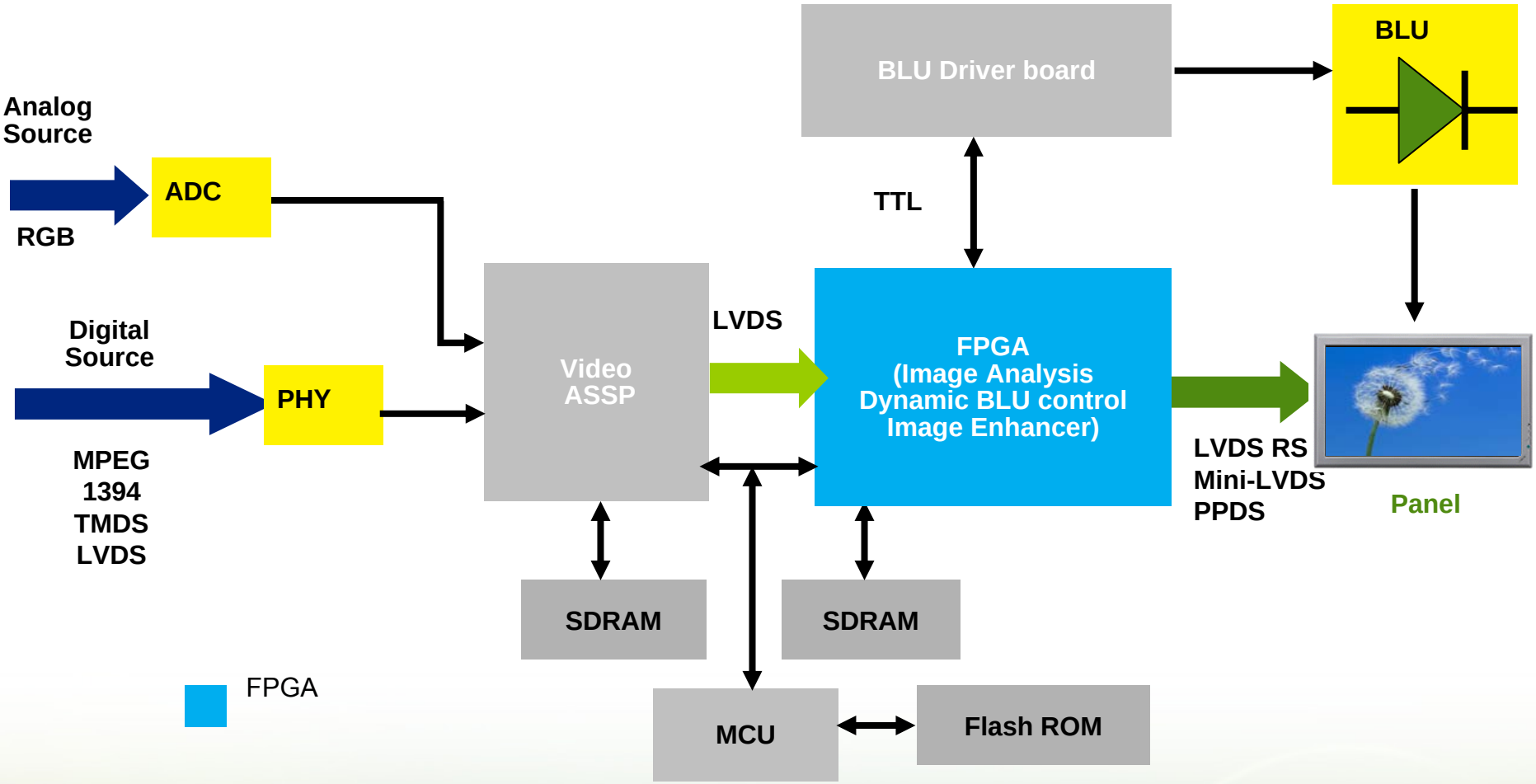
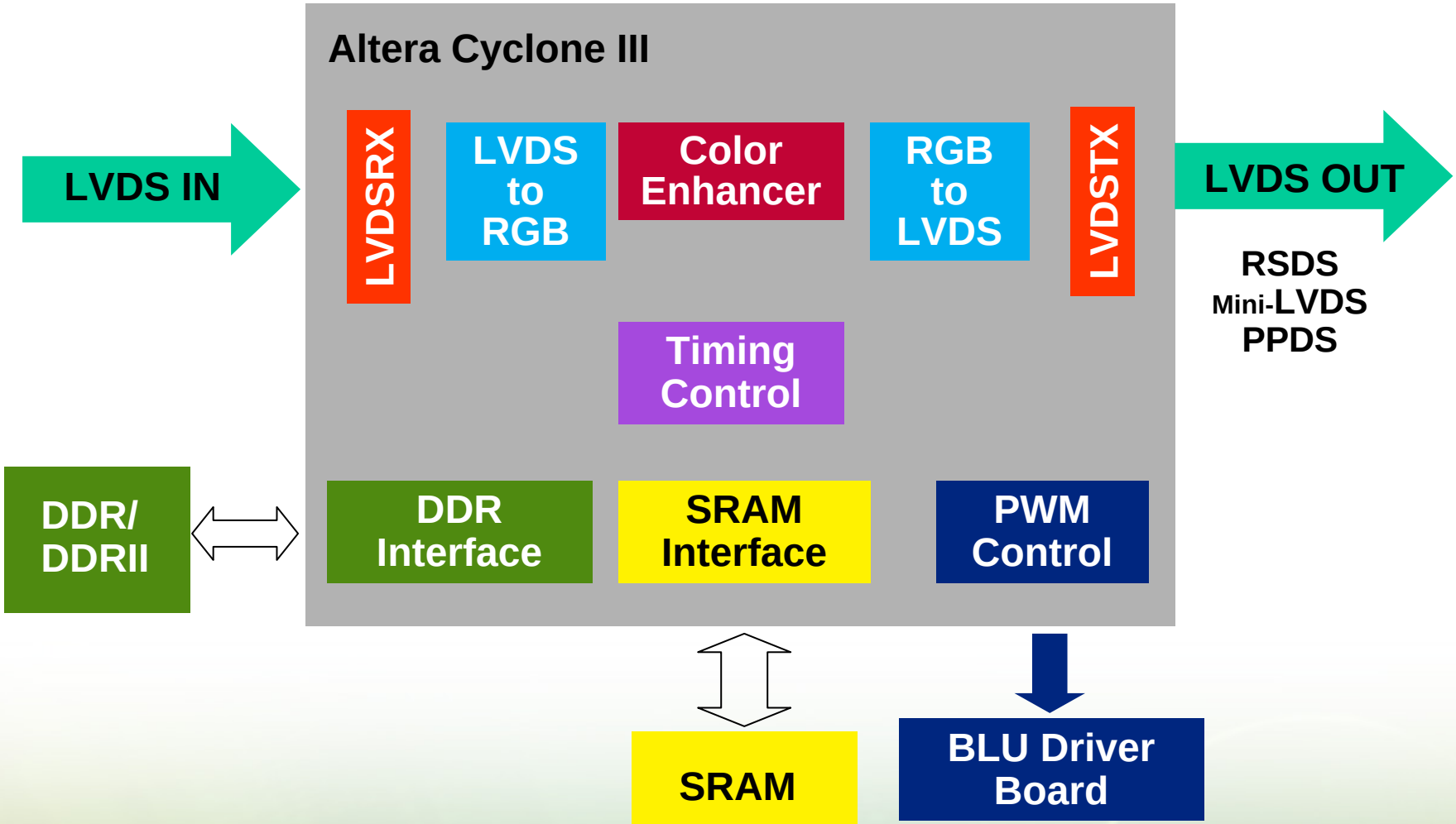
Typical Display Processing



Improve ASIC/ASSP Picture Quality and Features for as Little as $4

FPGA Application in Display



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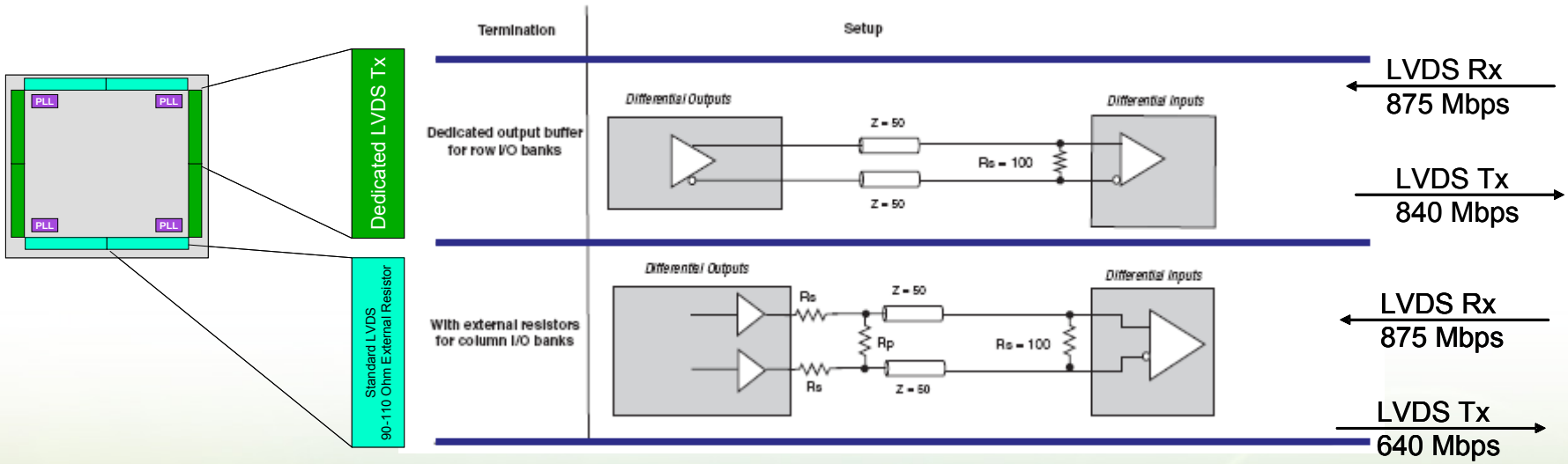
Enhanced LVDS Buffers

- Dedicated LVDS Output Buffers on the left and right banks
  - Increased performance, 840 Mbps
  - No external resistors required
- Improved LVDS Input Buffers on all banks
  - Increased performance, 875 Mbps



LVDS Pairs Reference

Package	Device	Total I/O	LVDs pairs		
			With dedicated output buffers	Without dedicated output buffers	Total
E144	3C10	85	5	7	12
	3C16	67	3	4	7
	3C25	65	4	2	6
Q240	3C16	143	17	18	35
	3C25	131	17	14	31
	3C40	111	7	7	14
F256	3C10	173	21	36	57
	3C16	151	19	24	43
	3C25	139	18	24	42
F324	3C25	196	29	42	71
	3C40	178	22	27	49
F484	3C16	329	66	62	128
	3C40	314	58	56	114
	3C55	310	61	62	123
	3C80	278	53	48	101
F780	3C40	518	110	105	215
	3C55	260	68	83	151
	3C80	412	77	92	169

Cyclone III: Supported I/O Standards

Single-Ended I/O Standards	Max	Usage
2.5V SSTL Class I and II	200 MHz	DDR SDRAM
1.8-V SSTL Class I and II	200 MHz	DDR/DDR2 SDRAM
1.8-V/1.5V/1.2-V HSTL I and II	167 MHz	QDR I/II SRAM
3.3-V PCI Compatible	66 MHz	Embedded
3.3-V PCI-X 1.0 Compatible	100 MHz	Embedded
3.3-V/2.5-V/1.8-V LVTTL	167 MHz	System Interface
3.3-V/2.5-V/1.8-V/1.5-V/1.2-V LVCMOS	167 MHz	System Interface
Differential I/O Standards	**Max**	**Comment**
LVDS	875 Mbps	High-Speed Serial
RSDS	360 Mbps	High-Speed Serial
Mini-LVDS TX	440 Mbps	High-Speed Serial
LVPECL	500 MHz	High-Speed Clocks
PCI Express*	2.5 Gbps	Per Channel
Serial RapidIO*	3.125 Gbps	Per Channel

*IP cores available, requires external PHY devices

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Video Line Buffering Application

Buffer eight lines of video in a mid-range Cyclone II device

Buffer eight lines of video in the smallest Cyclone III device

	Cyclone II device – EP2C35	Cyclone III device – EP3C5
Volume price	$18.00	$4.00

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Enhanced PLLs for Displays

	Cyclone II	Cyclone III	Advantages
Outputs per PLL	3	5	Supports multiple data rates with up to 8 additional global clocks
Min - Max Frequency (MHz)	10 – 400	5 – 440	Supports higher data rates required by high definition displays
Dynamically Configurable	No	Frequency and Phase	Dynamically adjust for changing refresh rates
Cascadable	No	Yes	Increase PCB routing flexibility, reduce jitter

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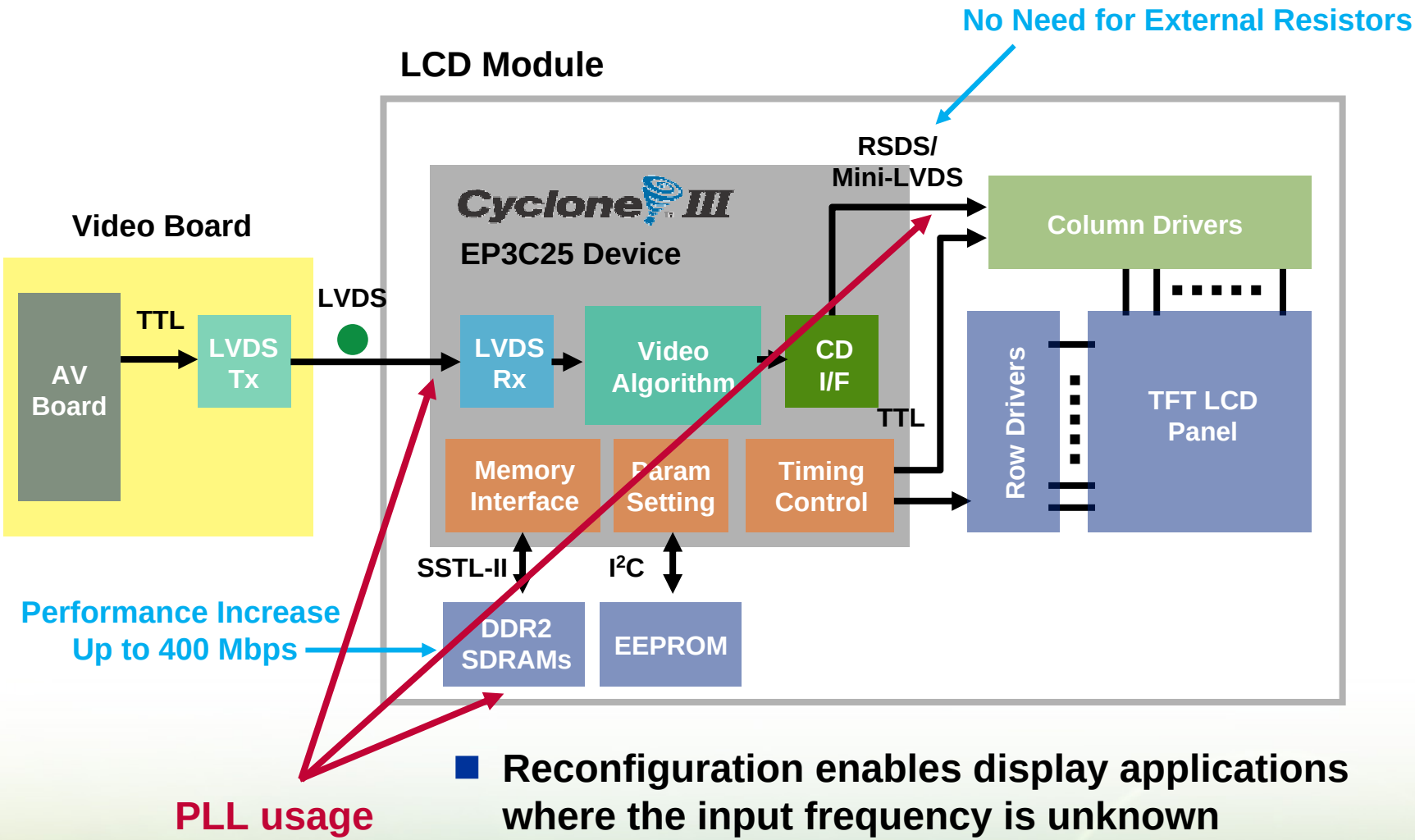
LCD TV Block Diagram



- Reconfiguration enables display applications where the input frequency is unknown

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Cyclone III External Memory Support

Memory Standards	C6 (MHz)		C7 (MHz)		C8 (MHz)		Availability
	Col I/O	Row I/O	Col I/O	Row I/O	Col I/O	Row I/O	Quartus II software version
DDR1 SDRAM	167	150	150	133	133	125	6.1
DDR2 SDRAM	200	167	167	150	167	133	6.1
QDRII SRAM	167	150	150	133	133	125	Q3 '07

- All numbers are minimum frequencies achievable; maximum frequencies pending characterization

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Cyclone III 65nm Low Power Technology

- Cyclone® III FPGAs deliver lower static and dynamic power consumption than Spartan-3 series families including the latest -3A and -3A DSP variants
  - Only Cyclone III FPGAs are designed on TSMC's 65nm Low Power Process
  - Cyclone III static power is lower than Xilinx static power in Suspend mode at 85C Tj
  - Only Cyclone III FPGAs can take advantage of Quartus® II PowerPlay optimization technology to lower dynamic power up to 25%

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Design Resources for Display

Quartus II Design Software

- Industry-leading software for performance and productivity
  - Supports all Cyclone III devices in *free* Web Edition
    - Including the EP3C120, largest FPGA in its class
- Key features
  - PowerPlay technology to reduce power up to 25 percent
  - TimeQuest timing analyzer for easy timing closure
  - DSP Builder to rapidly bring your DSP design into hardware
  - SOPC Builder to rapidly and easily build whole systems

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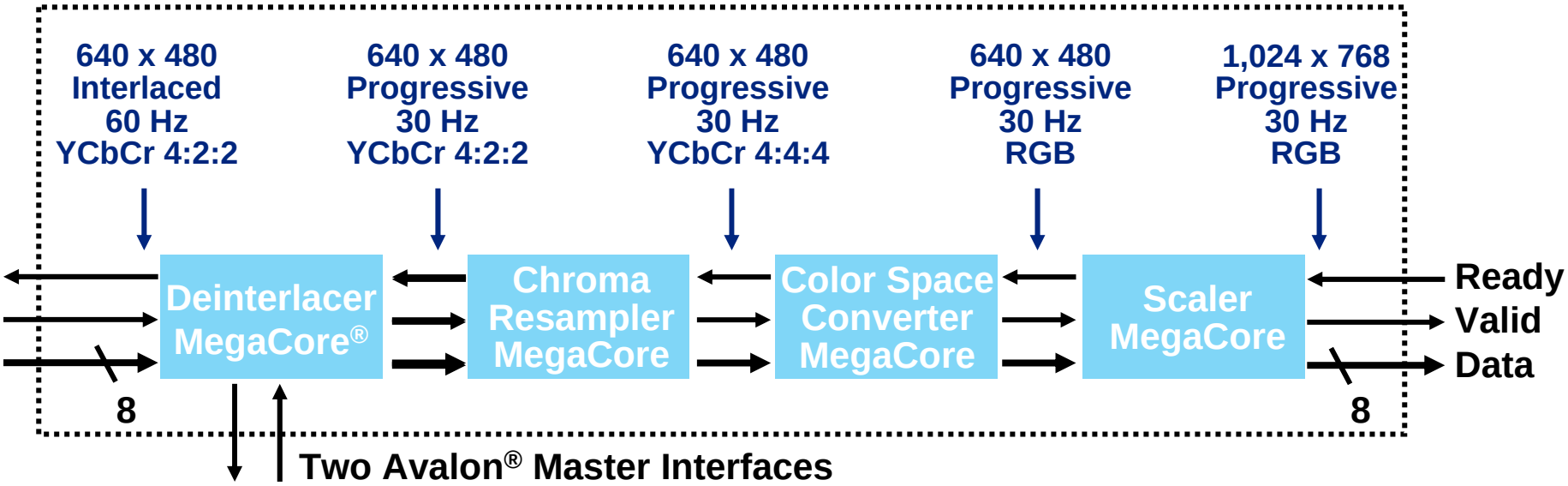
Video and Image Processing Suite

Core	Function
Deinterlacer	Converts interlaced video formats to progressive video format
Color space converter	Converts image data between a variety of different color spaces
Scaler	Resizes and clips image frames
Gamma corrector	Performs gamma correction on a color space
Alpha blending mixer	Mixes and blends multiple image streams, including picture-in-picture (PIP)
Chroma resampler	Changes the sampling rate of the chroma data for image frames
2D filter	Implements a 3x3, 5x5, or 7x7 FIR filter on an image data stream to smooth or sharpen images
2D median filter	Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Line buffer compiler	Efficiently maps image line buffers to Altera on-chip memory

- ***9 IP in one package to enable designers to kick start your own imaging algorithm !***

Video Upconversion Datapath

- Entire datapath is assembled in DSP Builder



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Nios II Embedded Processor

- Choose the *exact* set of CPUs, peripherals, and memory you need for your application
  - Achieve over 160 DMIPs of performance
  - Build custom instructions
  - Accelerate with hardware—C2H compiler automatically converts C subroutines into hardware for Nios II embedded processor

  - Low cost
    - Integrate your peripherals and microprocessor into a single chip
    - Support for multiple processors in a single device
    - Implement a processor for $0.25 of logic on a Cyclone III FPGA

Industry's Leading Soft-Core Processor

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Complete Product Solution for Display

- **MAX II use**
  - Enhancements
  - Bug Fixes
  - Interface Bridging
  - System Config
- **MAX II benefits**
  - Lowest Cost Per I/O Pin
  - Instant-On, Non-Volatile
  - Low Power Consumption
  - Reprogrammable

- **Cyclone III use**
  - Image processing
  - Timing controller
  - Data arrangement
  - Format conversion
  - Interfaces
- **Cyclone III benefits**
  - Flexible, time-to-Market
  - System integration
  - FPD I/F built-in
  - Memory I/F built-in
  - Embedded Processor

- **Stratix III use**
  - Highest logic density
  - Highest performance I/O (1.25G LVDS, 400Mhz DDRIII)
- **Stratix III benefits**
  - ASIC prototype
  - HC migration

- **HardCopy use**
  - Similar to FPGA
  - Structured ASIC
- **HardCopy benefits**
  - Risk reduction
  - Time-to-market
  - Improved performance
  - Lower power

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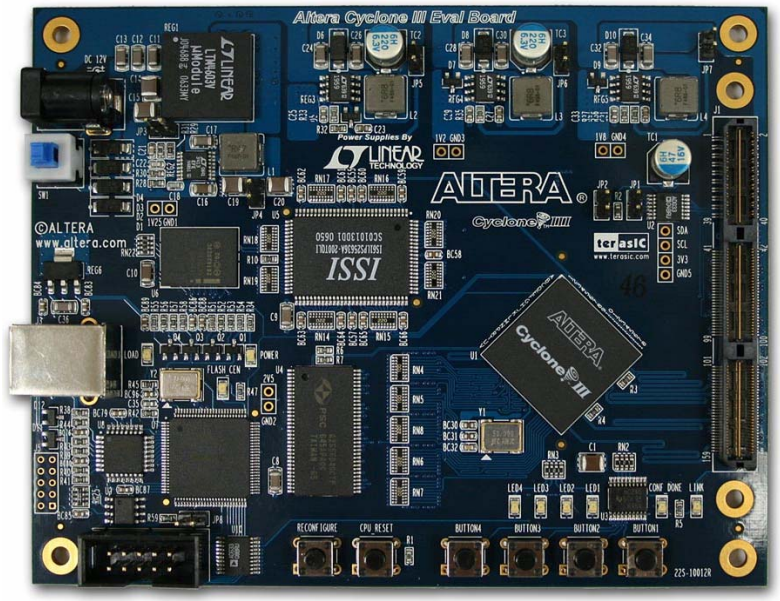
Cyclone III FPGA Starter Kit Available Now

- Full-featured FPGA board
  - Introduces the latest technology
- Cyclone III FPGA
  - Lots of Logic - 25K LEs
  - 608 kilobits of embedded RAM
  - 66 embedded 18 x 18 multipliers
  - 214 user I/O
- Built-in device programmer (USB)
- Memory Devices
  - SDRAM
  - SRAM
  - Flash
- Expandable with daughter cards through HSMC connector
- Part #: *DK-START-3C25N/P*



Get Your Design in Hardware Today

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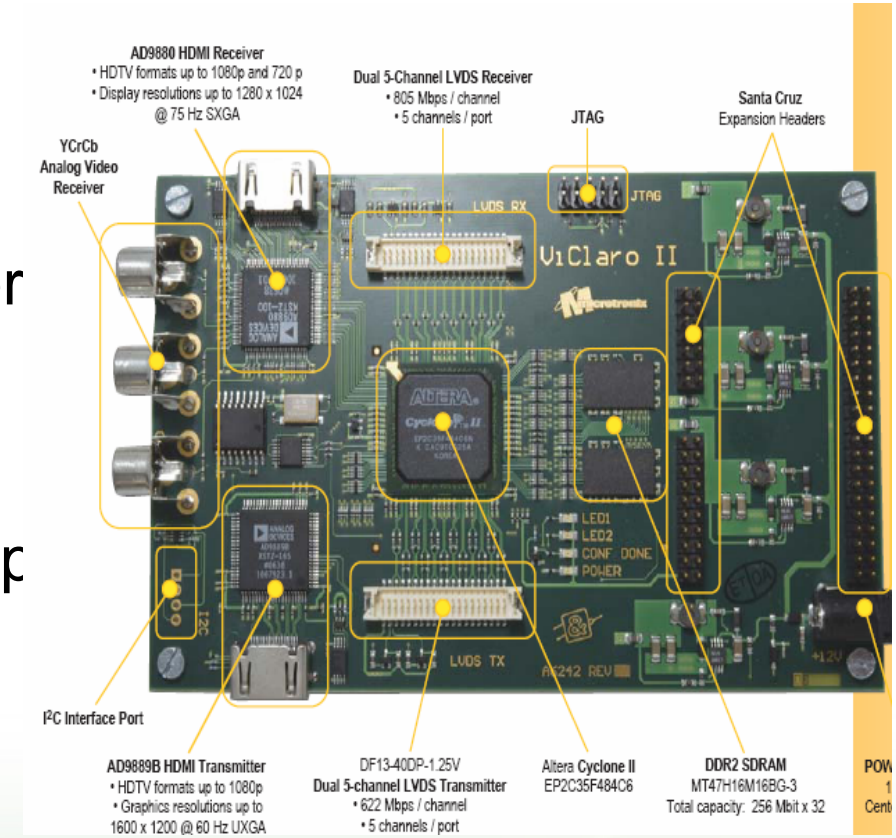
Microtronix ViClaro II HD Video Enhancement Development Platform

- Altera® EP2C35 device
- 32 bit DDR2 SDRAM
- HDMI Transmitter/Receiver
- Analog / Video Reciver
- Dual LVDS links
- Supports 720p/1080i/1080p 50/60HZ HDTV



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LET IT WAVE Bandlet Transform Technology

- Let It Wave product
  - **Built on Altera Stratix and Cyclone devices**
  - Format conversion
    - Any input scaled to the desired resolution
    - Exceptional upconversion of SD sources to the display size
    - Delivering sharp and flicker-free images
  - Picture enhancement
    - Compression artefacts reduction
    - Advanced detail enhancement for clear images
  - Other features
    - Film mode detection, aspect ratio control ...
- Let It Wave Evaluation Kit and DVD
  - Available now for evaluation

"Superior Technology Award Recipient" at IBC 2006

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Breakthrough Picture Quality: Upconversion Example

Current state-of-the art

LET IT WAVE

"The Amazing Images Produced by The Let It Wave Upconversion Process Are Reaching The Ultimate Quality Point" -- Yves Faroudja

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Other Altera® Display Application Resources

- Video and Image Processing Suite
  - Library of nine common video and image processing functions optimized for Altera FPGAs
- Video processing reference design
- *Develop a Display System Using Low-Cost Cyclone III FPGAs* QuickCast
- White papers
  - *Cyclone III FPGAs Enable a New Class of LCD HDTVs*
  - *A Flexible Architecture to Drive Sharp Two-Way Viewing Angle and Standard LCDs*
  - *Satisfy the Demand for Rapid Feature Enhancement in Consumer Display Products*

www.altera.com/cyclone3-markets

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Conclusion

Conclusion

- The display evolution requires a high performance and flexibility solution to meet today market dynamics
- Cyclone III devices deliver low power, high performance, and low cost to enable customer innovation and fast time to market
- DSP Builder, Quartus® II design software, and development kits improve productivity
- Altera® display application resources and partner solution facilitate customers' design

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Thank You!

Backup

Family Plan

Device	LEs	M9K memory blocks	Total memory (Mbits)	18 X 18 Multipliers	PLLs	Global clocks
EP3C5	5,136	46	0.4	23	2	10
EP3C10	10,320	46	0.4	23	2	10
EP3C16	15,408	56	0.5	56	4	20
EP3C25	24,624	66	0.6	66	4	20
EP3C40	39,600	126	1.1	126	4	20
EP3C55	55,856	260	2.3	156	4	20
EP3C80	81,264	305	2.7	244	4	20
EP3C120	119,088	432	3.9	288	4	20

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Package Offerings

Device	E144	Q240	F256	U256	F324	F484	U484	F780
	0.5 mm 22 x 22	0.5 mm 35 x 35	1.0 mm 17 x 17	0.8 mm 14 x14	1.0 mm 19 x 19	1.0 mm 23 x 23	0.8 mm 19 x19	1.0 mm 29 x 29
EP3C5	94		182	182				
EP3C10	94		182	182				
EP3C16	84	160	168	168		346	346	
EP3C25	82	148	156	156	215			
EP3C40		128			195	331	331	535
EP3C55						327	327	377
EP3C80						295	295	429
EP3C120						283		531

Denotes vertical migration support

Optimized to Offer the Highest Logic, Memory, Multiplier, and I/O Resources

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