Trends in High-Speed Serial Technology

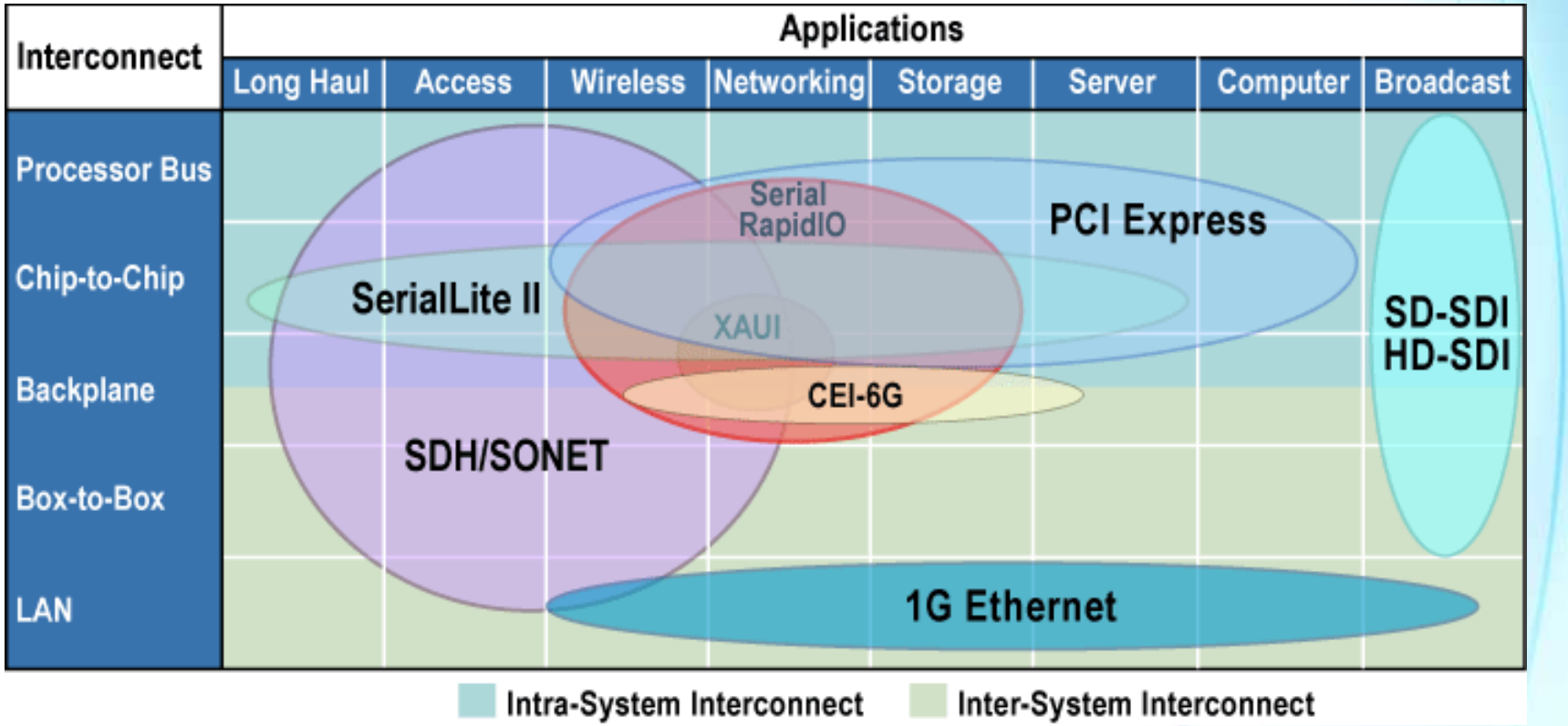
Agenda

- Trends in serial I/O protocols
- Transceiver-based FPGAs
- Success factors
- Conclusion

Market Trends

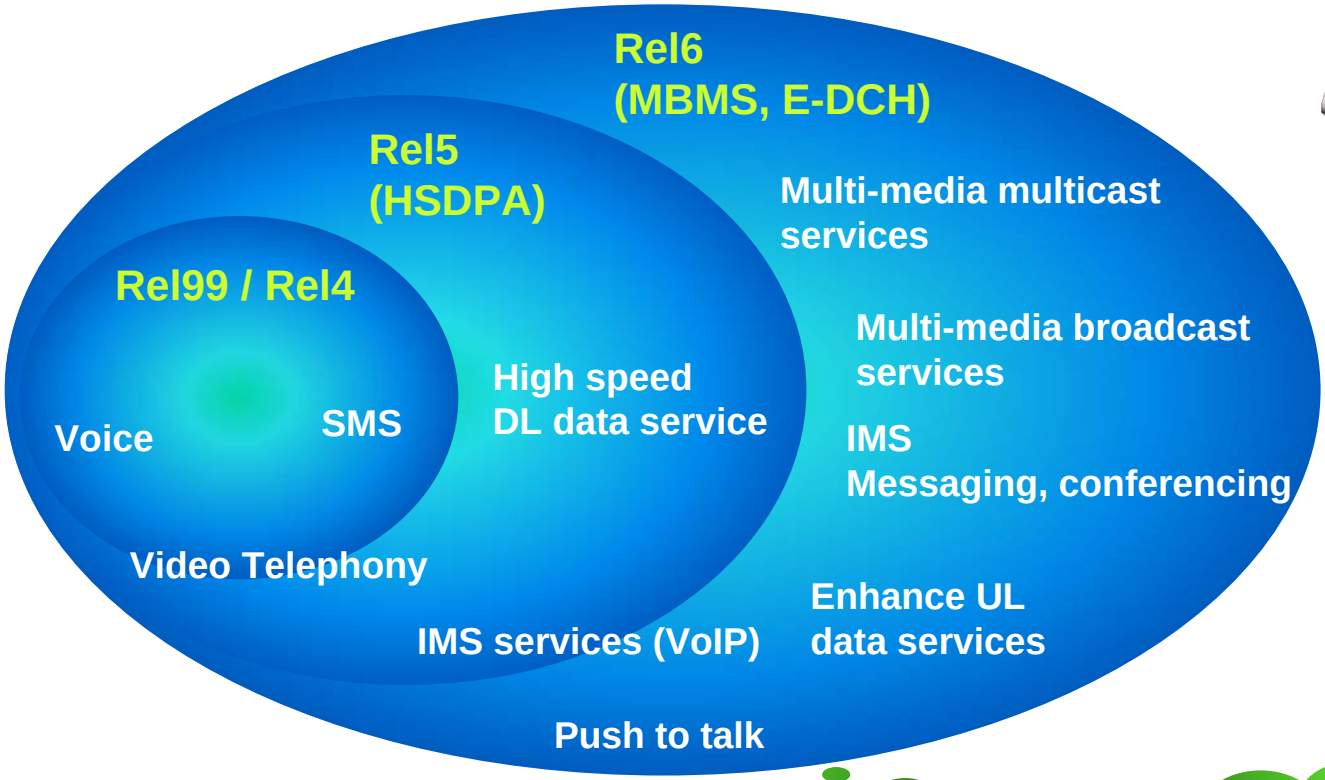
CY5

Serial Interfaces



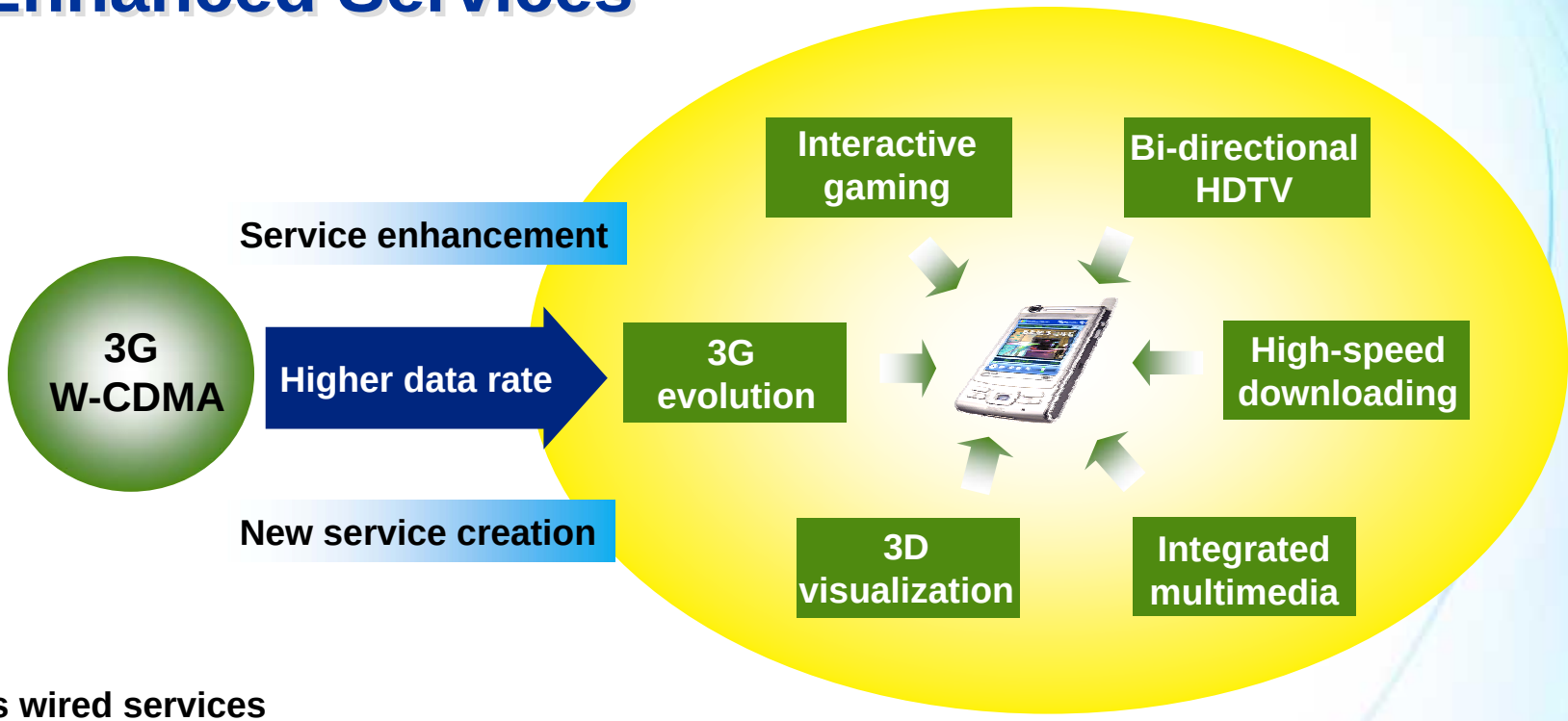
CY1

3rd Generation Partnership Project (3GPP) Evolution – Current Scenario



Key drivers for Rel5/Rel6 were *New Data Services*

3GPP Long Term Evolution Required to Enable Enhanced Services



As wired services

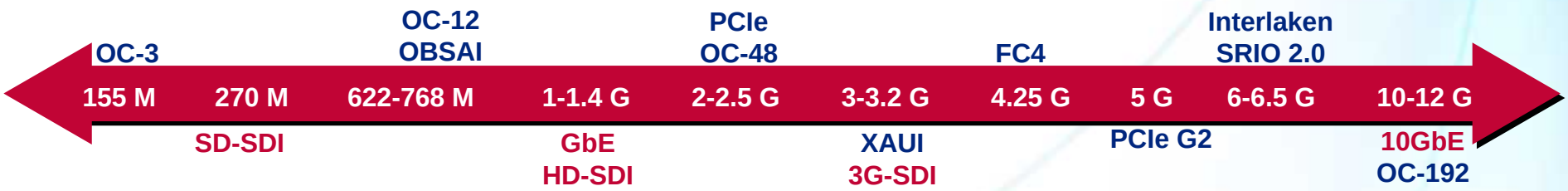
Text-based Internet services (BBS, Gopher, Usenet)	Text-oriented Web services	Basic multimedia Web services (audio, video streaming) interactive network gaming	Peer-to-peer services (Napster) Fast uploading services	VoD with HD quality Home networking
Modem (2.4 Kbps~56 Kbps)	ISDN (128 Kbps)	ADSL (1.5 Mbps~6 Mbps)	VDSL (10 Mbps~30 Mbps)	FTTH (~50Gbps)

Broadcast Market Trends – HD

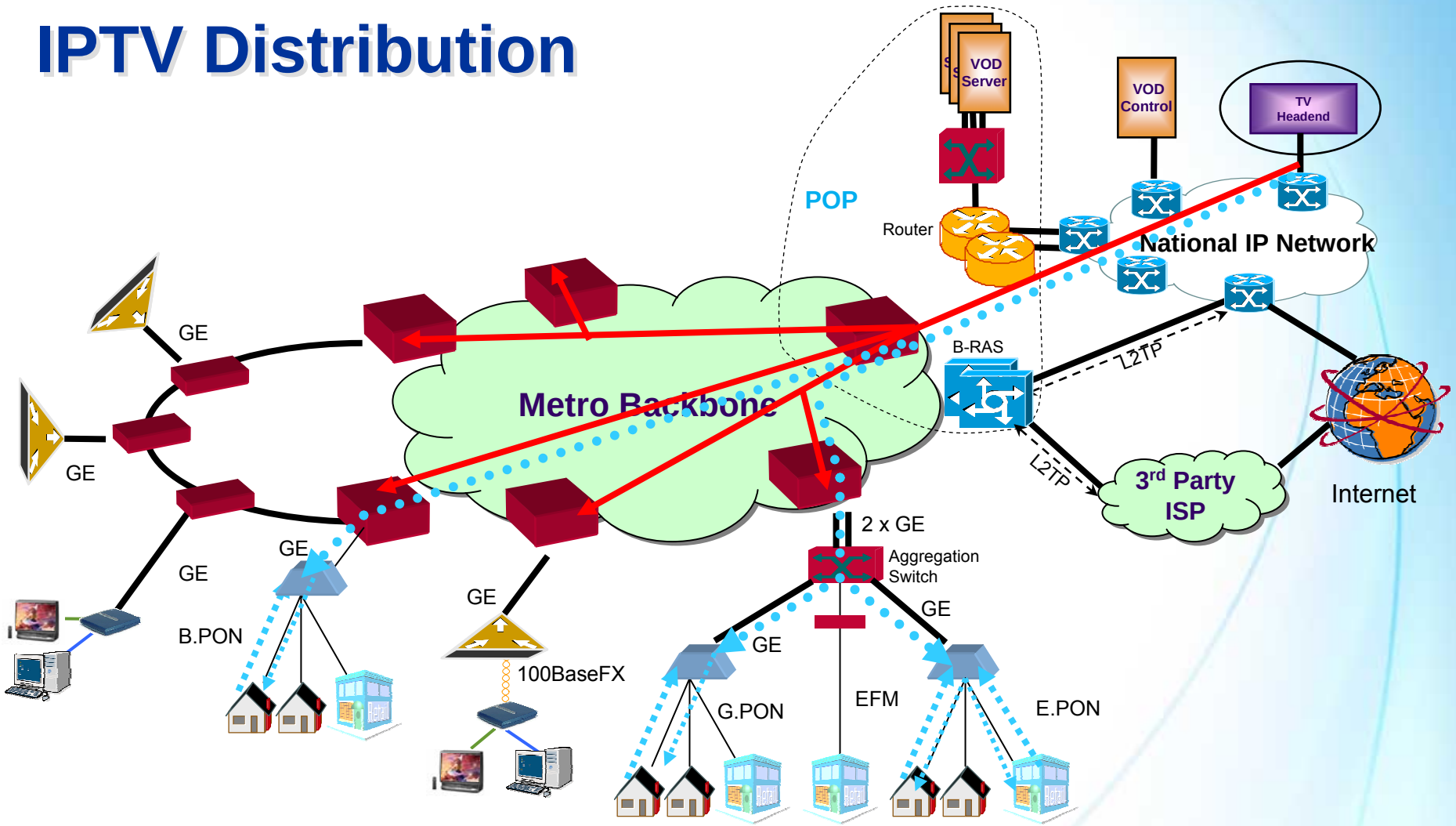
- HD perhaps as big a change as black-and-white to color transition
- Studio dilemma: Both 1080i and 720p used for broadcast, so they need to store in 1080p (or higher) to preserve quality

abc	720p	upn	1080i	Discovery HD	1080i	HDNet Movies	1080i	STARZ!	1080i
	1080i	WB	1080i	encore	1080i	themovie channel	1080i		1080i
FOX	720p	A&E	1080i	ESPN HD	720p	MSG	1080i		
NBC	1080i	Bravo	1080i	HBO HDTV	1080i	STV	1080i		
	1080i	Comcast SportsNet	1080i	HDNet	1080i	SHOWTIME HDTV	1080i		

- 3G-SDI and 10 GbE in the studio and headend in not too distant future
  - Beyond 3G-SDI, feasibility of 10 Gbps over coax already demonstrated



IPTV Distribution



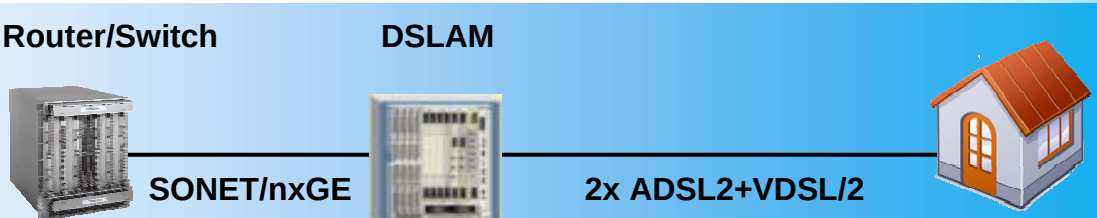
Multicast Requirements for Video Driving Ethernet Aggregation Market

Source: Metro Ethernet Forum

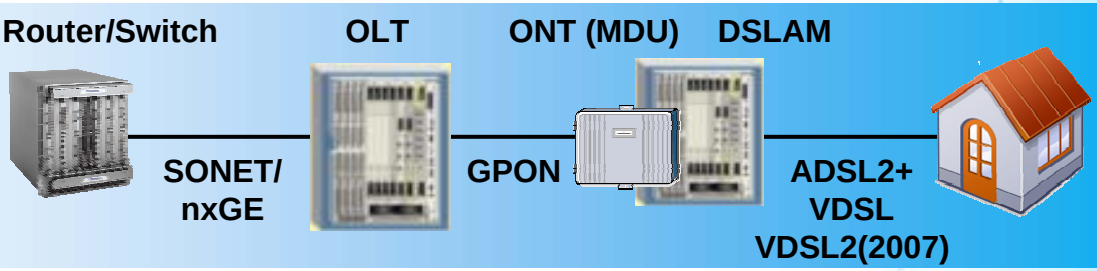
CY6

Delivering 20+ Mbits to Consumer

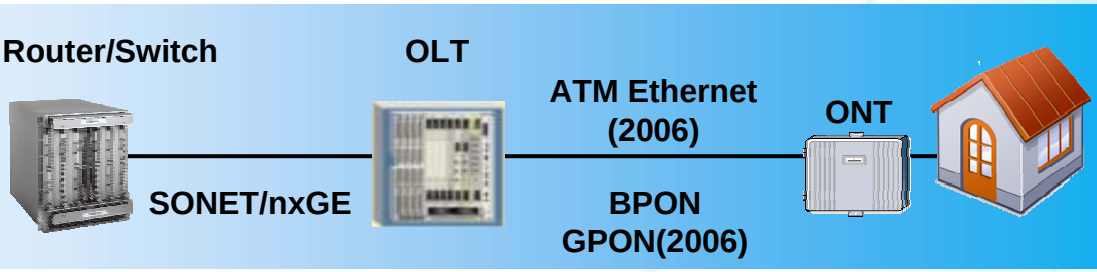
- VDSL/channel bonded ADSL



- Fiber to the node
  - Decreasing distance of copper loop



- Fiber to the home



Parallel Interfaces

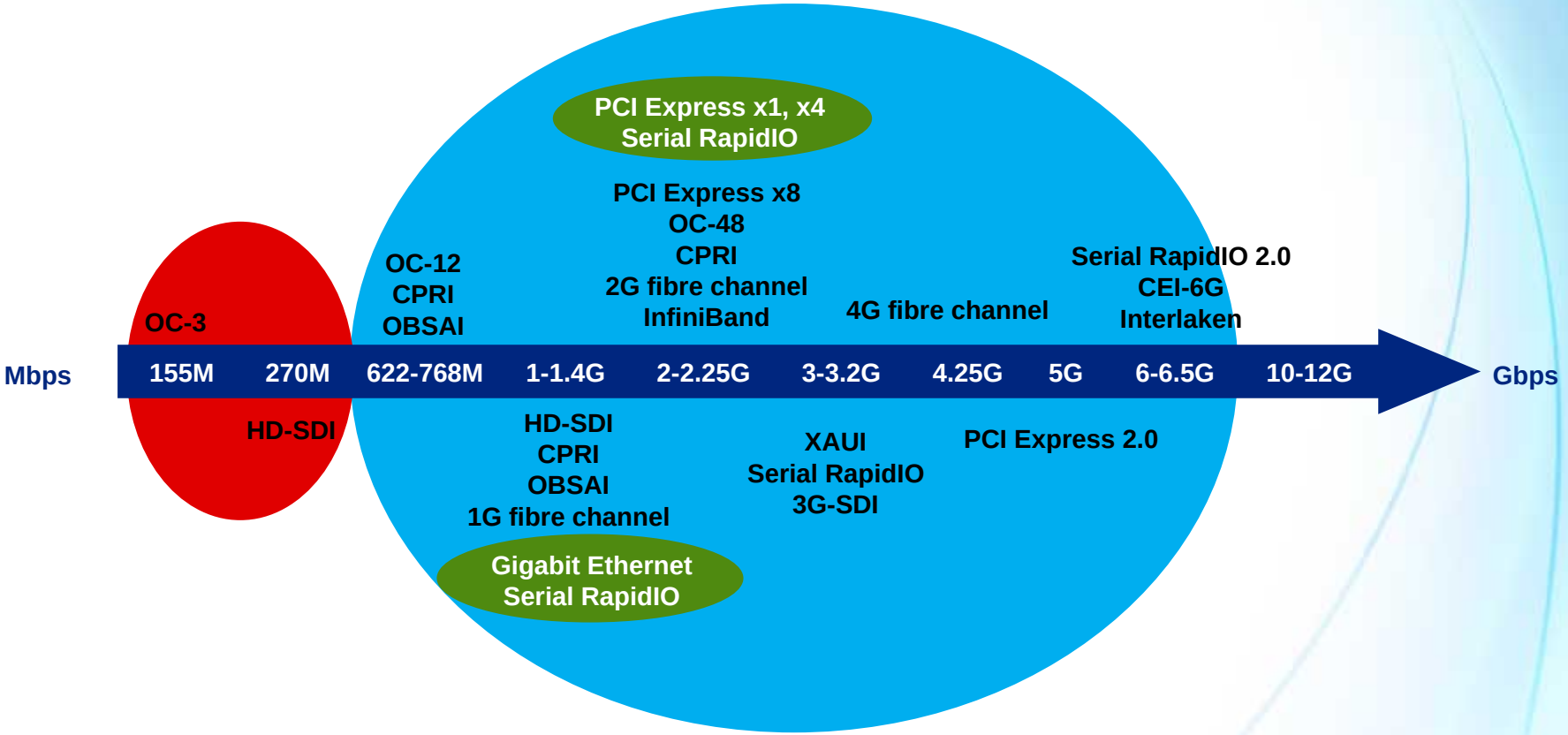
- Increasing bandwidth needs for several applications
- Parallel interfaces cannot scale up
  - I/O pin counts grow rapidly
  - Wider parallel buses have skew and synchronization issues
  - Driving parallel buses over longer distance demands more power

Serial Interfaces

- Transition from parallel to serial I/O solutions will:
  - Reduce system costs
  - Simplify system design
  - Provide scalability to meet new bandwidth requirements, and
  - Drive broadbase adoption of serial standards, e.g. PCI Express, Serial RapidIO, Gigabit Ethernet

CY3

Protocol Data Rates: 0.6 to 6.375 Gbps



- Addressable by Altera® Stratix® II GX FPGAs
- Achievable by Stratix II GX FPGAs with oversampling
- Mainstream protocols supported by Altera Arria™ GX FPGAs

Serial Interfaces - Future

- High-speed serial I/O solutions will ultimately be deployed in nearly every type of electronic products imaginable!
- Customers in all business segments and all categories start making the transition now
- Transceiver technology gaining in importance

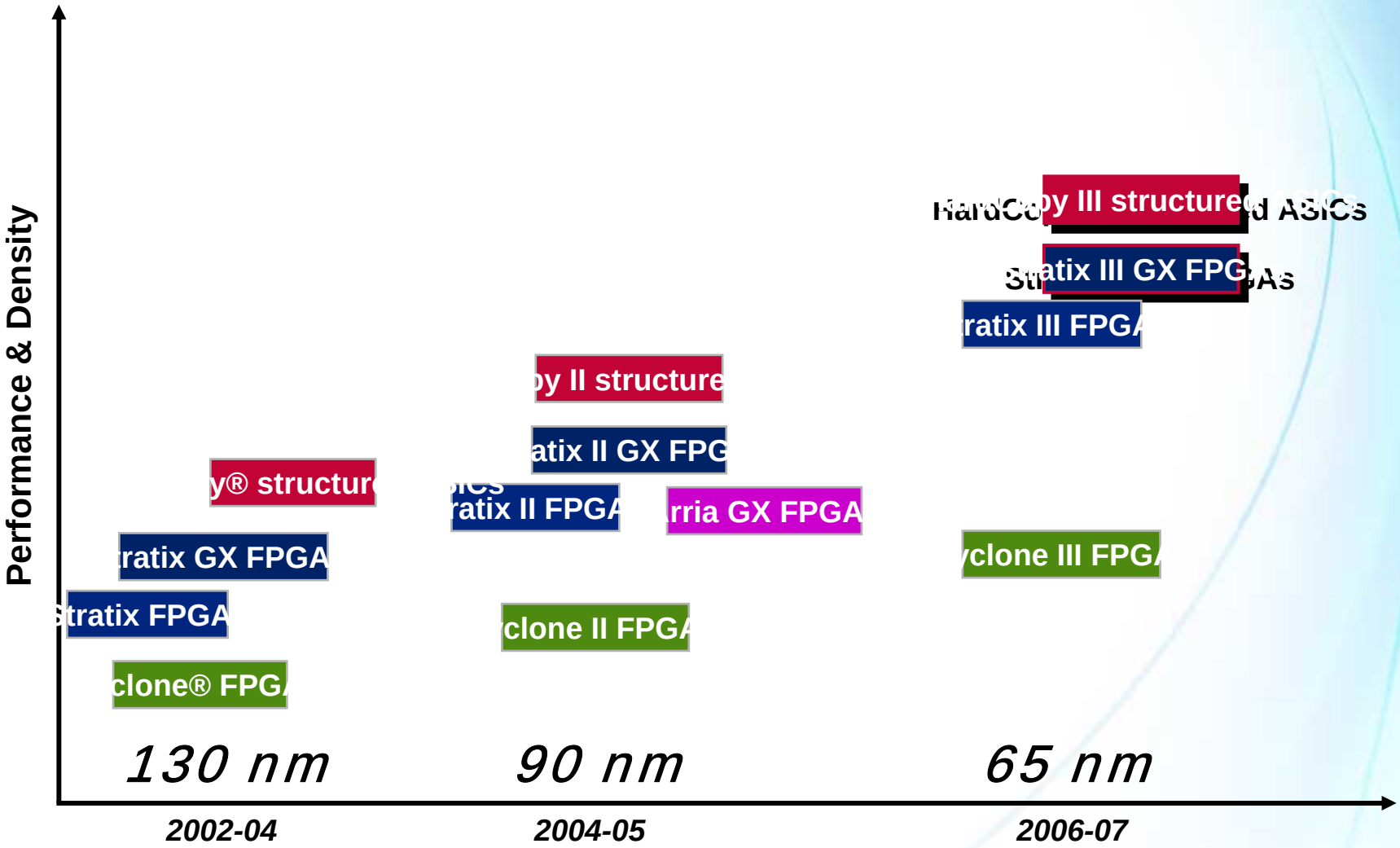
Transceiver-Based FPGAs

Transceiver-Based FPGAs

- FPGA vendors have introduced transceiver-based FPGAs
  - Altera has 4 generations of transceiver products
- Benefits
  - Integration of transceivers with FPGAs
  - Lower system cost
  - Ease of design and customization
  - Proprietary high-speed protocols
  - Respond to market dynamics

CY4

FPGAs with Transceivers



Stratix II GX FPGAs

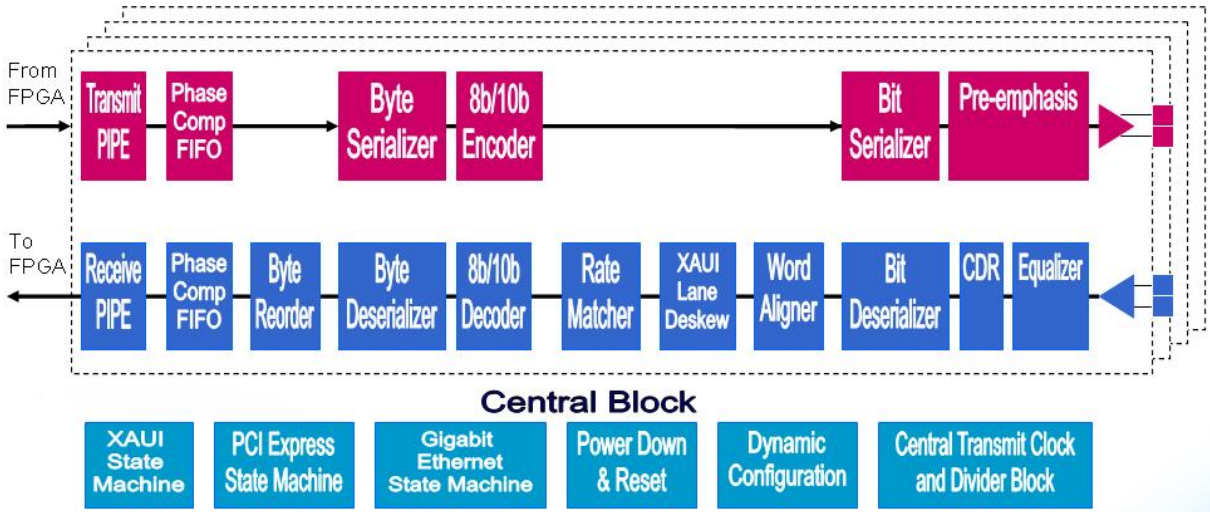
- Up to 20 transceivers operating between 600 Mbps & and 375 Gbps
- Lowest-power FPGA with embedded transceivers
- Best-in-class signal integrity solution includes pre-emphasis and equalization
- Complete protocol solution including software support, intellectual property, system models and reference designs

Third Family on 90 nm

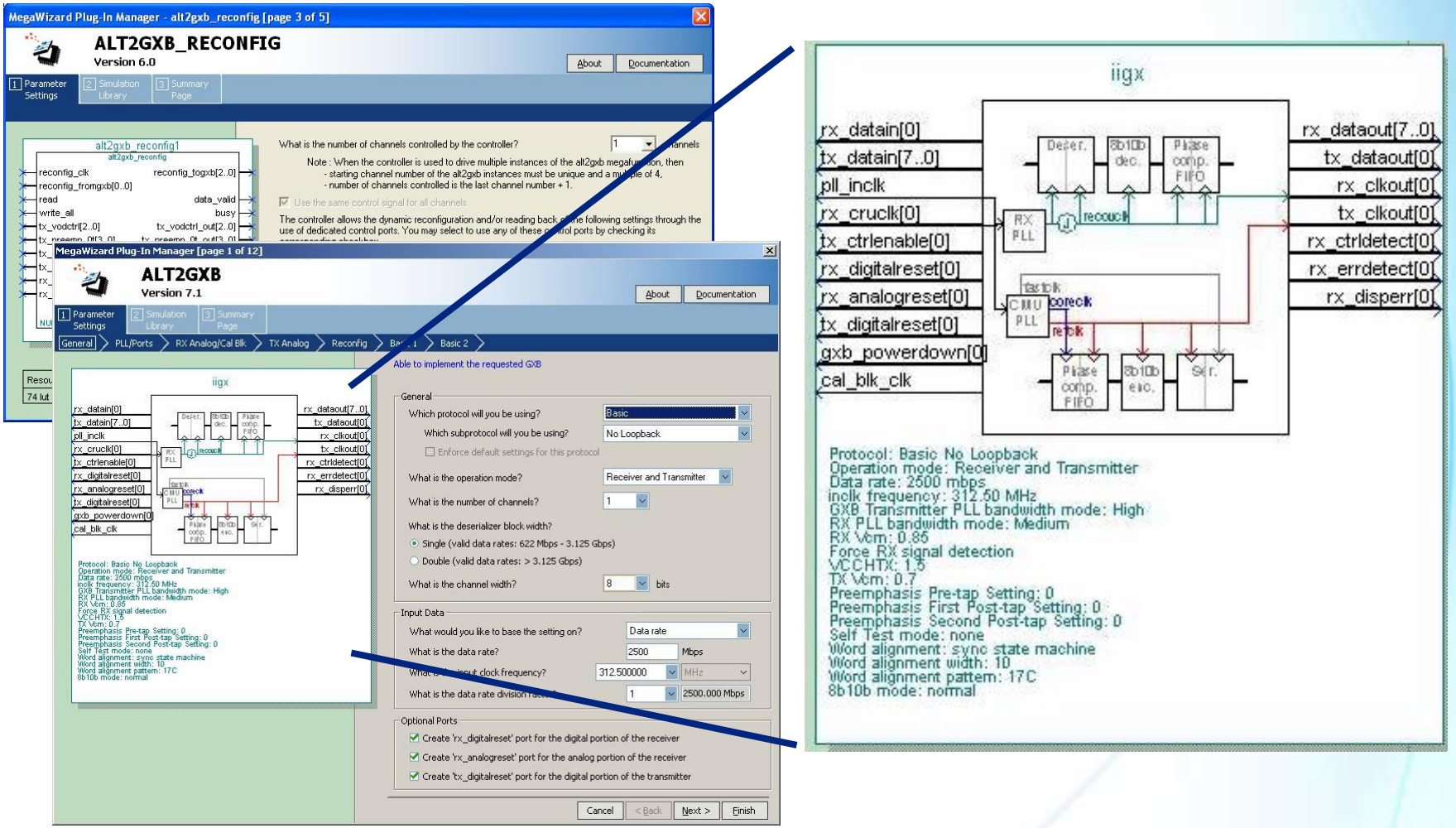
Transceivers With Optimal Signal Integrity

Complete Transceiver Building Blocks

- 600 Mbps – 6.375 Gbps
- Pre-emphasis and equalization
- Generic (basic) transceiver functionality
  - 8b/10b encoder/decoder
  - Rate matcher
  - Phase compensation FIFO
  - 8,10,16, 20, 32, 40 bit interface to core
- PCIe state machine
  - Power state sequencing
  - Electrical Idle, receive detect, and others
  - PIPE interface to core
- PCIe state machine
  - Power state sequencing
  - Electrical Idle, receive detect, and others
  - PIPE interface to core
- Gigabit Ethernet state machine
  - Comma character insertion/deletion
  - GMII-like interface to core
- XAUI state machine
  - Channel deskew, alignment, and bonding
  - XGMII-like interface to core



Transceiver MegaWizard



Simplifies Transceiver Design

Adaptive Dispersion Compensation Engine (ADCE)

- Automatically monitors and adjusts the receive equalizer for the best eye opening
- Typical systems don't require pre-emphasis for low bit error ratio (BER)
- Combined with pre-emphasis, the ADCE's adaptive equalization results in very low BER
- On-chip hot-socketing transceiver support

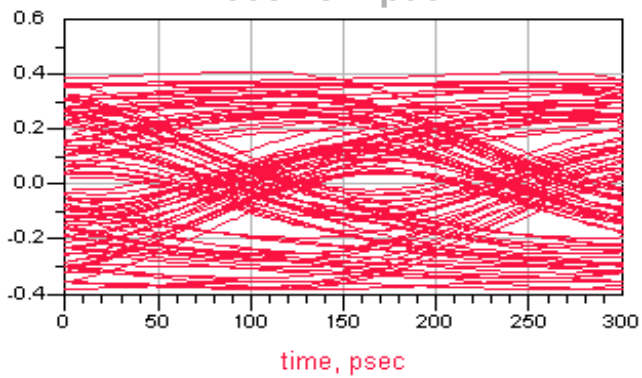
Plug and Play Signal Integrity with Adaptive Equalization and Hot Socketing

Best-in-Class Signal Integrity

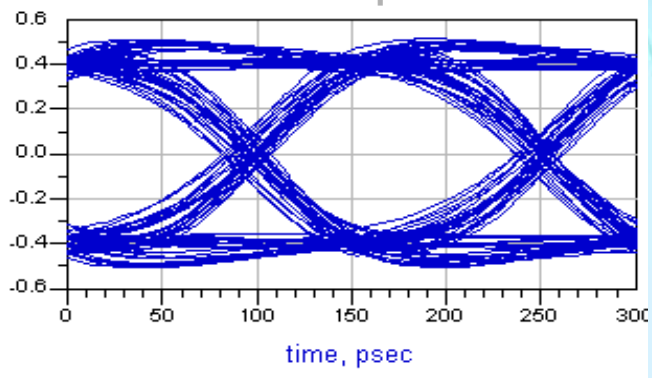
6.375 Gbps Across 40” of FR4

Receive Equalizer

Receive Input

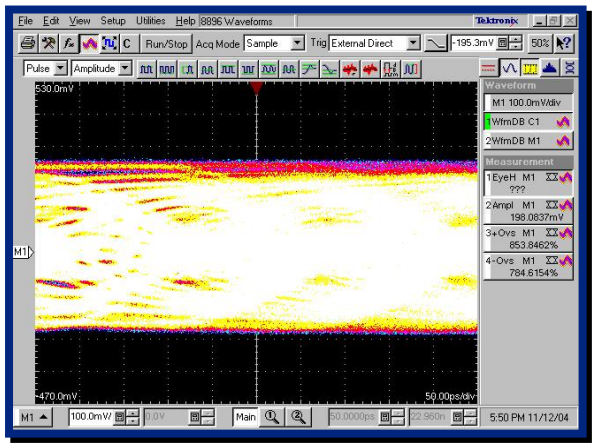


After 17dB Equalization

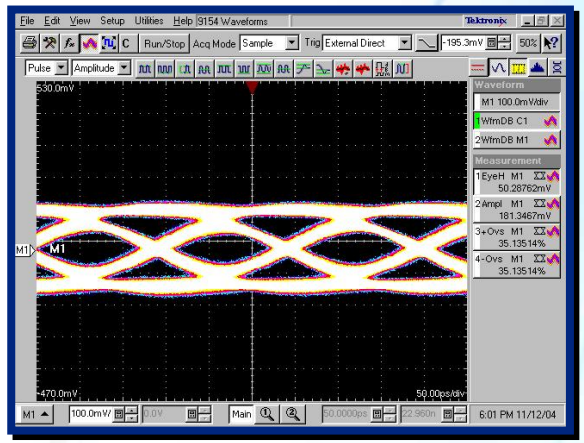


Transmit Pre-Emphasis

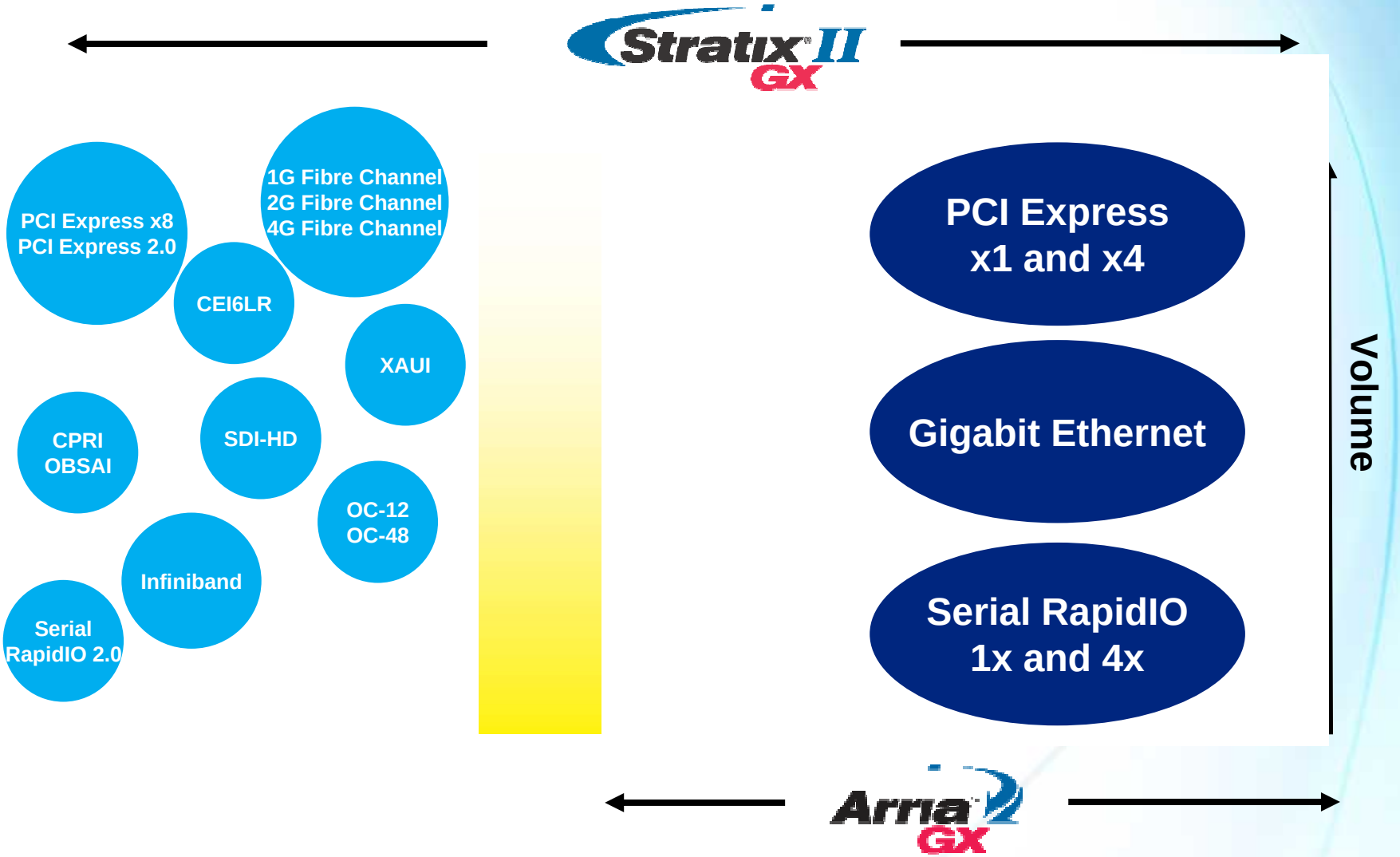
Receive Input



After 9.5dB Pre-emphasis



Market Transition



Introducing the Arria GX FPGA Family

- Risk-free, low-cost, transceiver-based FPGA family
- Support for mainstream protocols at 1.25 and 2.5 Gbps
  - PCI Express (x1 and x4)
  - Gigabit Ethernet
  - Serial RapidIO (1x and 4x)
- 5 family members ranging from 21,580 to 90,220 logic elements (LEs) with up to 4.5 Mbits of memory and 12 transceivers
- 50K LEs for $50 at launch (25Ku)

Stratix III FPGAs

- **Lowest power**
  - Lowest-power high-end FPGAs with Programmable Power Technology and selectable core voltage
  - Quartus® II PowerPlay analysis and optimization technology
- **Highest performance core**
  - Fastest FPGA: Minimum of one speed grade faster than all competitive FPGAs
  - Quartus II TimeQuest timing analyzer
- **Highest performance I/Os**
  - Best I/O performance and signal integrity
  - Tools for signal integrity analysis
- **Highest density**
  - Biggest FPGAs with most logic, memory, and DSP resources
  - Logic: 338K LEs and 270K registers
  - Memory: 17.2 Mbits of 600-MHz memory
  - DSP: 896 18X18 multipliers

Lowest-Power
High-Performance FPGA in the Industry

65-nm High-End Product Offerings

- General applications
  - Balanced logic, memory, and multipliers

- **Memory- and DSP-rich applications**
  - More memory and multipliers per logic
  - Ideal for wireless, medical imaging, and military applications

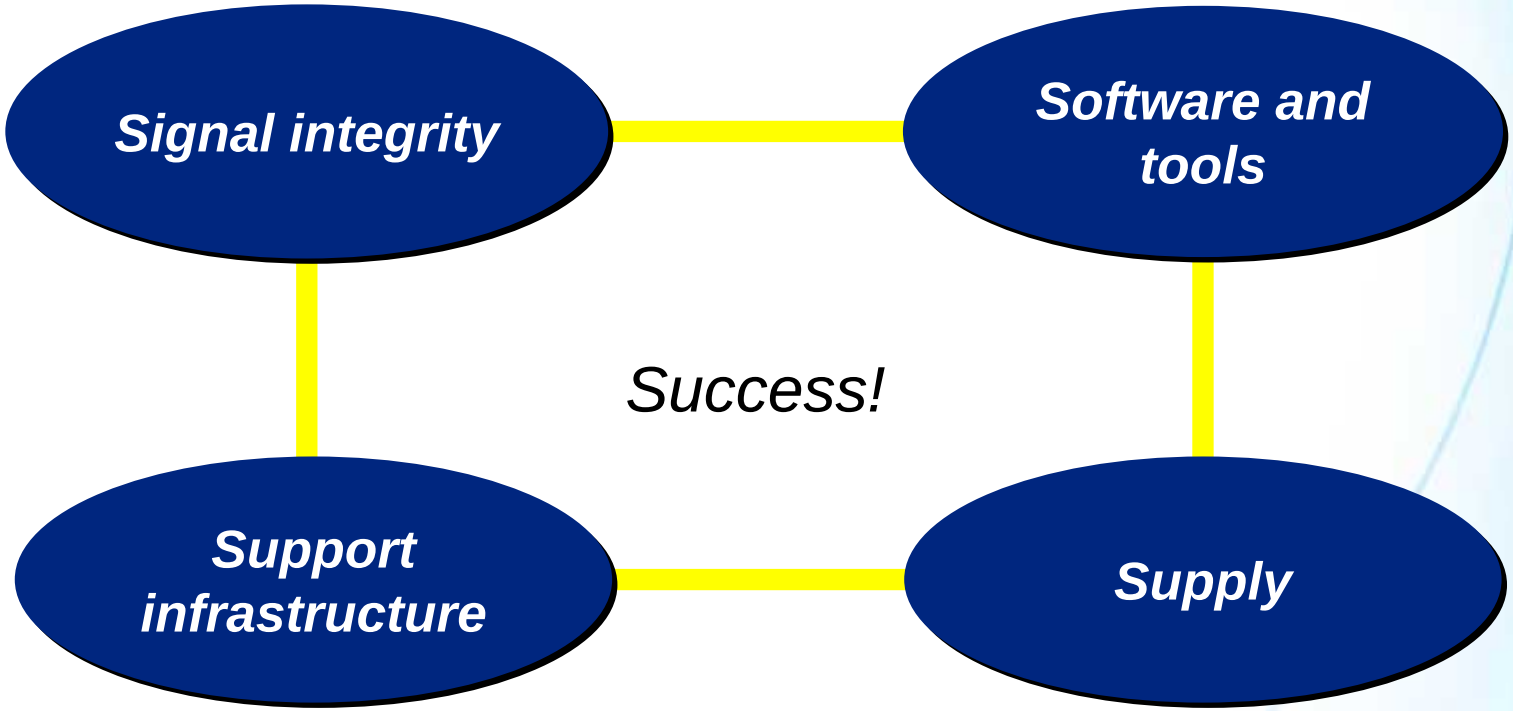
- High-bandwidth applications
  - Integrated multigigabit transceivers
  - Ideal for telecom, broadcast, test equipment, computer, and storage applications

- High-volume applications
  - Lower cost, lower power, and higher performance
  - Seamless migration from Stratix III FPGAs

Application-Optimized Solutions With Cost-Reduction Path

Success Factors

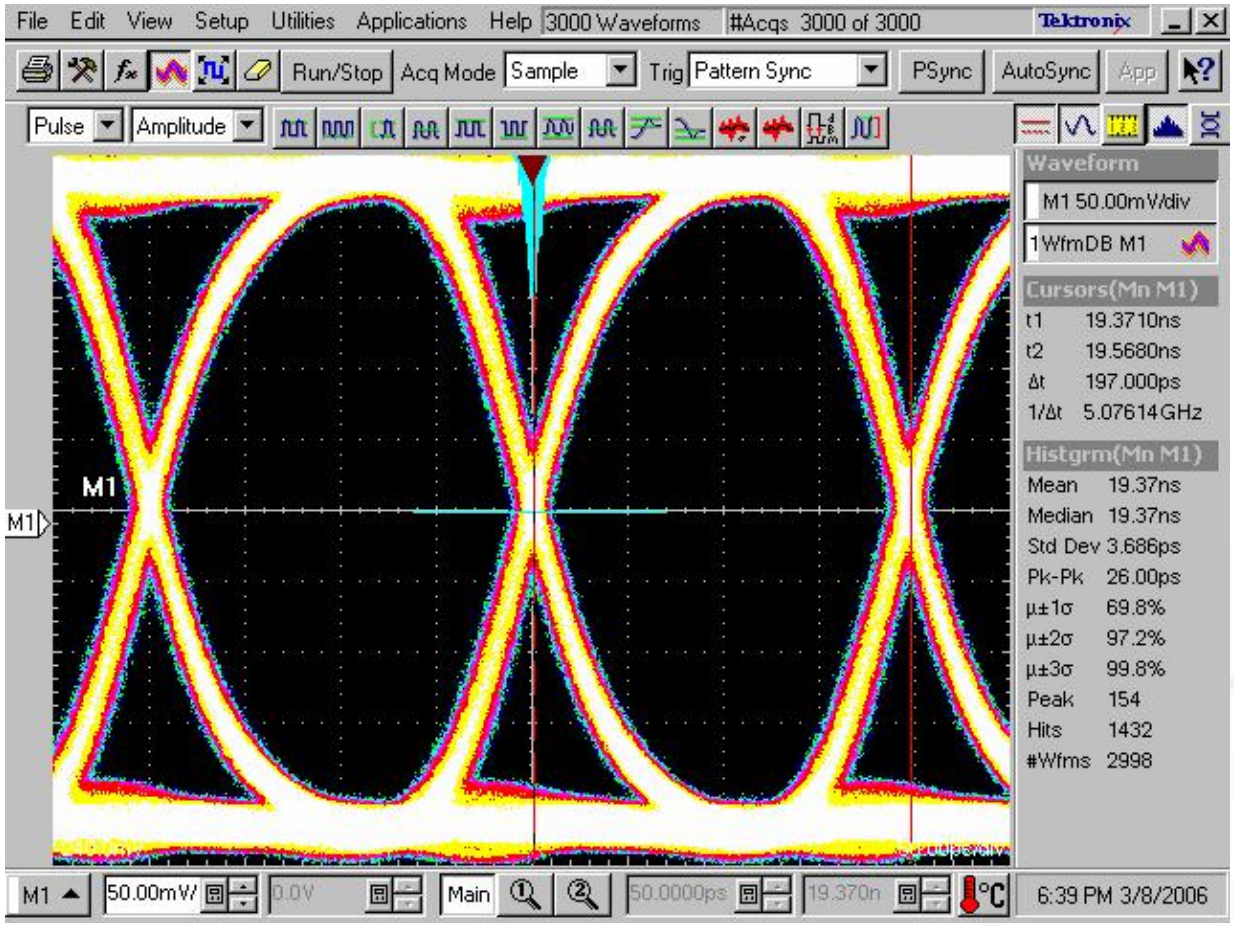
Success Factors for Transceiver-Based Designs



Designing with Transceivers is Not About Silicon Alone

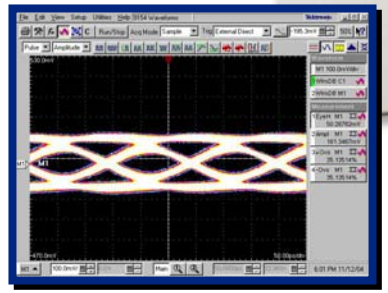
Optimal Signal Integrity

- Stratix II GX FPGAs offer best-in-class signal integrity at 6.375 Gbps



Complete Protocol Solutions

- Hard protocol intellectual property (IP), IP MegaCore® functions, reference designs
- Signal integrity modeling
- Protocol-specific development boards
  - PCI Express and SDI
- Evaluation board
- Quartus II software support
- Compliance testing
- System validation reports
- Characterization reports



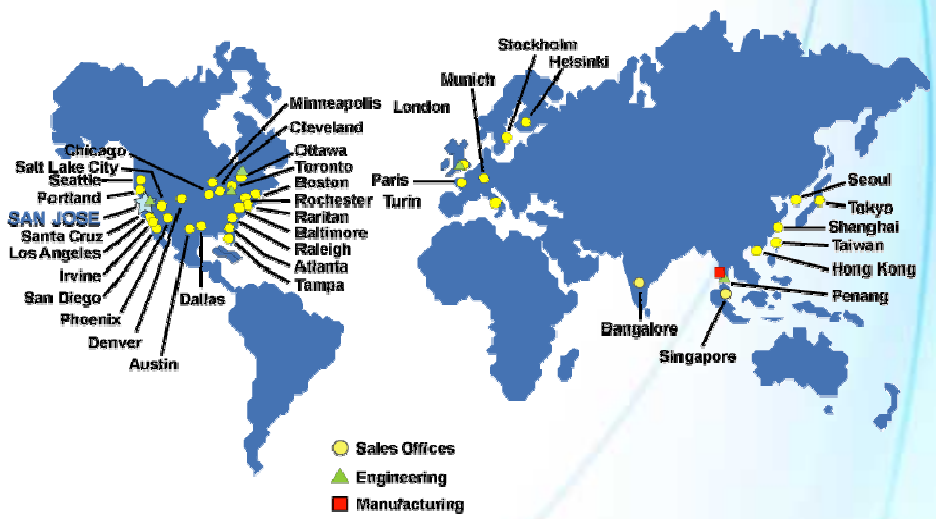
QUARTUS II

MegaCore®

Dramatically Increase Ease of Design

System-level Support Infrastructure

- Large network of high-speed experts to support system-level integration
  - Regional Support Centers (RSCs) in North America, Europe, Asia, and Japan
  - Field-based high-speed specialist Field Applications Engineers (FAEs)
  - Knowledgeable regional FAEs proficient in transceiver technology
  - Online support (MySupport)
  - Extensive collection of collateral, design examples, and characterization reports



Altera-TSMC Symbiotic Partnership

Benefit to ALTERA

What Altera gets:
Access to most advanced process without huge R&D investments
Pure play foundry—no capacity conflict
Mutual benefit of an exclusive relationship
Ability to get process tuned to its needs

Benefit to tsmc

FPGA structure	What TSMC gets:
Memory structure	Defect identification
Large dies	Defect density (DD) reduction
Dense interconnect	Back-end improvements
High performance	Front-end improvements

ALTERA

Conclusion

Summary

- Serial protocols becoming mainstream due to end-market evolution
- Stratix II GX and Arria GX FPGAs offer best-in-class transceivers with optimal signal integrity
- Unique software tools, IP, and support infrastructure enable customers to design with confidence with Altera

Design with Confidence with Altera