White Paper

Video Surveillance Implementation Using FPGAs

Introduction

Currently, the video surveillance industry uses analog CCTV cameras and interfaces as the basis of surveillance systems. These system components are not easily expandable, and have low video resolution with little or no signal processing. However, the next generation of video surveillance systems will replace these components with newer digital LAN cameras, complex image processing, and video-over-IP routing. They will no longer be simply surveillance camera systems, but also video communication systems.

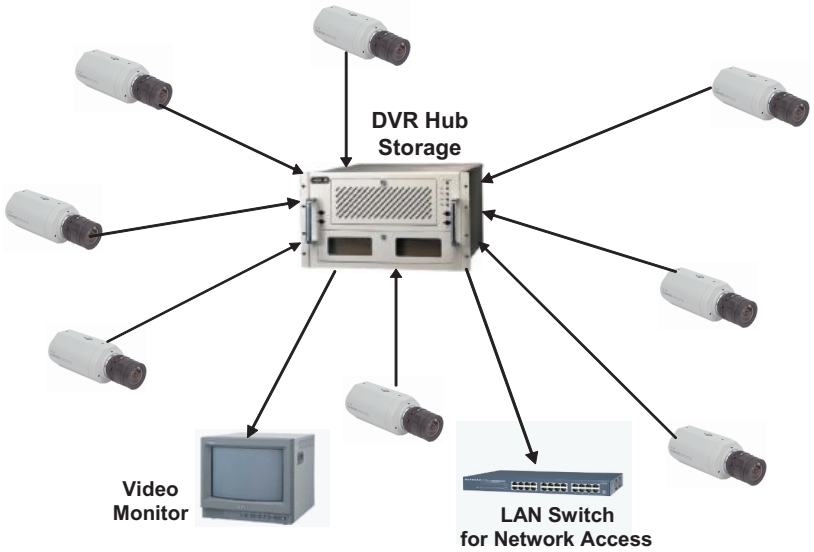
The Internet protocol (IP)-based structure of the new surveillance systems allows for scalability, flexibility, and cyber security. Various encoding and decoding standards transport the video stream (MPEG4 CODEC is the standard used today). Besides the CODEC function, image pre- and postprocessing enhances the picture quality in real time with low latency. Programmable logic with embedded DSP blocks, memories, interfaces, and off-the-shelf IP solutions allows a designer to meet the new system requirements.

Digital Video Recorder Architecture

In a digital video recorder (DVR) system, multiple analog CCTV cameras route to a central video switching hub for storage, scaling, image processing, and display. Video resolution and quality are typically low to reduce complex compression and cost. Special processing, such as motion detection, reduces the amount of storage space in the central hub. This architecture is therefore not flexible or readily expandable, so video monitoring is limited in terms of quality and quantity.

A typical DVR system (shown in Figure 1) combines with either an internal or external video matrix switcher to route the video from cameras to monitors. This type of system requires multiple inputs and output multiplexing, making it very suitable for using programmable logic for system flexibility and expandability.

Figure 1. DVR System



Video Compression and Image Processing

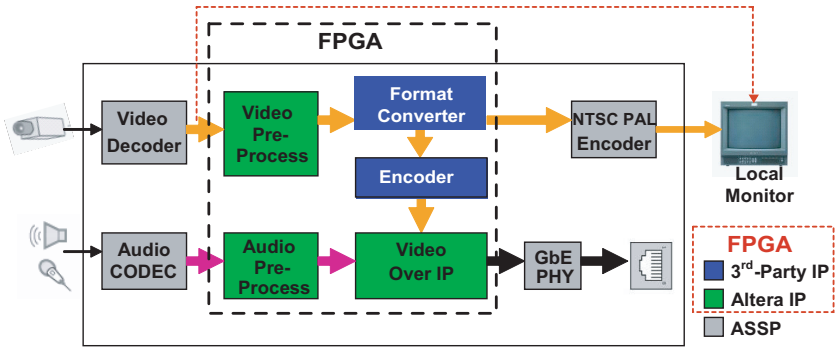
There are many different standards for video data compression, with the most popular including JPEG, H.263, Motion JPEG, MPEG, and Wavelet. The type of compression used has an impact on hardware system requirements, including memory, data rate, and storage space. However, next-generation surveillance systems will probably use the H.264

standard due to its compression efficiency. Efficiency is a key factor in the transmission of high-quality video over a bandwidth-limited network. For example, a color transmission at 30 fps at 640 x 480 pixels requires a data rate of 26 Mbytes/sec. This data rate must be reduced (compressed) to a more manageable data rate that can be routed over a twisted pair of copper wires.

The two types of video compression data rate are constant bit rate (CBR) and variable bit rate (VBR). CBR limits the data rate for a real-time communication channel with limited bandwidth. However, when CBR compresses high-motion details, image quality is lost and results in image blocks on the display. VBR allows the data rate to adapt to the motion or absence of motion, which is extremely useful for video surveillance system storage. H.264 compression with VBR provides the best efficiency for security video storage.

Pre- and postprocessing techniques, such as de-interlacing, scaling, noise reduction using 2D filtering, and color space conversion, are also critical parts of a video surveillance system. These functions are included in Altera's Video and Image Processing Suite. Figure 2 illustrates a typical video surveillance system setup using FPGAs and ASSPs.

Figure 2. Surveillance Camera System With FPGA



With expanding resolutions and evolving compression, there is a need for high performance while keeping architectures flexible to allow for quick upgradeability. As technology matures and volumes increase, the focus will move to cost reduction. System architecture choices include standard cell ASICs, ASSPs, and programmable solutions such as digital signal processing (DSP) or media processors and FPGAs. Each of the approaches has advantages and disadvantages, with the ultimate choice depending on end-equipment requirements and solution availability. Given the trend discussed above, the ideal surveillance architecture would have the following characteristics: high performance, flexibility, easy upgradability, low development cost, and a migration path to lower cost as the application matures and volume ramps.

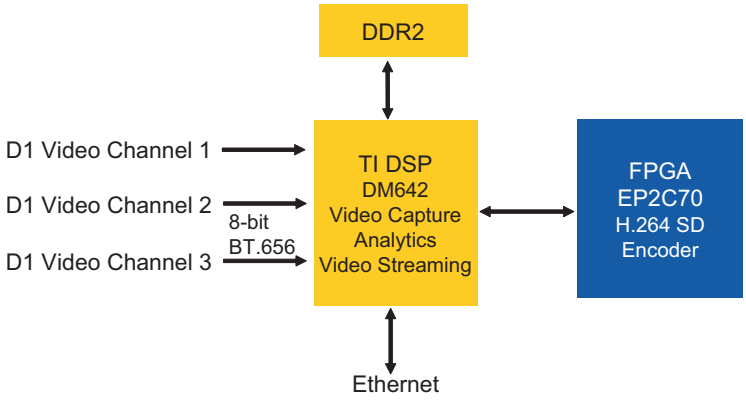
High Performance

Performance not only applies to compression, but also pre- and postprocessing functions. In fact, in many cases these functions consume more performance than the compression algorithm itself. Examples of these functions include scaling, deinterlacing, filtering, and color space conversion.

For video surveillance, the need for high performance rules out processor-only architectures. They simply cannot meet the performance requirements with a single device. A state-of-the-art DSP running at 1 GHz cannot perform H.264 HD decoding or H.264 HD encoding, which is about ten times more complex than decoding. FPGAs are the only programmable solutions able to tackle this problem. In some cases, the best solution is a combination of an FPGA plus an external DSP processor.

This FPGA coprocessing approach can deliver significantly higher performance, since the designer can partition the system to take advantage of the benefits of each device. Figure 3 shows the block diagram.

Figure 3. Architecture With FPGA and TI DSP



Flexibility Provides Fast Time to Market and Easy Upgradeability

When technology rapidly evolves, architectures must be flexible and easy to upgrade. This rules out standard cell ASICs and ASSPs for those applications. Typically designed for very high-volume consumer markets, ASSPs often are quickly obsolete, making them an extremely risky choice for most applications.

Low Development Cost

When adding up costs for masks and wafer, software, design verification, and layout, development of a typical 90-nm standard-cell ASIC can cost as much as US$30 million. Only the highest volume consumer markets can justify such pricey development costs.

Migration Path to Lower AUP

As standards stabilize and volumes increase, it is important to have a solution with a low-cost migration path. Often this means either market-focused ASSPs or standard-cell custom ASIC devices. However, the rising cost of custom silicon makes those solutions economically feasible in only the highest volume consumer applications. Most video- and imaging-focused silicon companies target high-volume applications such as video camcorders, set-top boxes, digital still cameras, cell phones, and other portable products, and LCD televisions and monitors. Therefore, when designing a lower-volume type of application, it is best to consider an FPGA, as it is unlikely an ASSP with the exact feature set required exists and even the best off-the-shelf solution is a high-risk choice due to the potential for obsolescence.

Altera's Video and Image Processing Solution

For the reasons described above, FPGAs are particularly well suited to meet the requirements of many video and image processing applications. Altera® FPGAs have the following characteristics that make them very appealing for video and image processing architectures:

- *High performance:* HD processing can be implemented in a single Altera FPGA.
- *Flexibility:* Altera FPGAs provide the ability to upgrade architectures quickly to meet evolving requirements, while scalability allows use of FPGAs in low-cost and high-performance systems.
- *Low development cost:* Video development kits from Altera start as low as US$1,095 and include the software tools required to develop a video system using Altera FPGAs.
- *Obsolescence proof:* Altera FPGAs have a very large customer base who ship products for many years after introduction. In addition, FPGA designs are easily migrated from one process node to the next.
- *Plan for lower production costs:* Altera offers several ways to help plan for the time when products move from lower unit volumes to much higher volumes:
  - For designs initially using Stratix® series FPGAs, Altera offers a structured ASIC migration path to low costs: Altera's HardCopy® structured ASICs cost as low as US$10 at 100ku for 1 million ASIC gates.

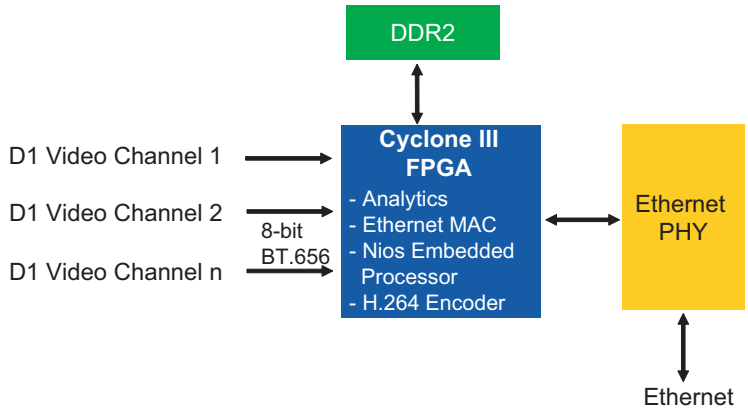
- Also for designs initially using Stratix series FPGAs, future versions of the Cyclone® series, such as today's Cyclone III FPGA family, may deliver sufficient performance and features at a significantly lower cost.

- *Video and Image Processing Solution:* This includes Altera's Video and Image Processing Suite, optimized DSP Design Flows, interface and third-party video compression IP, and video reference designs.

ASSP-Like Functionality on FPGAs and Structured ASICs

With a growing number of solutions, Altera and its partners provide ASSP functionality in the form of an FPGA or structured ASIC. An example is an H.264 encoder (shown in Figure 4) developed as a product in which customers use FPGAs just as they do ASSPs. The benefit over the traditional ASSP approach is that the FPGA solution evolves quickly, with no risk of obsolescence.

Figure 4. Cyclone III FPGA Standalone H.264 Engine



This solution provides significant flexibility, since it is scalable from low-cost systems to very high-function systems, supporting over 16 channels in a single device with the lowest cost per channel available today. To see how design teams can trade off cost for H.264 performance, measured in frames per second processing, see Table 1.

Table 1. Scaling Cyclone III FPGA for H.264 Performance

D1 (Frames per Second)	FPGA	HardCopy II Structured ASICs
40	EP3C25	HC210
80	EP3C40	HC210
120	EP3C55	HC210
160	EP3C80	HC210
240	EP3C120	HC220
480	2 EP3C120	2 HC220
720	3 EP3C120	3 HC220
960	4 EP3C120	4 HC220

The additional advantage designers appreciate about this solution is that the flexibility provides a way to future-proof designs, minimizing the chance of product obsolescence.

DSP Design Flow

For custom development, Altera provides an optimized DSP design flow that allows several different ways to represent the design. These include VHDL/Verilog, model-based design, and C-based design. Altera's Video and Image Processing Suite of cores can be used in conjunction with any of these design flow options.

Altera and The MathWorks have joined forces to create a comprehensive DSP development flow that allows designers to enjoy the price/performance benefits of Altera FPGAs while leveraging Simulink, The MathWorks's model-based design tool. Altera's DSP Builder is a DSP development tool that connects Simulink with Altera's industry-leading Quartus® II development software. DSP Builder provides a seamless design flow in which designers perform algorithmic development in the MATLAB software and system-level design in the Simulink software, then port the design to hardware description language (HDL) files for use in the Quartus II software. The DSP Builder tool is tightly integrated with the SOPC Builder tool, allowing the user to build systems that incorporate Simulink designs and Altera embedded processor and intellectual property cores. This development flow is easy and intuitive for designers who do not have extensive experience using programmable logic design software.

Video and Image Processing Suite

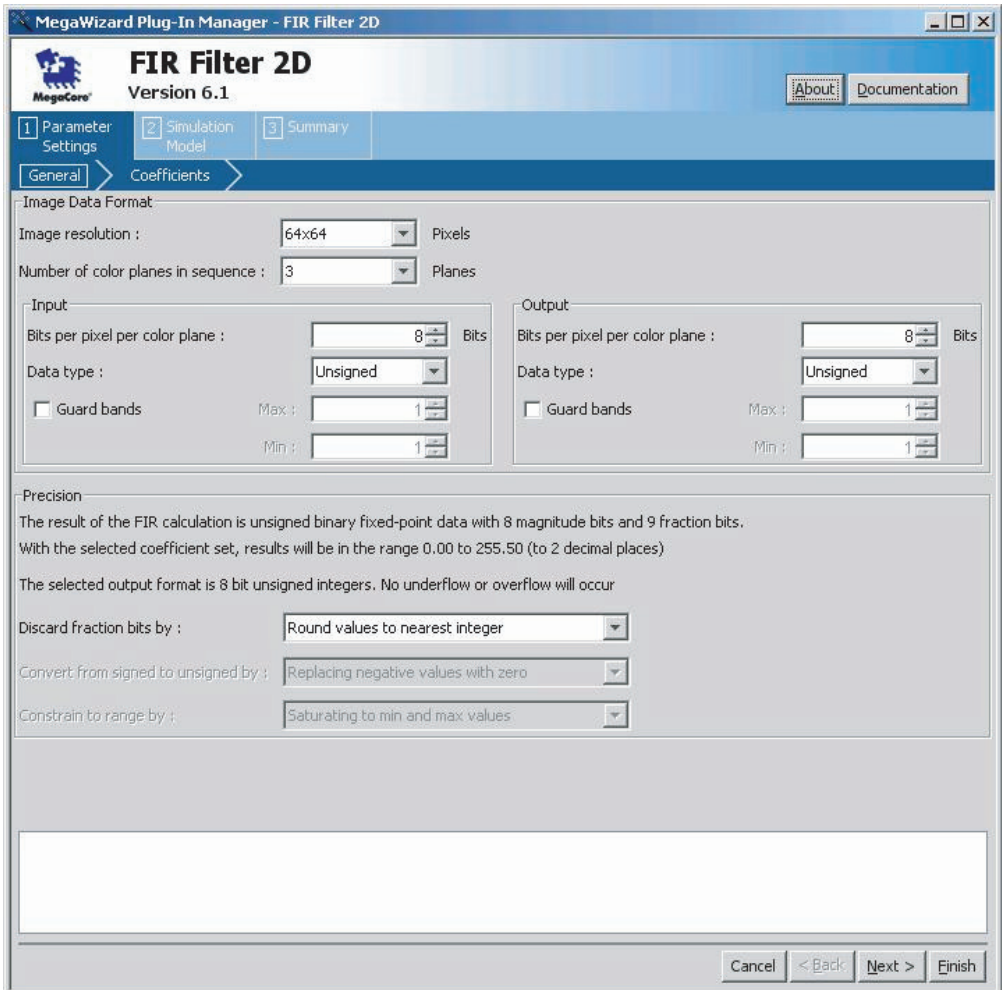
The Video and Image Processing Suite consists of nine functions with parameters that can be statically, or in some cases, dynamically changed. These functions can be used to create the video preprocess section of the video surveillance system setup shown in Figure 2. Table 2 summarizes these functions.

Table 2. Functions Available With the Video and Image Processing Suite

Function	Description
Deinterlacer	Converts interlaced video formats to progressive video format
Color Space Converter	Converts image data between a variety of different color spaces
Scaler	Resizes and clips image frames
Alpha Blending Mixer	Mixes and blends multiple image streams
Gamma Corrector	Performs gamma correction on a color plane/space
Chroma Resampler	Changes the sampling rate of the chroma data for image frames
2D Filter	Implements 3x3, 5x5, or 7x7 finite impulse response (FIR) filter operation on an image-data stream to smooth or sharpen images
2D Median Filter	Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Line Buffer Compiler	Efficiently maps image line buffers to Altera on-chip memories

The 2D Filter GUI is shown in Figure 5 as an example of the type of user configuration available with the cores provided in the Video and Image Processing Suite. Resolutions, bits per sample, and FIR filter size are some of the parameters supported in the 2D filter core.

Figure 5. 2D Filter GUI



Video Compression

Several third parties have video compression solutions targeting Altera FPGAs and structured ASICs. Table 2 lists some of the common video compression standards and the associated third parties.

Table 3. Third-Party Video Compression Solutions

Function	Company
H.264 Main and High Profile	ATEME
H.264 Baseline Profile	CAST, W&W, 4i2i
JPEG/JPEG2000	Barco, Broadmotion, CAST
MPEG4 SP/ASP	Barco, CAST, 4i2i

Video Over IP

Altera offers a reference design for video over IP. The design transmits video transport stream (TS) data over IP-based networks, bridging one or more compressed video streams and IP packets over 100-Mbps or 1-Gbps Ethernet. The reference design accepts TS data and encapsulates it for transmission over Ethernet, as well as receiving frames from Ethernet and generating TS data.

Encapsulation of the TS data for Ethernet uses IP and the user datagram protocol (UDP). Optionally, the real-time transport protocol (RTP) can also be used. Dedicated hardware performs the encapsulation, maximizing the throughput of the reference design and minimizing latency. Frames can be processed, transmitted, and received at the Ethernet line rate, which supports an aggregate TS bandwidth of over 900 Mbps for a gigabit Ethernet link. For multiple TS interfaces, the reference design individually maps each one to a specific UDP/IP socket (combination of IP address and UDP port). All other encapsulation parameters also can be individually configured per TS. The reference design supports IP multicast and includes a Nios® II processor. Software running on the Nios II processor configures the operation of the reference design and handles any Ethernet management traffic.

Systems Interfaces

Altera and its partners offer several interface cores that are relevant to video surveillance systems. These include DDR2 SDR DRAM Controllers, ATA Hard Disk Drive Controller, and PCI Express.

Benchmarks

An 4-channel D1 solution or 16-channel CIF solution with H.264 baseline profile encoding, deinterlacing, scaling, color space conversion, and noise reduction using 2D FIR filtering can be implemented in Altera's Cyclone III EP3C55 FPGA.

Conclusion

The ideal surveillance architecture will have the following characteristics: high performance, flexibility, easy upgradability, low development cost, and a migration path to lower cost as the application matures and volume ramps. Altera's FPGAs in conjunction with the feature-rich Altera Video and Image Processing Suite, Altera Video over IP reference design, and partner's compression solutions offer video system designers all the key building blocks needed to produce such a system.

Further Information

- Altera's Video and Image Processing Solutions website:
  www.altera.com\video_imaging
- Altera’s Video Processing Reference Design:
  www.altera.com/end-markets/refdesigns/sys-sol/broadcast/ref-post-processing.html

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