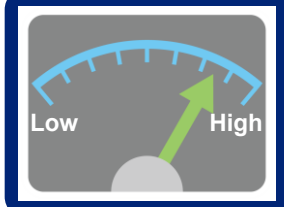
SoC FPGAs

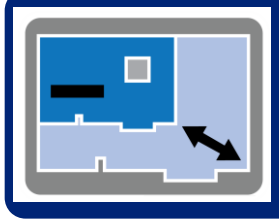
Your User-Customizable System on Chip

Embedded Developers Needs



Increase system performance

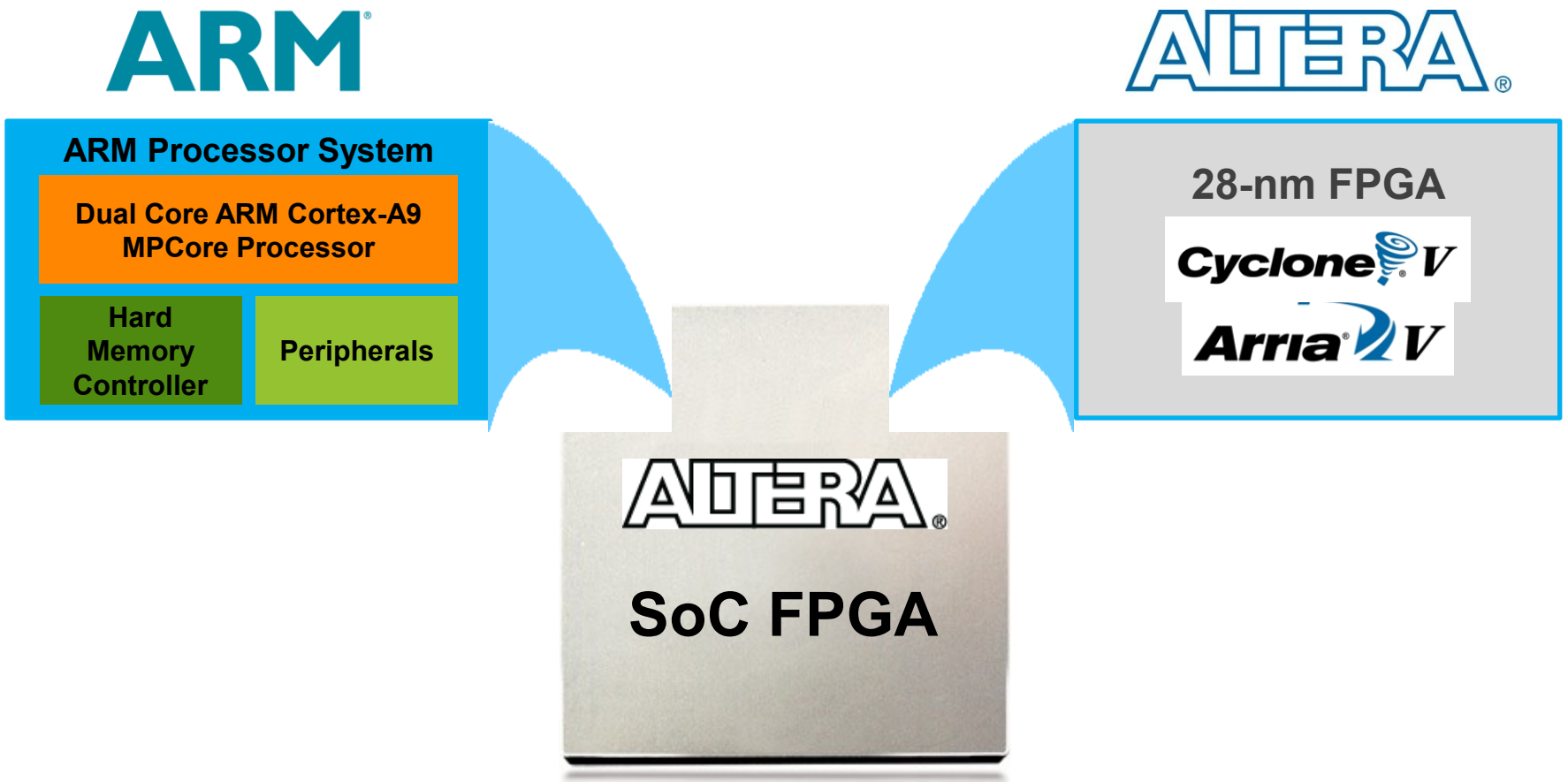
Reduce system power



Reduce board size

Reduce system cost

Providing the Best of Both Worlds

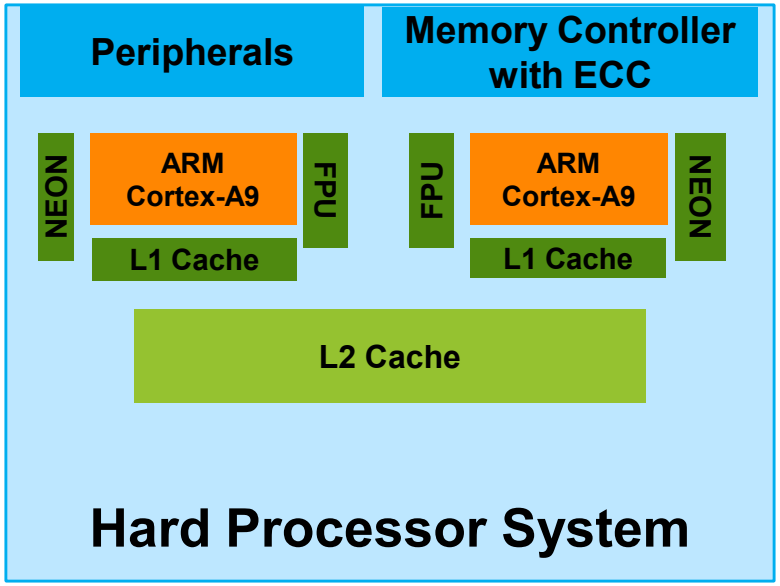


ARM + Altera = SoC FPGAs

SoC FPGA Family Highlights

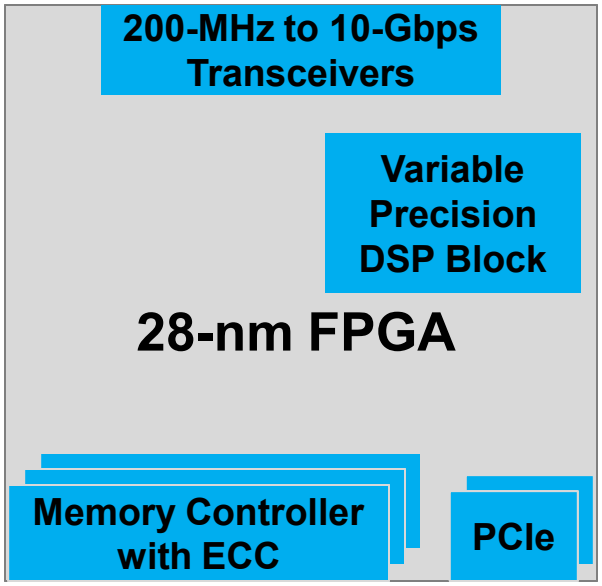
- Dual-core ARM Cortex-A9 MPCore processor
  - Hard memory controller, peripherals and high-bandwidth interconnect
- Altera's 28-nm FPGA fabric
  - Cyclone V FPGA and Arria V FPGA
- ARM's ecosystem and Altera's hardware development flow
  - Quartus II software and Qsys system integration tool
- Proven virtual prototyping methodology
  - SoC FPGA Virtual Target for device-specific software development

ARM Processor Combined with Hard IP



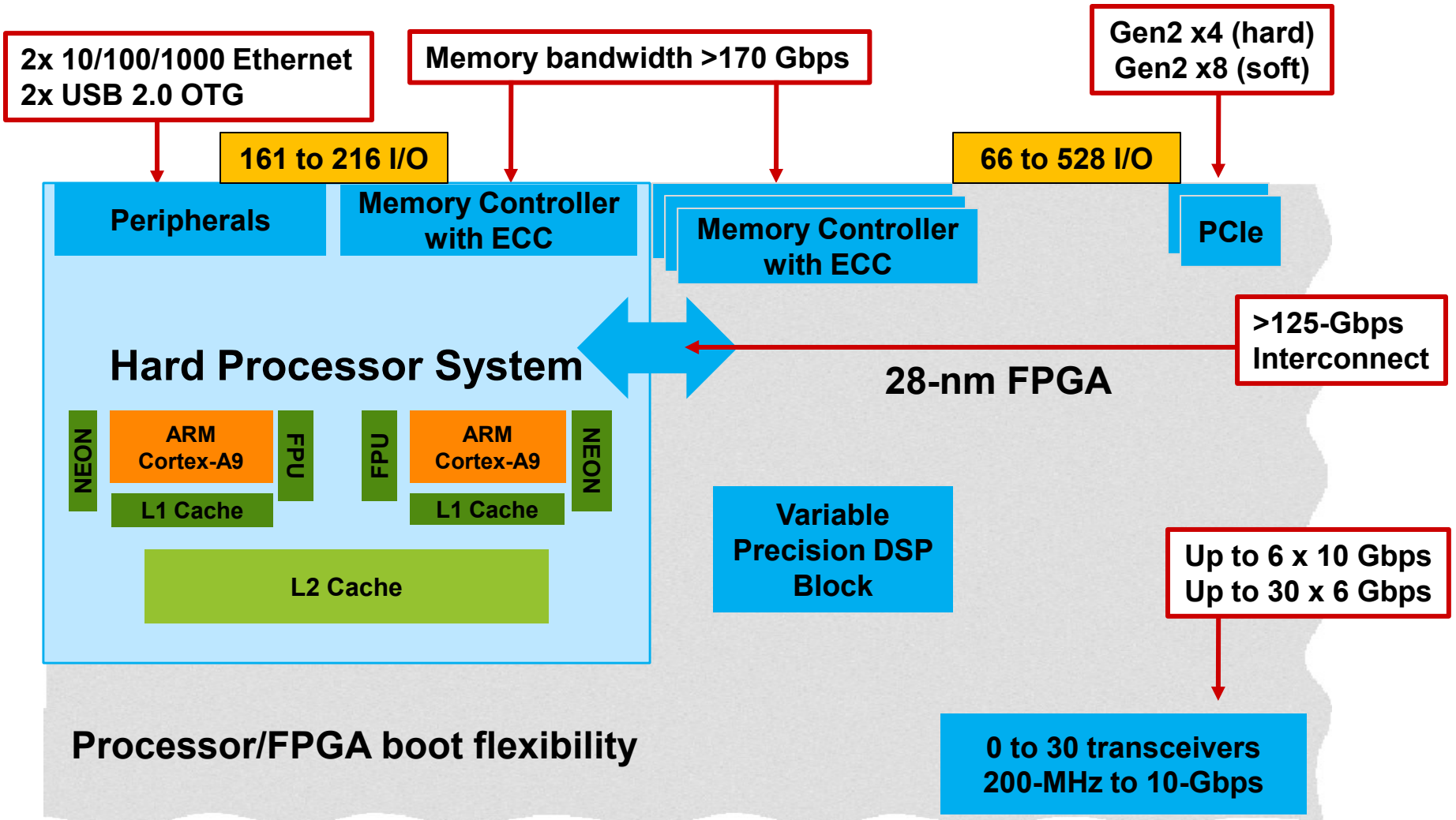
- Dual-core ARM Cortex-A9 MPCore processor
  - 800 MHz per core (industrial grade)
  - NEON media processing engine
  - Single/double precision floating point unit (FPU)
  - 32-KB/32-KB L1 caches per core
  - ECC-protected 512-KB shared L2 cache
- Hard IP
  - Multi-port memory controller with ECC
    - DDR2/3, Mobile DDR and LPDDR2
  - Flash memory controllers with ECC
    - QSPI (NOR), NAND and SD/SDIO/MMC
  - Wide range of common peripherals

Advanced 28-nm FPGA Technology

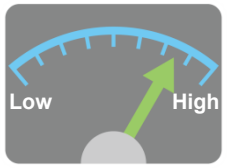


- 28-nm low-power (28LP) FPGA fabric
  - The optimal choice for addressing today's power- and cost-constrained applications
  - Lowest absolute power
- Hard IP
  - Up to three memory controllers with ECC
  - Variable precision DSP technology
  - Up to two hard PCIe Gen 2 x4
  - High-speed transceivers operating up to 10 Gbps

Superior System Bandwidth with Data Integrity



System-Level Benefits of SoC FPGA

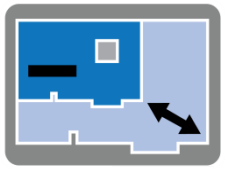


Increased system performance

- 4,000 DMIPS for under 1.8W
- Up to 1,600 GMACS, 300 GFLOPS DSP
- >125 Gbps processor to FPGA interconnect
- Cache coherent hardware accelerators

Reduced power consumption

- Up to 30% power savings vs. 2-chip solution

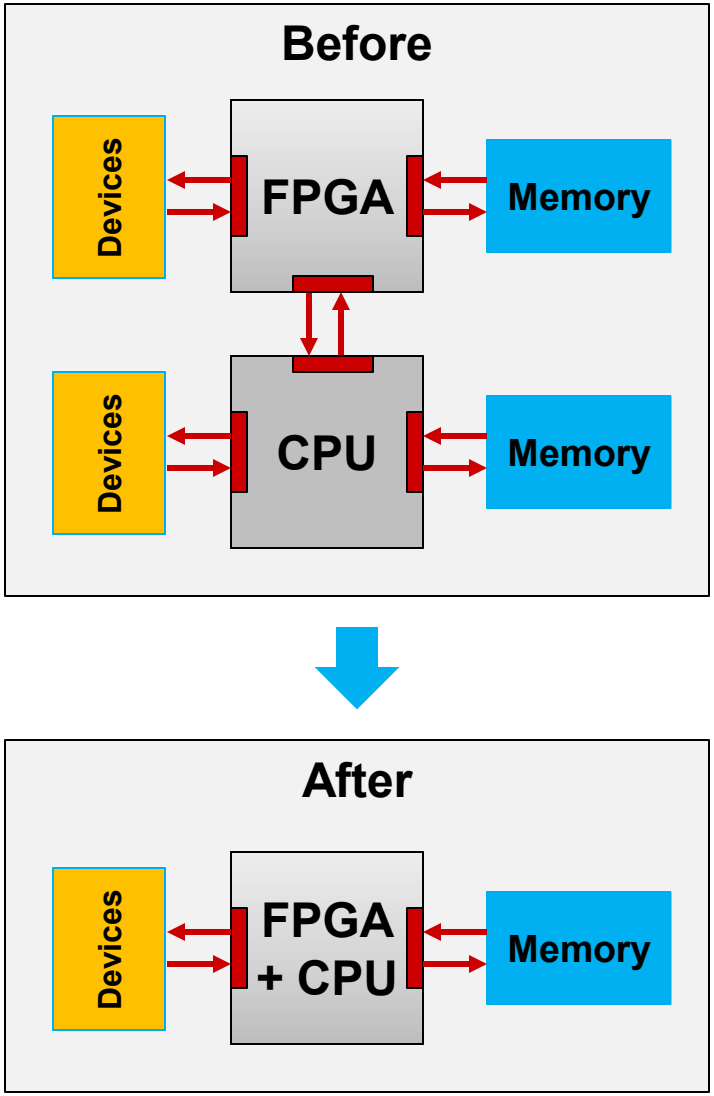


Reduced board size

- Up to 55% form factor reduction
- As few as two power rails

Reduced system costs

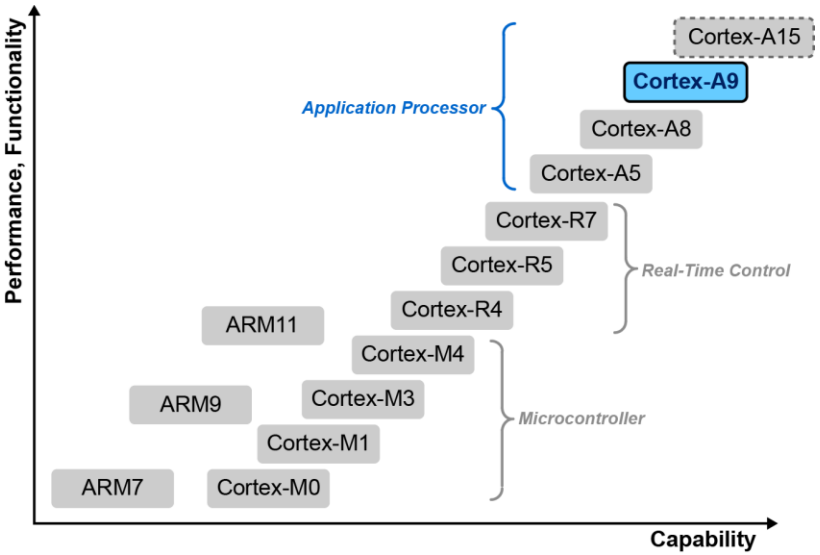
- Lower component cost
- Reduction in PCB complexity and cost
  - Less routing with fewer layers

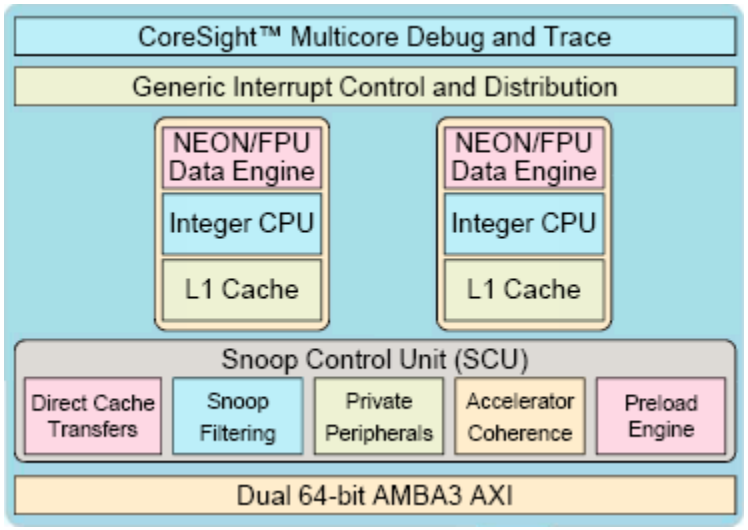


Technical Details

ARM Cortex-A9 MPCore Processor

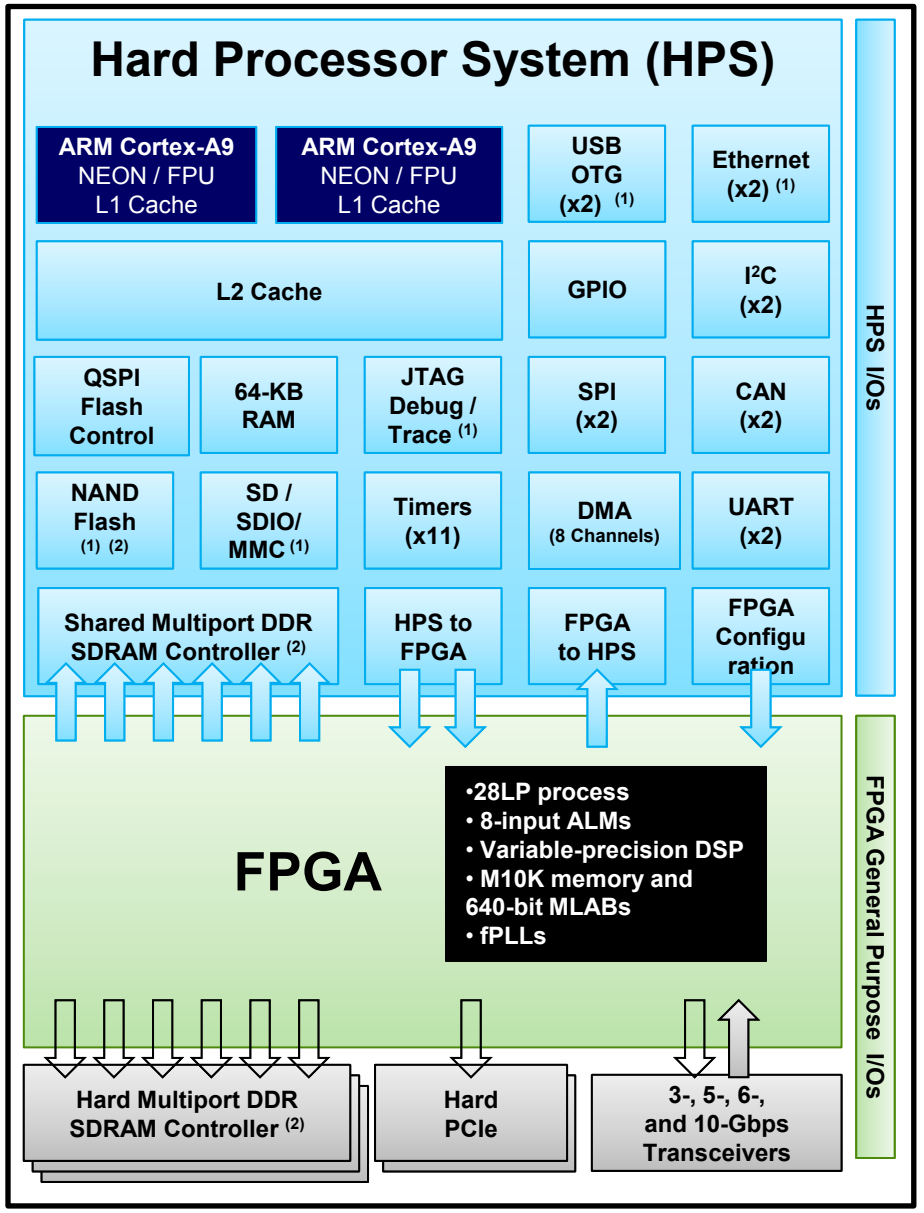
- Dual-issue superscalar pipeline
- 2.5 MIPS per MHz
- Single- and double-precision floating-point unit (FPU)
- NEON media processing engine for media and signal processing acceleration
- Coherent L1 caches
- Memory coherency maintained between processors and FPGA





System Architecture

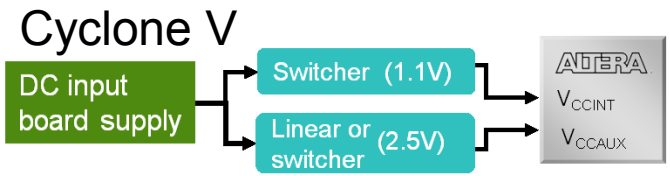
- Processor
  - Dual-core ARM® Cortex™-A9 MPCore™ processor
  - 4,000 MIPS (up to 800 MHz per core)
  - NEON coprocessor with double-precision FPU
  - 32-KB/32-KB L1 caches per core
  - 512-KB shared L2 cache
- Multiport SDRAM controller
  - Up to 533-MHz DDR3 and LPDDR2
  - Up to 400-MHz DDR2
  - Up to 200-MHz Mobile DDR
  - Integrated ECC support
- High-bandwidth on-chip interfaces
  - > 125-Gbps HPS-to-FPGA interface
  - > 125-Gbps FPGA-to-SDRAM interface
- Cost- and power-optimized FPGA fabric
  - Lowest power transceivers
  - Up to 1,600 GMACS, 300 GFLOPS
  - Up to 25Mb on-chip RAM
  - More hard intellectual property (IP): PCIe® and memory controllers

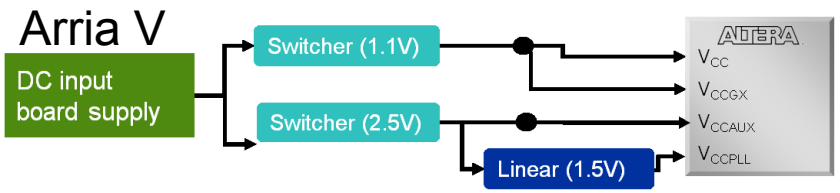


Notes:
(1) Integrated direct memory access (DMA)
(2) Integrated ECC

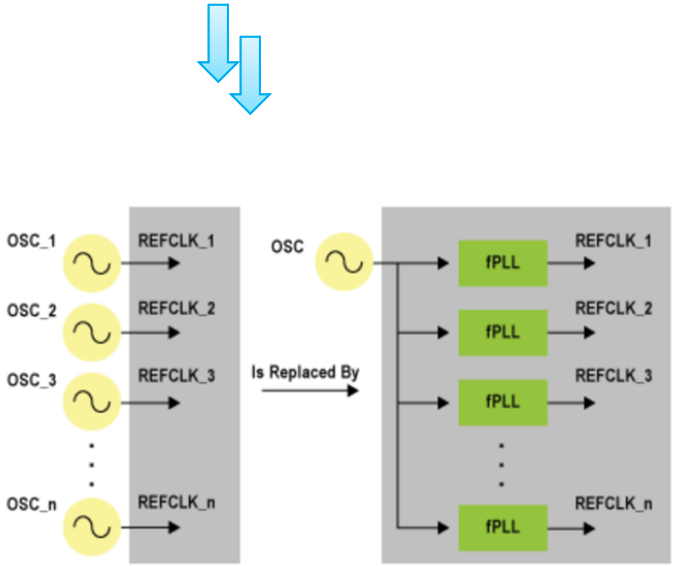
Save BOM Cost

- Power distribution networks
  - Cyclone V designs with only 2 power rails and only two switchers
  - Arria V designs with only 3 power rails using 2 switchers and 1 linear



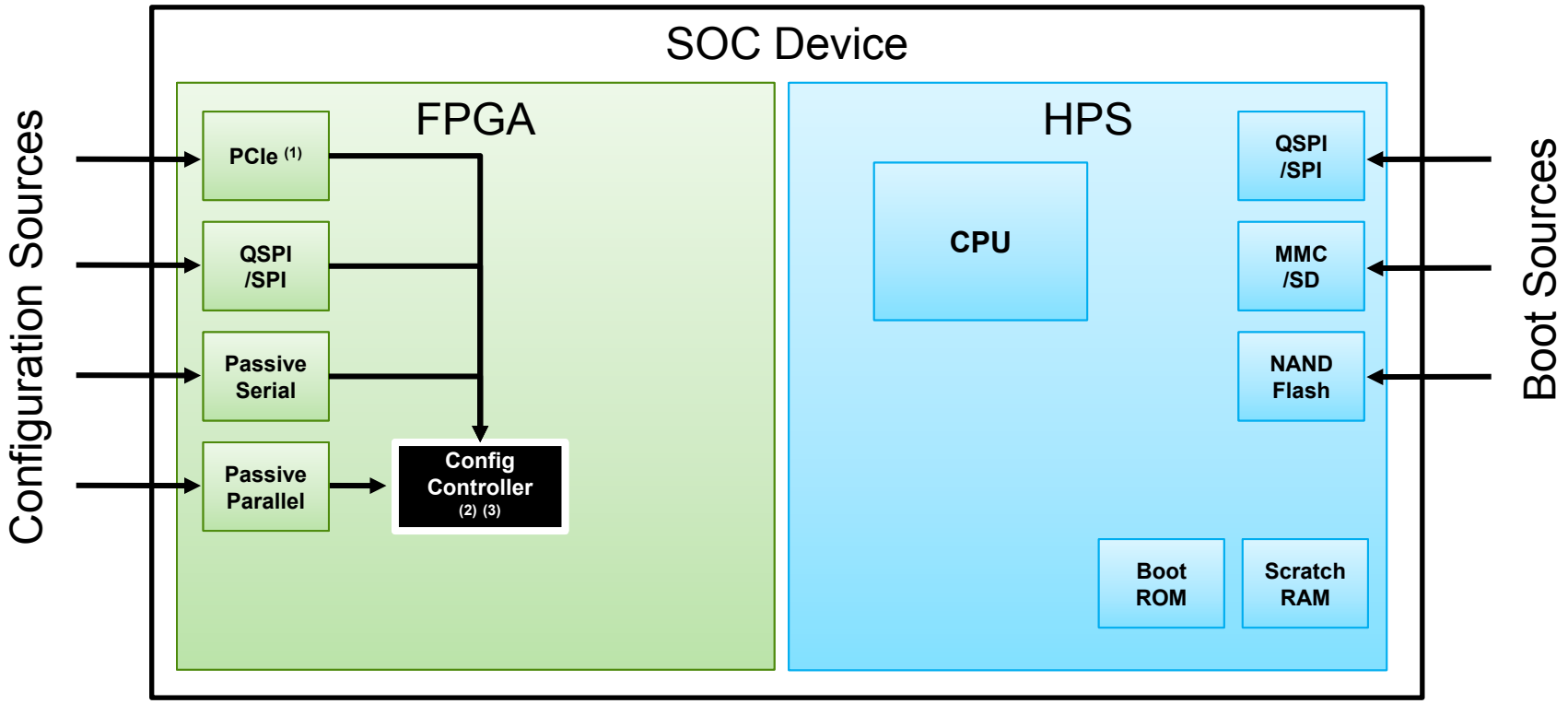


- Oscillators
  - Synthesize ANY frequency with high precision
  - Nine independent outputs from each fPLL
  - Reduce clock pins



Ultimate Configuration Flexibility

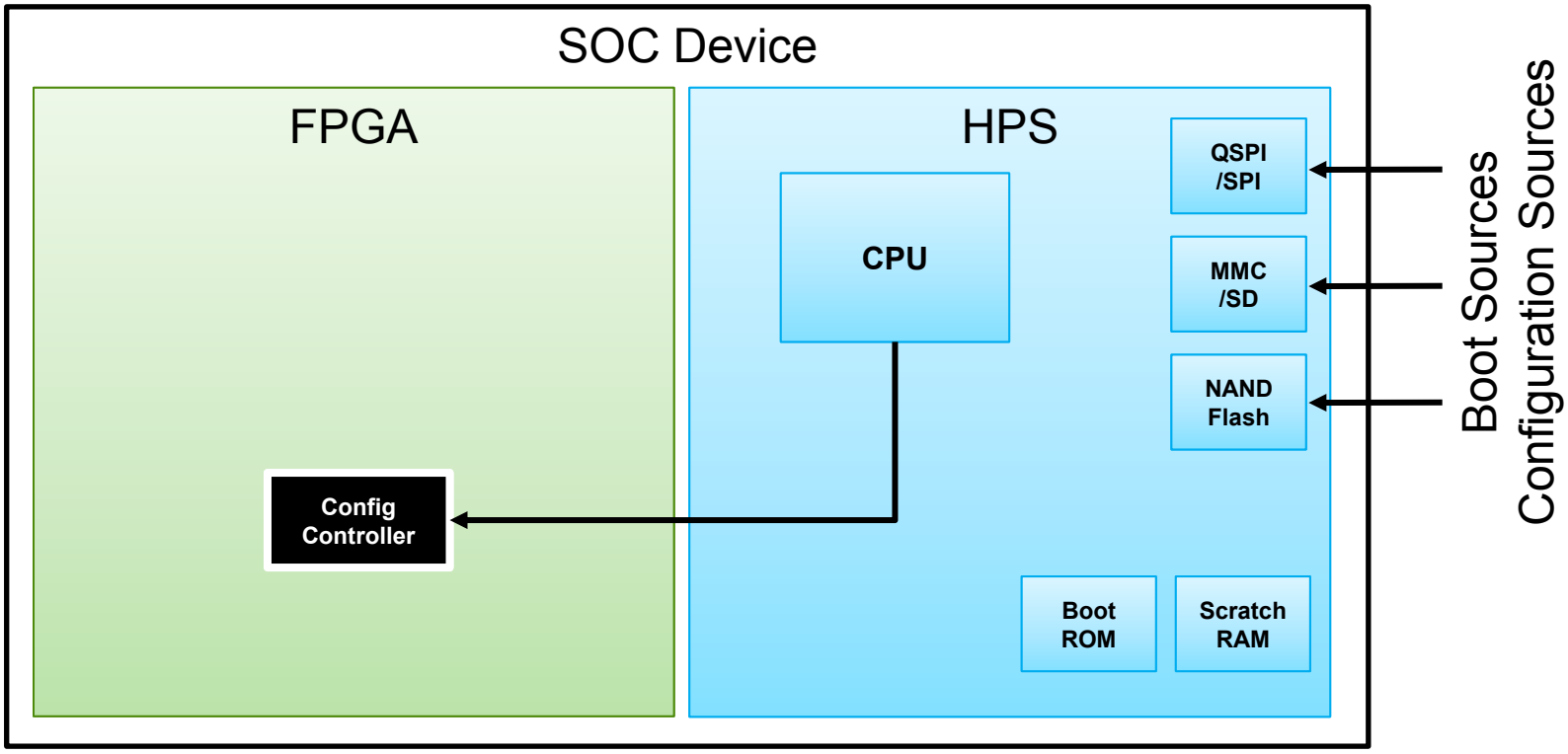
Independent FPGA configuration and processor boot



(1) Meets the PCIe 100 ms power-up-active time requirement
(2) Supports AES encryption for design security
(3) Supports partial re-configuration

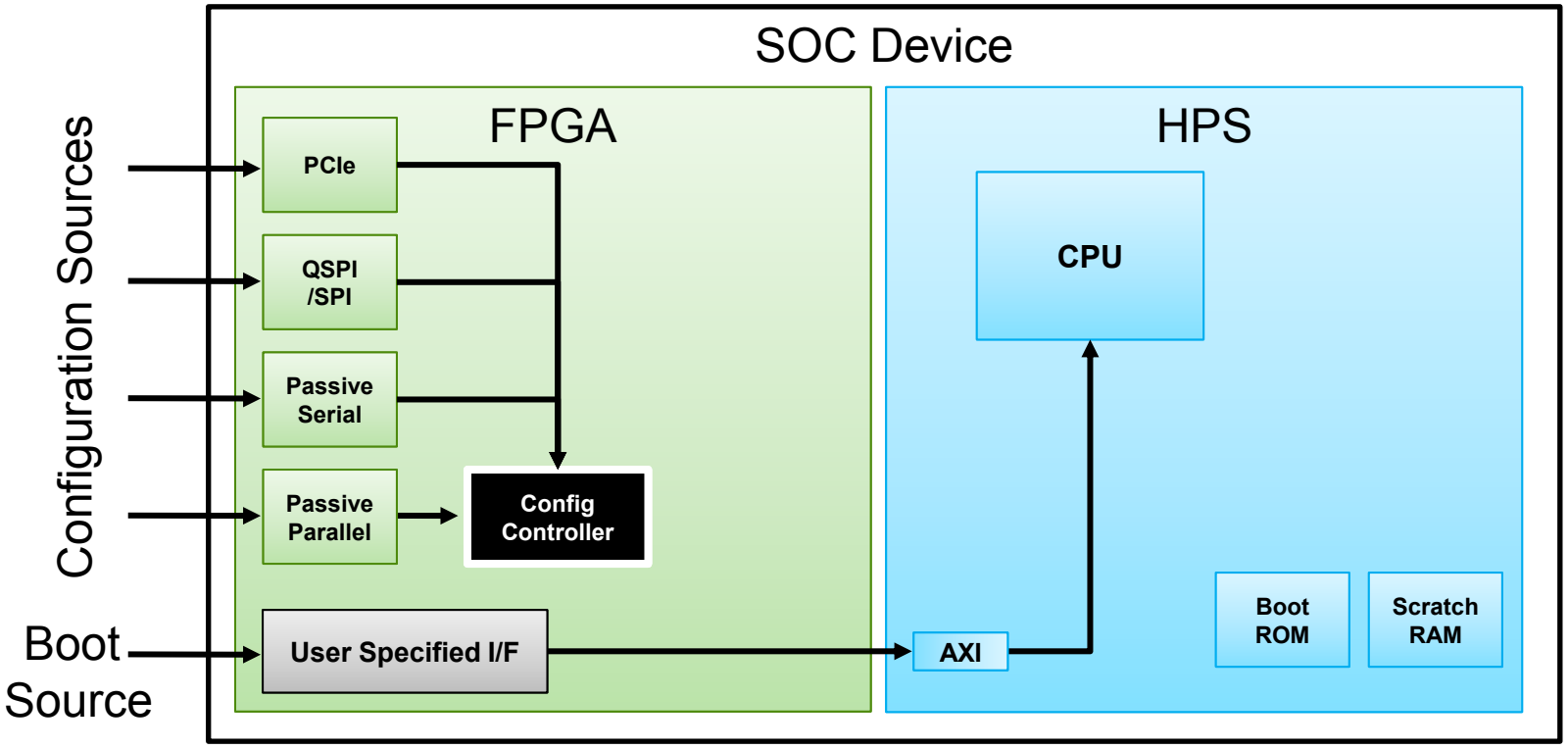
Ultimate Configuration Flexibility

Processor boots first, then configures the FPGA



Ultimate Configuration Flexibility

FPGA configures first, CPU boots through FPGA logic
(e.g. secure boot, custom backplane I/F)



Development Flow & Tools

System Development Flow

Standard FPGA Flow

Standard Software Flow

Hardware Development

- Quartus II design software
- Qsys system integration tool
- Standard RTL flow
- Altera and partner IP

Design

- ModelSim, VCS, NCSim, etc.
- AMBA-AXI and Avalon bus functional models (BFMs)

Simulate

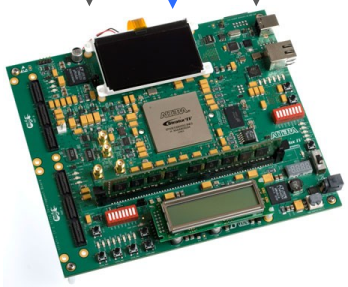
- SignalTap™ II logic analyzer
- System Console

Debug

- Quartus II Programmer
- In-system Update

Release

FPGA in the Loop



Software Development

Design

- ARM Development Studio 5
- GNU toolchain
- OS/BSP: Linux, VxWorks
- Etc…

Simulate

- Virtual Target

Debug

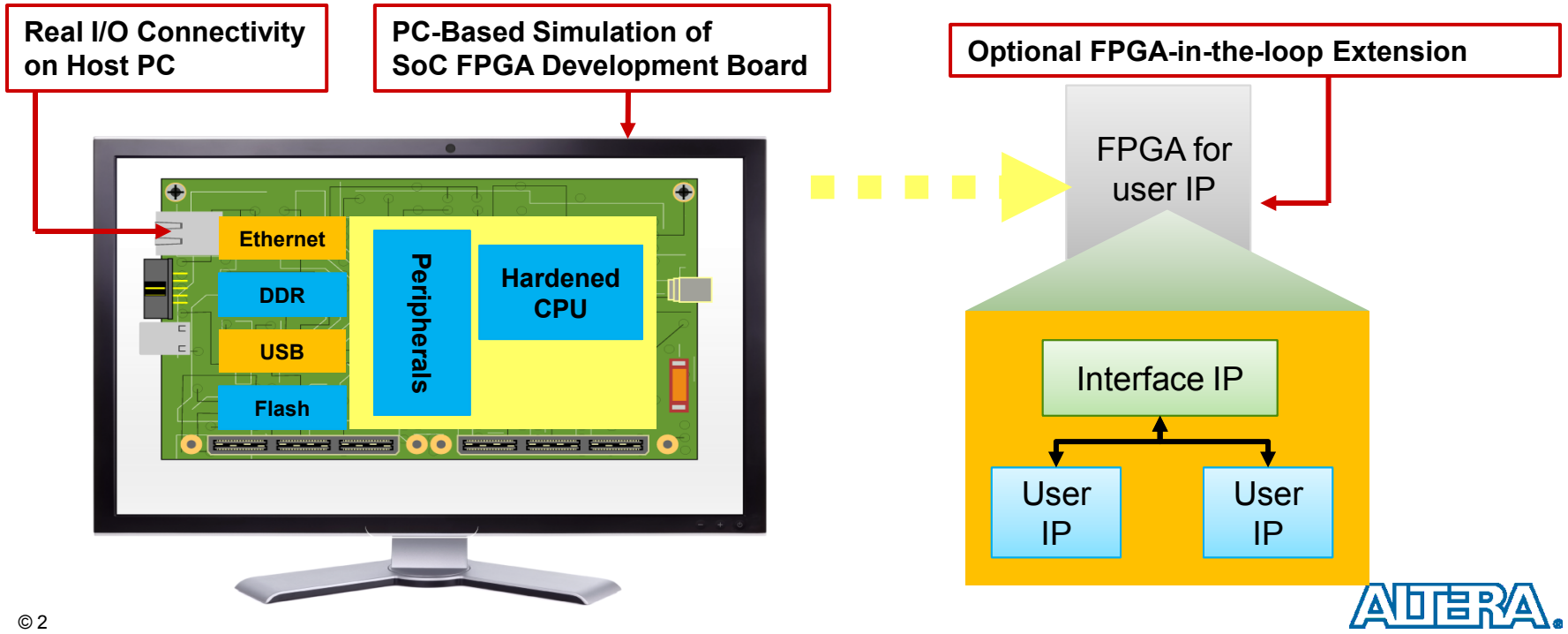
- GNU, Lauterbach, DS5 and ARM ecosystem

Release

- Flash Programmer

FPGA Industry's First Virtual Target

- Immediate device-specific software development
  - Binary- and register-compatible
- Uses proven virtual prototyping technology
- Linux and VxWorks enabled, compatible with ARM tools
- FPGA-in-the-loop extension option



Leveraging the ARM Ecosystem

Source: ARM

Leveraging the ARM Ecosystem

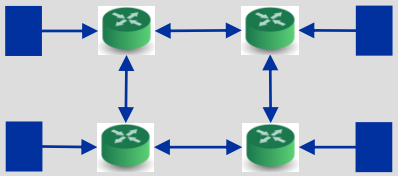
- Software Development Tools
  - GNU
  - ARM Design Studio 5 (DS-5)
  - Lauterbach TRACE32
  - Wind River Workbench

- Available on the Virtual Target Today!

	Vendor	OS/RTOS
OS Support Available on the Virtual Target	**Altera**	**Linux**
	Wind River Systems	**VxWorks**
	Micrium	**uC/OS-II**
	All major OS support in planning. Contact Altera for availability.	

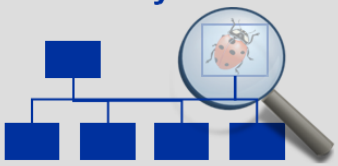
Qsys: Altera's System Integration Tool

High-Performance Interconnect



Based on Network-on-a-Chip (NoC) Architecture

Real-Time System Debug

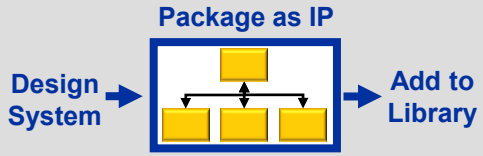


Industry-Standard Interfaces

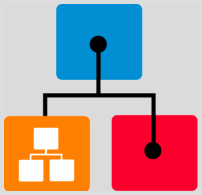
ALTERA.	Avalon® Interfaces
ARM®	AMBA® AXI3*, AXI4*

*AXI3 & AXI4 support in 2011+

Design Reuse



Hierarchy



Qsys Improves Your Productivity Where You Need It

Family plan

SoC FPGA Device Family Plan

Family	KLE	Block Memory Bits (Mb)	Var. Prec. Multiplier Blocks	Max. FPGA User I/Os	Max HPS I/Os	Max. XCVRs (GP)	Per - XCVR Max. Data Rate (Gbps)	HPS Hard Memory Controller	FPGA Hard Memory Controllers	Hard PCIe®
Cyclone V SoC FPGA	25	1.4	36	145	188	6	3	1	1	2 ea, Gen1
	40	2.2	58	145	188	6	3	1	1	2 ea, Gen1
	85	4.0	87	288	188	9	5	1	1	2 ea, Gen2
	110	5.1	112	288	188	9	5	1	1	2 ea, Gen2
Arria V SoC FPGA	350	17.3	809	528	216	30 / 16	6 / 10	1	3	2 ea, Gen2
	460	22.8	1,068	528	216	30 / 16	6 / 10	1	3	2 ea, Gen2

SoC FPGA Device Package Plan

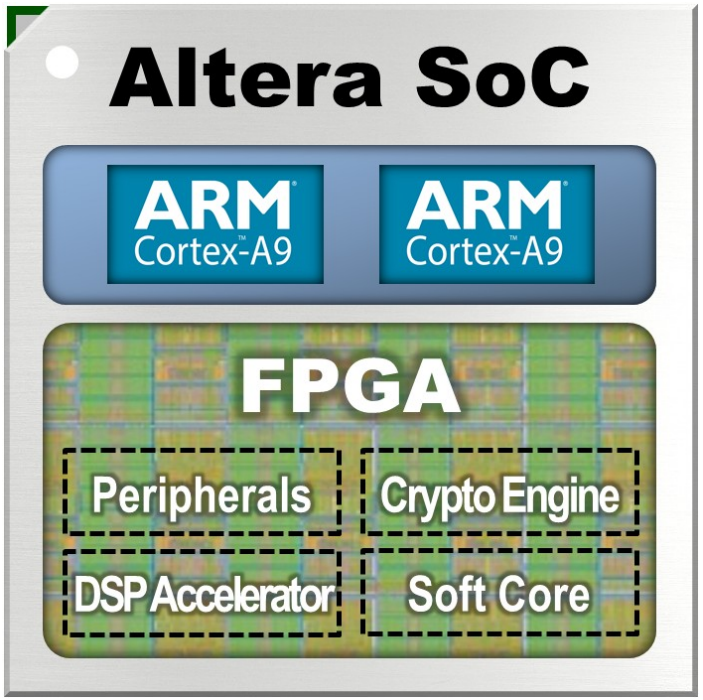
		Non-XCVR Devices (FPGA User I/Os)			XCVR Devices (FPGA User I/Os,XCVRs)				
Family	KLE	U484-WB 19x19	U672-WB 23x23	F896-WB 31x31	U672-WB 23x23 (IO,3G)	F896-WB 31x31 (IO,3G/5G)	F896-FC 31x31 (IO, 6G, 10G)	F1152-FC 35x35 (IO, 6G, 10G)	F1517-FC 40x40 (IO, 6G, 10G)
Cyclone V SoC FPGA	25	66							
	40	66							
	85	66		288		288,9			
	110	66		288		288,9			
Arria V SoC FPGA	350						170,12,4	350,18,8	528,30,16
	460						170,12,4	350,18,8	528,30,16
HPS I/O		161	188	188	188	188	216	216	216

ARM® DS-5™ Altera® Edition Toolkit

December 2012

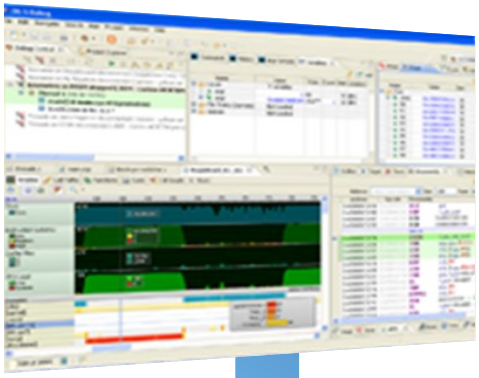
Altera SoC Devices

- Combines dual-core ARM® Cortex™-A9 MPCore™ processor system with FPGA logic
- Enables product differentiation through custom peripherals and hardware accelerators in the FPGA
- Creates new challenges for existing embedded debugging tools

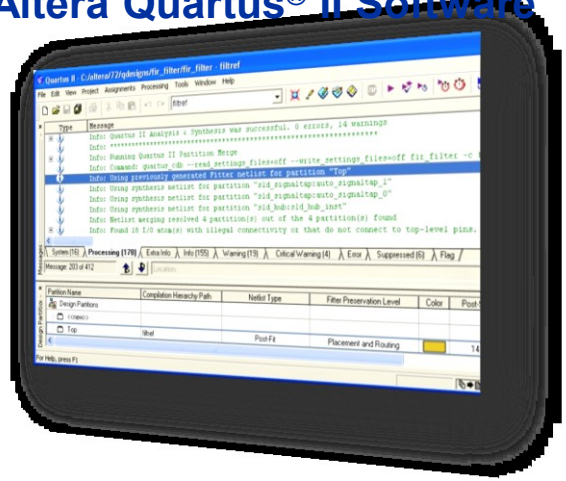


One Device, Two Debugging Tools?

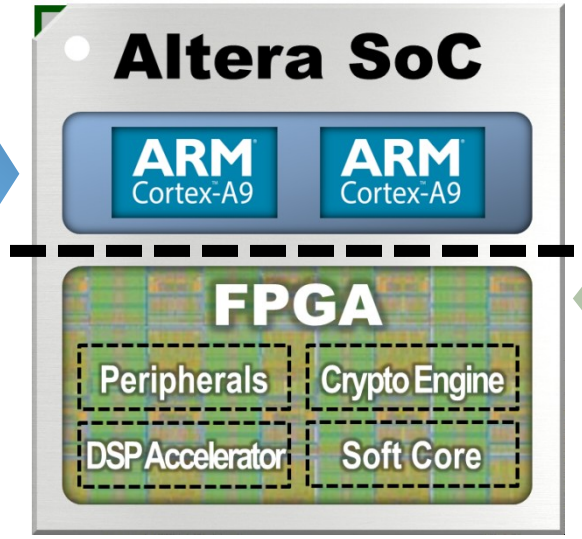
ARM® DS-5™ Toolkit



Altera Quartus® II Software



JTAG



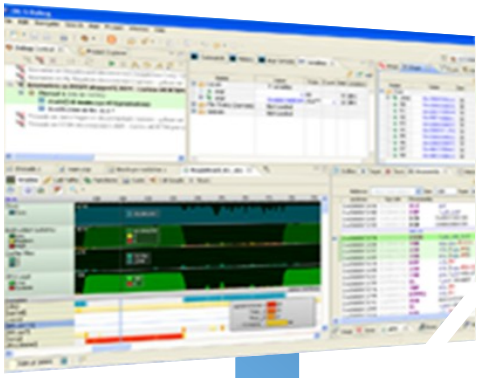
JTAG

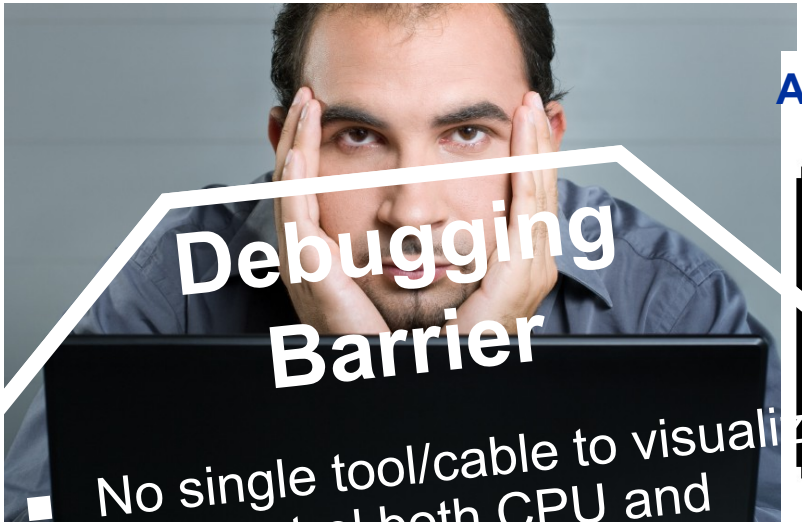
- Dedicated JTAG connection
- Visualize & control CPU subsystem

- Dedicated JTAG connection
- Visualize & control FPGA

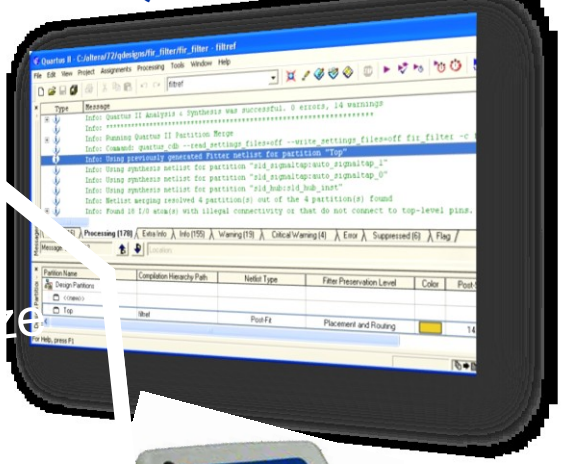
One Device, Two Debugging Tools?

ARM® DS-5™ Toolkit





Altera Quartus™ II Software



JTAG

JTAG

- Dedicated JTAG connection
- Visualize & control CPU subsystem

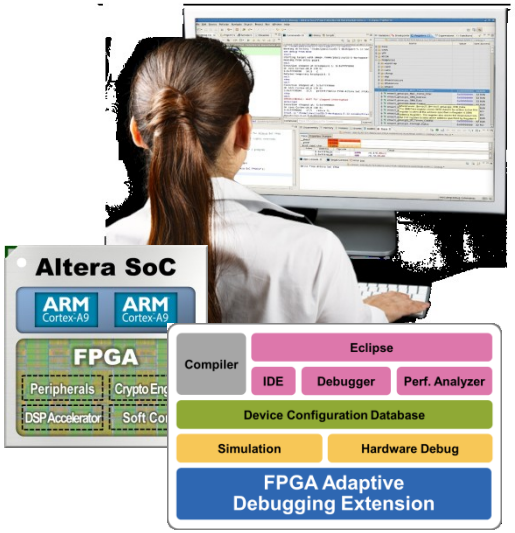
- Dedicated JTAG connection
- Visualize & control FPGA

ARM® Development Studio 5 (DS-5™) Toolkit

Industry's First *FPGA-Adaptive Software Toolkit*

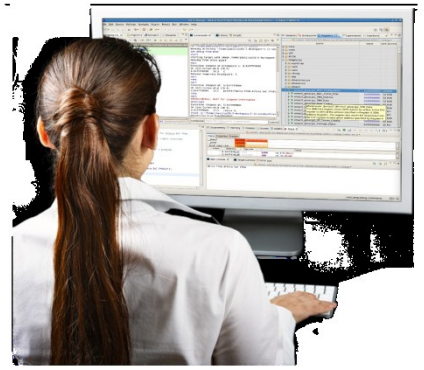
- Removes debugging barrier between CPUs and FPGA
- Unique OEM agreement between Altera and ARM
- Result of innovation in silicon, software, and business model

Unprecedented Combination of Productivity-Boosting Features

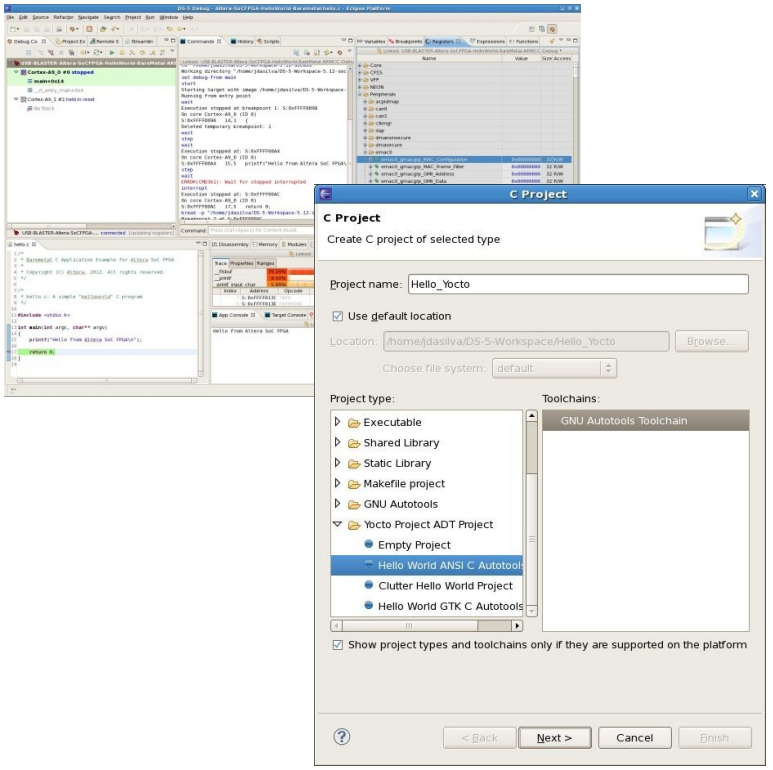


- Single USB-Blaster target connection for software and hardware debug
- Automatic creation of register views of FPGA peripherals
- Non-intrusive trace of CPU software instructions correlated with application events and FPGA hardware events
- Hardware cross-triggering between the CPU and FPGA domains
- Simultaneous debug and trace for Cortex-A9 cores and CoreSight™-compliant cores synthesized on FPGA
- Streamline support: Statistical analysis of software load and bus traffic spanning the CPUs and FPGA

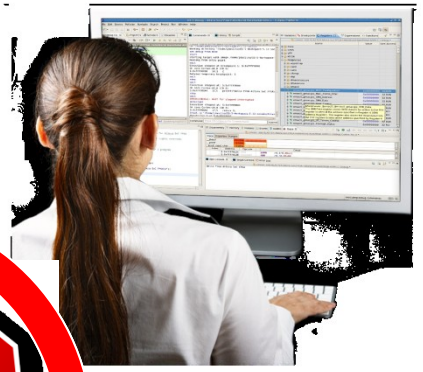
Unprecedented Combination of Productivity-Boosting Features



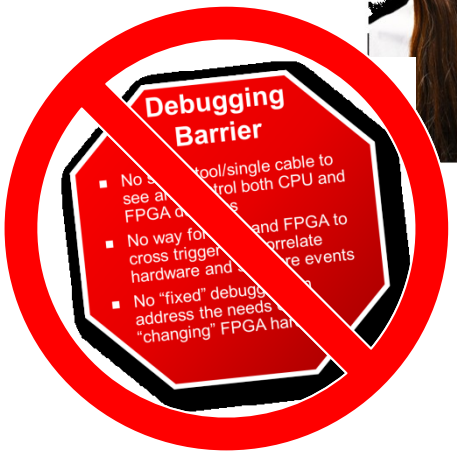
- Industry's most advanced multicore debugger for ARM
- JTAG based system-level debugging, gdbserver-based application debugging in one package
- Yocto plugin to enable Linux based application development
- Integrated OS-aware analysis and debug capability



Key Benefits for Developers



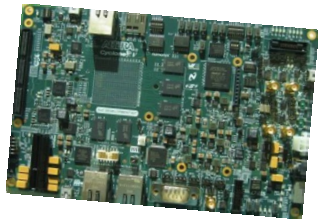
Removes Debugging Barrier!



- **Faster time to market, lower development costs**
- Significant productivity gains
- Provides software debug views of full SoC by adapting to changing FPGA designs
- Unprecedented visibility and control across processor cores and across CPU, FPGA domains
- Standard, widely used, familiar DS-5 user interface provides SW engineers with rapid starts
- OEM packing ensures ease of licensing and ease of use

Pricing and Availability

Two Configurations	Pricing	Availability
■ Altera SoC Embedded Design Suite (Altera SoC EDS)	■ $995	■ Early 2013
■ Altera Cyclone V SoC Development Kit	■ $1,595	■ April 2013



Thank You