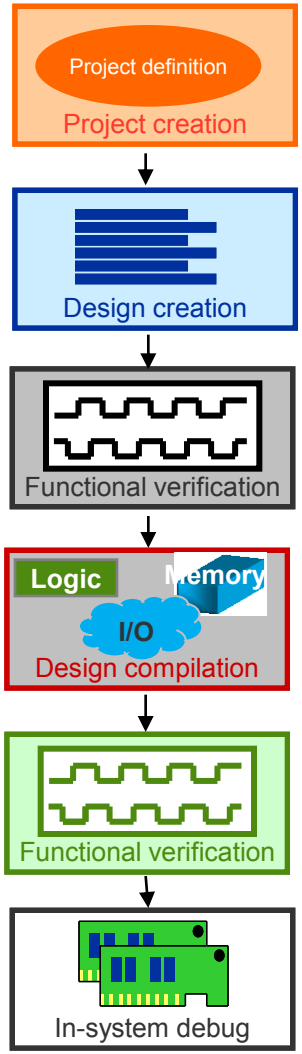
Advanced Development Environment: Quartus II

Altera Technology Roadshow 2013

Typical FPGA Design Flow



Functional verification
- Verify design behavior

Functional verification
- Verify design will work in target technology

Design entry/RTL coding and early pin planning
- Behavioral or structural description of design
- Early pin planning allows board development in parallel

Synthesis (mapping)
- Translate design into device-specific primitives
- Optimization to meet required area and performance constraints

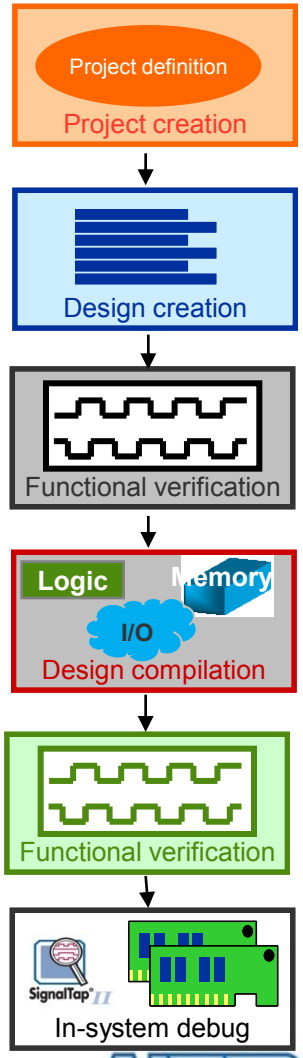
Placement and routing (fitting)
- Place design in specific device resources with reference to area and performance constraints
- Connect resources with routing lines

Timing analysis
- Verify performance specifications were met
- Static timing analysis

PC board simulation and test
- Simulate board design
- Program and test device on board
- On-chip tools for debugging

Advanced Development Environments: Quartus II

- **Quartus II: the fully integrated development tool**
  - Multiple design entry methods
    - Includes intellectual property- (IP-) based system design
  - Up-front I/O assignment and validation
    - Enables printed circuit board (PCB) layout early in the design process
  - Incremental compilation
    - Reduces design compilation and improves timing closure
  - Logic synthesis
    - Includes comprehensive integrated synthesis solution
    - Advanced integration with third-party EDA synthesis software
  - Timing-driven placement and routing
  - Physical synthesis
    - Improves performance without user intervention
  - Verification solution
    - TimeQuest timing analyzer
    - PowerPlay power analysis and optimization
    - Functional simulation
  - On-chip debug and verification suite



Altera is Focusing on Today's Design Challenges

Designers come from varied backgrounds	Larger devices need longer compile times	Design requirements are tighter than ever
Design Entry	***Compile Time***	***Timing Closure***
Tailored design flows for targeted users	*Fastest compile times in FPGA industry*	*Highest performance in FPGA industry*
Innovation	***Productivity***	***Performance***

Altera is the Leader in Innovation, Productivity & Performance

History of Software Innovation & Leadership

Multiprocessor Support
- Quad-core support

Multiprocessor Support
- Industry's first
- Dual-core support

TimeQuest Timing Analyzer & SDC support
- Industry's first
- ASIC Strength

PowerPlay Power Optimization
- Industry's first

Design Space Explorer
- Automatic compilations with multiple optimization settings

System Verilog

VHDL 2008

System Console
- Address-based reads/writes

- Advanced blockset

Industry 1st!

sys

- Industry's first
- System integration tool
- Network-on-chip interconnect architecture
- Industry standard interfaces

OpenCL

Industry's first FPGA support

2003

2013

Many Industry Firsts

Many More to Come

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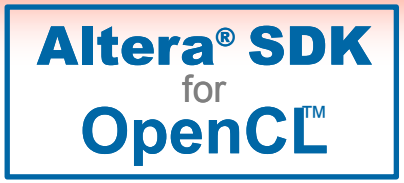
Breakthrough Productivity

Hardware Designer	DSP Designer	Software Developer	
			
Industry's Fastest Compile Times	**Industry's Only** Model-Based, Performance-Driven HLS Tool	**Industry's Only** FPGA-Adaptive Debug	**Industry's Only** OpenCL Solution for FPGAs

Attack Your Design from Any Level of Abstraction

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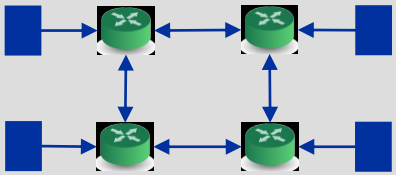
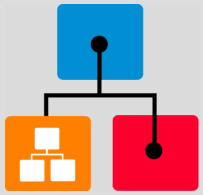
Qsys: Altera's System Integration Tool

High-Performance Interconnect

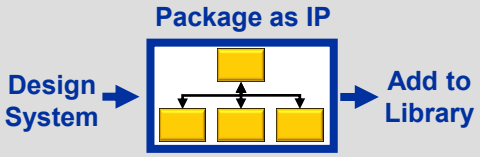


Based on Network-on-a-Chip (NoC) Architecture

Hierarchy



Design Reuse

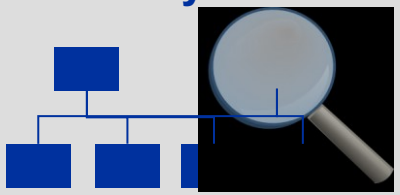


Industry-Standard Interfaces

ALTERA.	Avalon® Interfaces
ARM®	AMBA® AXI3*, AXI4*

*AXI3 & AXI4 support in 2011+

Real-Time System Debug



Let Qsys Improve Your Productivity Where You Need It

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DSP Builder Advanced Blockset Advantages

Competitor Altera

- **High-level DSP design with "hand-coded" performance**
  - Automatic datapath pipelining and DSP block configuration
- **Reduced area use with automatic datapath folding**
  - Time-domain multiplex clock to share resources within design
- **Fast development with automatic poly-phasing**
  - DSP Builder auto-phases clock to drive multi-GHz data rates
- **Flexible floating point implementation**
  - High performance matrix operation library (QR, Cholesky)
    - Pipelined matrix decompositions to reduce data dependencies
  - Floating point compiler (fused data-path technology)
    - 50-75% resource reduction and latency reduction

Achieve Performance of Hand-Coded DSP Design!

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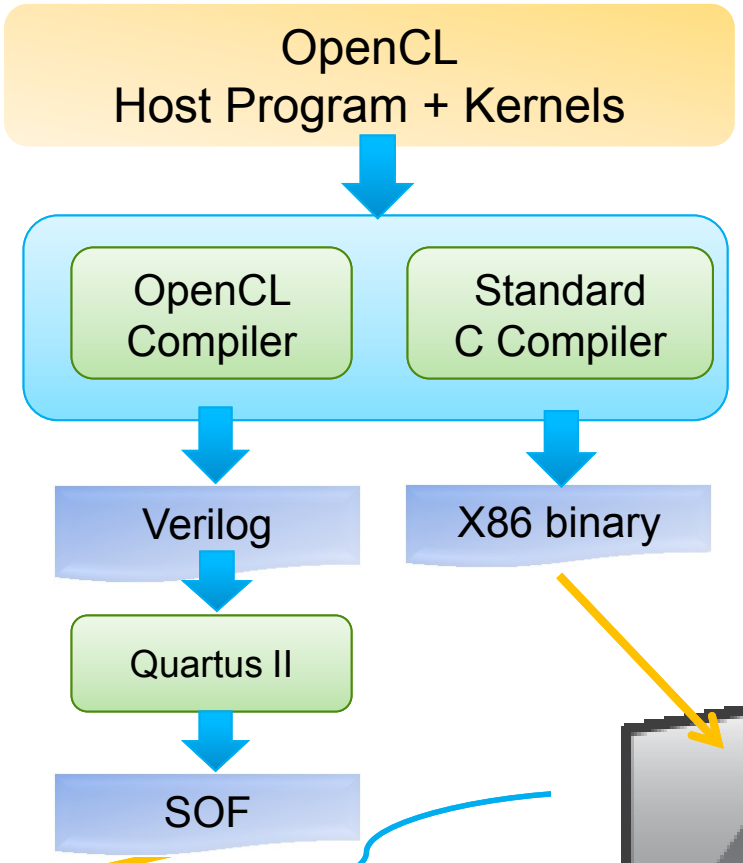
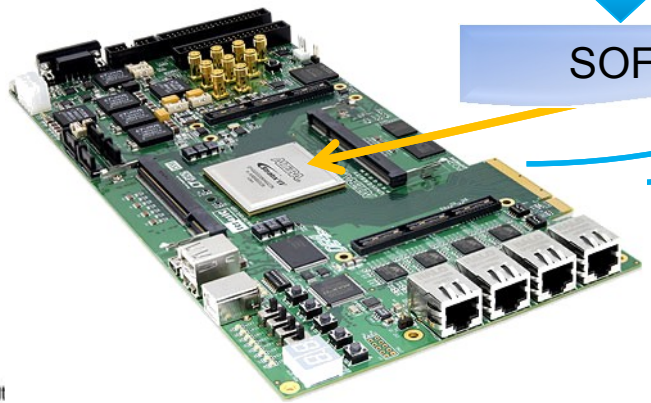
Altera OpenCL SDK – Industy's Only FPGA Solution

- Design hardware without need for FPGA knowledge or experience
- Target FPGA from software entry
- Rapidly iterate high-performance system design




```
main() {
    read_data( … );
    maninpulate( … );
    clEnqueueWriteBuffer( … );
    clEnqueueNDRange(…,sum,…);
    clEnqueueReadBuffer( … );
    display_result( … );
}
```

```
__kernel void
sum(__global float *a,
    __global float *b,
    __global float *y)
{
  int gid = get_global_id(0);
  y[gid] = a[gid] + b[gid];
}
```



Implement FPGAs with OpenCL

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Software Productivity: Compile Time

- **Explosive density**

Max Logic Density (in KLEs)	65nm	40nm	28nm	20nm	14nm
Stratix	340	820	950		4000+
Arria		350	500	1150	
Cyclone	150		300		

- **Altera is addressing compile time challenges by:**
  - **Faster raw compile speed**: for high density designs, Altera offers 2-3X faster compilation times compared to the nearest competitor
  - New Feature - **Rapid Recompile**: Small design changes can now be made without a full re-compile, which reduces compilation times by 2x-5x average versus running another full compile
  - **Parallelization** - Multi-core computing: targets supporting 64~128 CPU cores in a small group of servers in near term

Increasing Pace of Compile Time Improvement

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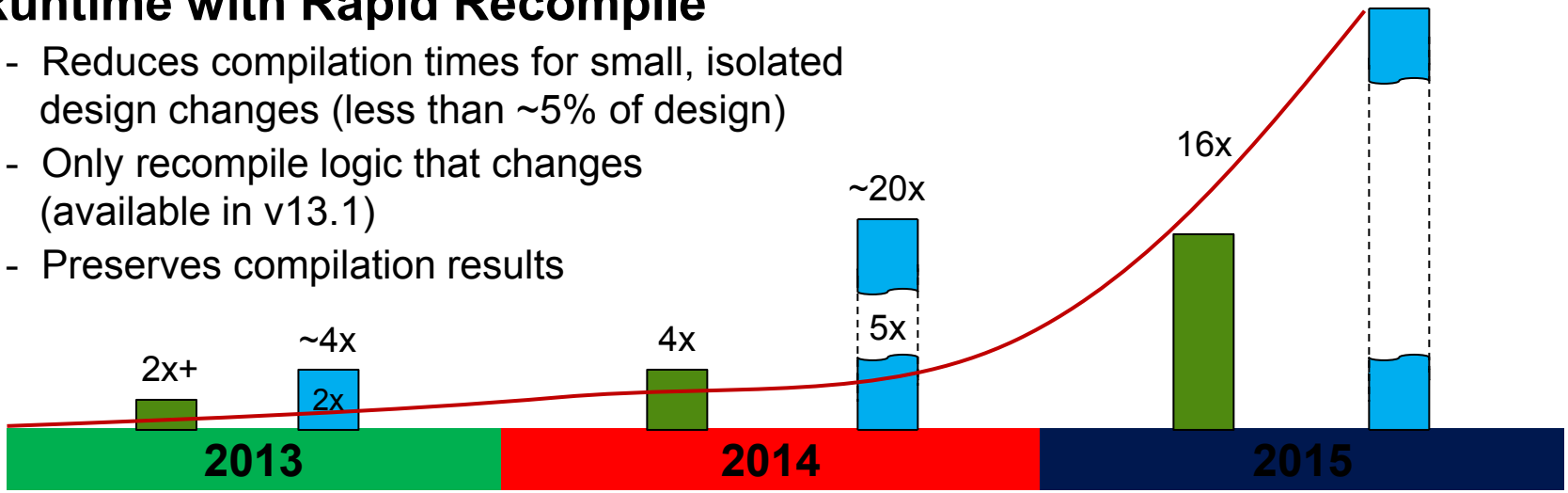
Roadmap to Continuing Compile Time Reduction

- **Compile time acceleration vs. 2012 results**
- **Runtime with Rapid Recompile**
  - Reduces compilation times for small, isolated design changes (less than ~5% of design)
  - Only recompile logic that changes (available in v13.1)
  - Preserves compilation results



	2013	2014	2015
Compile Time	**350K LE/hour** **Rapid Recompile – 2x Compile Time Reduction for 5% Logic Change**	**500K LE/hour** **Rapid Recompile – 5X Reduction in Compile Time for 5% Logic Change**	**2M LE/hour** **Parallelization**

Altera Extends Compile Time Leadership

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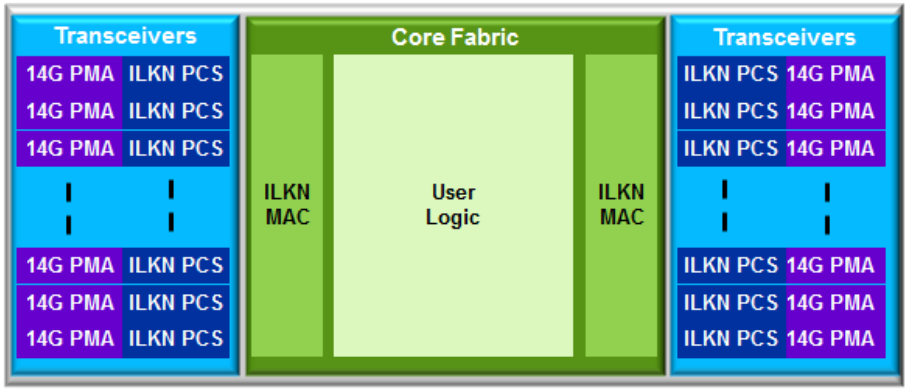
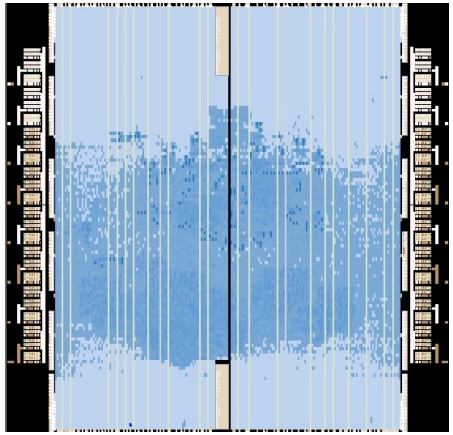
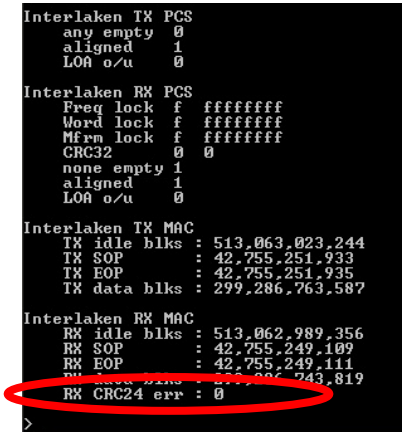
High Performance Leadership Example 1 (Quartus II)

- **Very high performance (500G) Interlaken prototype**
  - Fat data pipe coming into FPGA
    - 36 lanes @ 13.8Gbps = 500Gbps
  - 1280-bit wide data-path
  - Complex place & route challenge
  - Fmax requirement of 390MHz

- **Quartus II software results**
  - Fit into a Stratix V A7 (C2) FPGA in <42.7K ALMs and <99K Register
  - Met timing with 20% margin (468MHz)







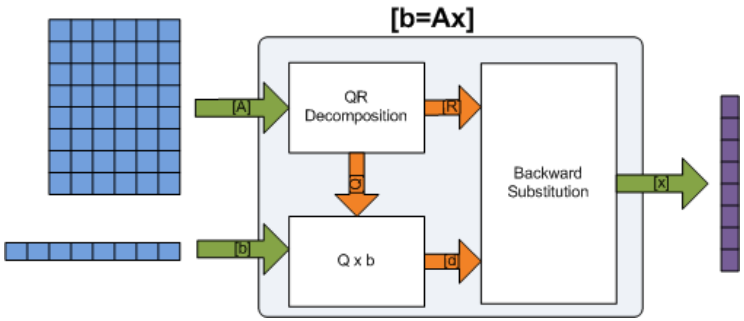
Fast timing closure
Easy integration with rest of design
Reduced cost through lower speed grade

Quartus II Software Enables Unmatched System Performance

High Performance Example 2 (DSP Builder Adv. Blockset)

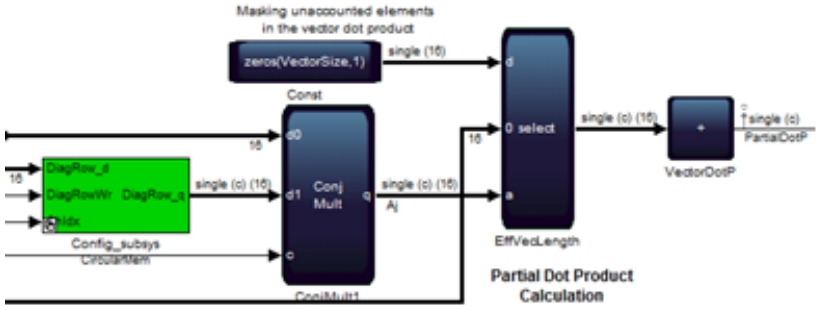
- **First demonstration of very large floating point matrix inversion in FPGAs**
  - Made highly parameterizable with DSP Builder Advanced Blockset
- **1 million matrices/s – (Cholesky 20x20 Matrix Inversion)**
  - No competing solution can provide this level of throughput

QR Decomposition



Matrix Size/ Vector Size	Fmax [MHz]	Throughput kMatrices/s	Latency [µs]
50x100/50	259	32.82	43.3
100x200/50	260	6.17	204.5
100x200/100	207	8.76	167
400x400/100	203	0.315	3970

Cholesky



Channel Size/ Matrix Size/ Vector Size	Fmax [MHz]	Throughput kMatrices/s	Latency [µs]
1 / 360x360 / 90	189	1.43	1112
20 / 60x60 / 60	234	118	330
64 / 30x30 / 30	288	544	222
50 / 20x20 / 20	236	1000	98.6

*BDTI verified: http://www.altera.com/literature/wp/wp-01187-bdti-altera-fp-dsp-design-flow.pdf

High Performance Example 3 (OpenCL)

- **Wall street option pricing algorithm**
  - Monte-Carlo simulation
    - Heston Model

$$dS_t = \mu S_t dt + \sqrt{v_t} S_t dW_t^S$$

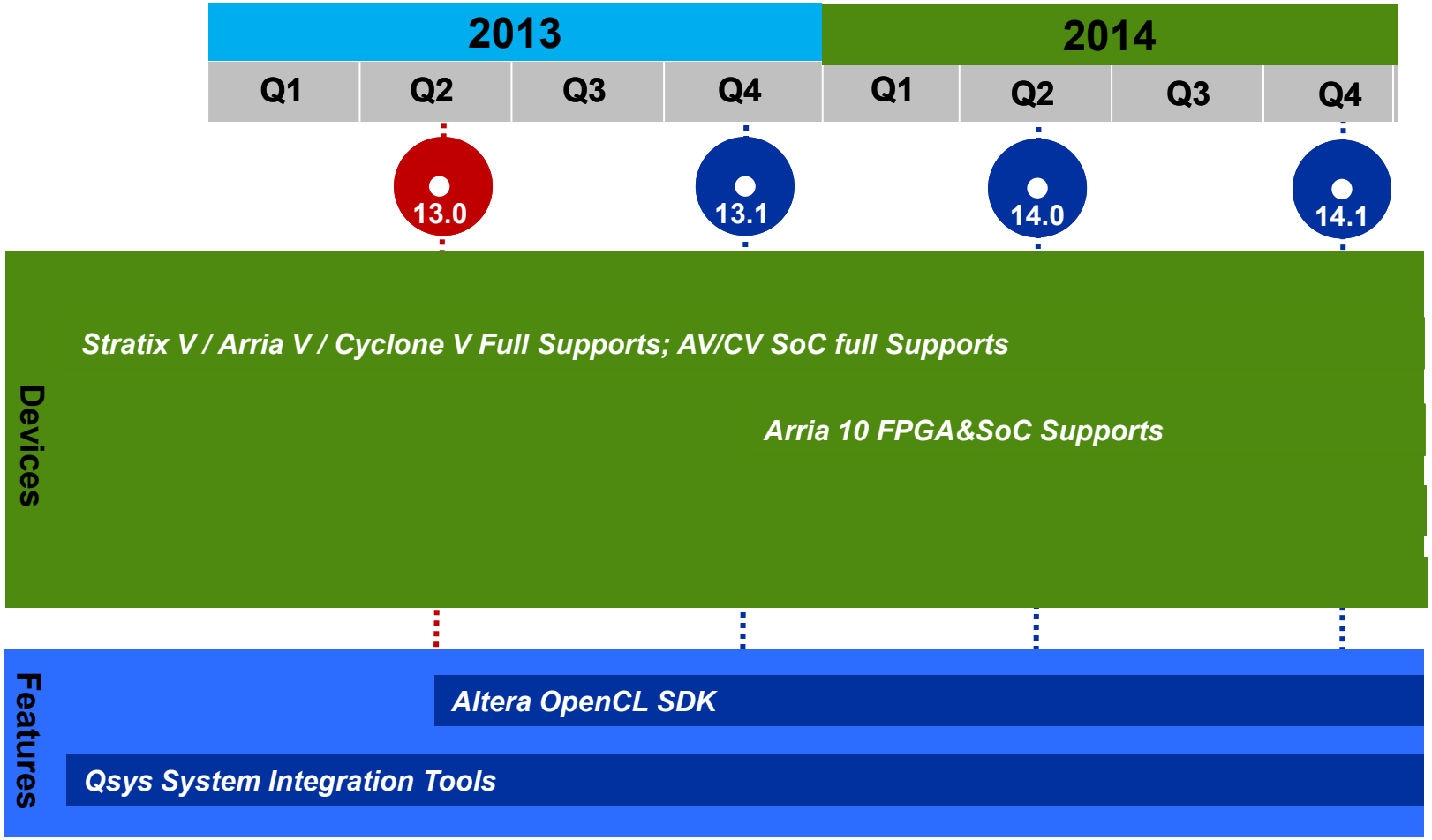
$$dv_t = \kappa(\theta - v_t)dt + \xi\sqrt{v_t} dW_t^v$$

    - ND Range
      - Assets x Paths (64x1000000)
- **FPGA advantage**
  - Complex control flow
- **Results**

Platform	Power (W)	Performance (Msims/s)	Msims/W
W3690 Xeon Processor	130	32	0.25
nVidia Tesla C2075	225	63	0.28
PCIe385 D5 Accelerator	23	170	7.40

Ultra Fast Hardware Starting from C-Level Abstraction!

Release Strategy



Summary

- **More and more complex system requirements heavily challenge FPGA&SoC development environments**

- **Quartus II offers the breakthrough advantages and solutions**
  - Innovations: Qsys, OpenCL
  - Productivity: Quicker compile time; DSP Builder; eSW
  - Performance: Highest performance in FPGA industry

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Thank You