Drive Control

Altera Technology Roadshow 2013

Challenges for Drive Manufacturers

Performance Improvements

- Higher switching frequencies, higher dynamic response
- Adapting to latest technologies
- Multi-axis, On-line Diagnostics

Differentiation While Lowering Costs

- Multiple Industrial Ethernet (IE) and encoder protocols
- Integrating functions into fewer components, drive miniaturization, platforms

Implementing Functional Safety

-Cost overhead and time to market impact

- Not always customer core competence

Challenge Across All Types of Drives Manufacturers

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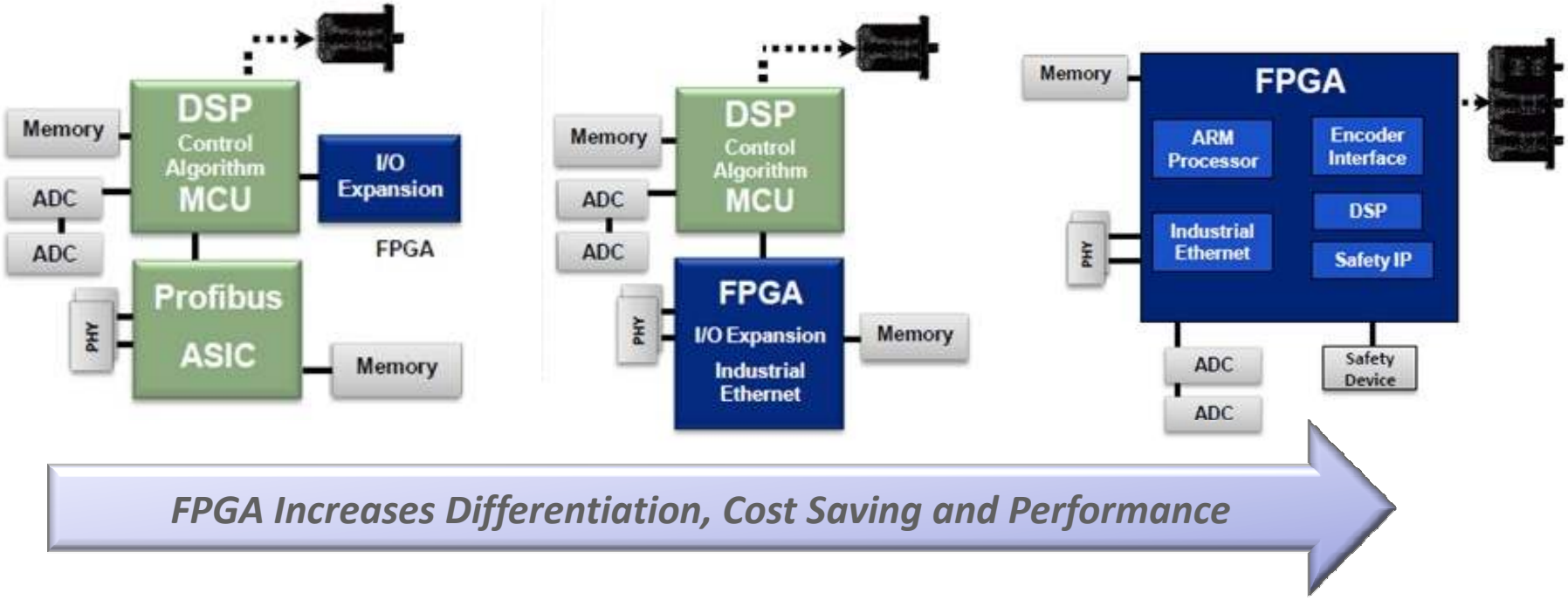
FPGA in Drives



FPGA Increases Differentiation, Cost Saving and Performance

- Low Cost Altera FPGA as an I/O expansion

- I/O Expansion
- Industrial Ethernet and Fieldbus IP
- Encoder IP
- Control Algorithm – HW Acceleration

- Cost and Performance optimized integrated ***Drive-on-a-Chip***
- Multi-axis control – significant system cost reduction

As FPGA Content Increases, System Costs Decreases!

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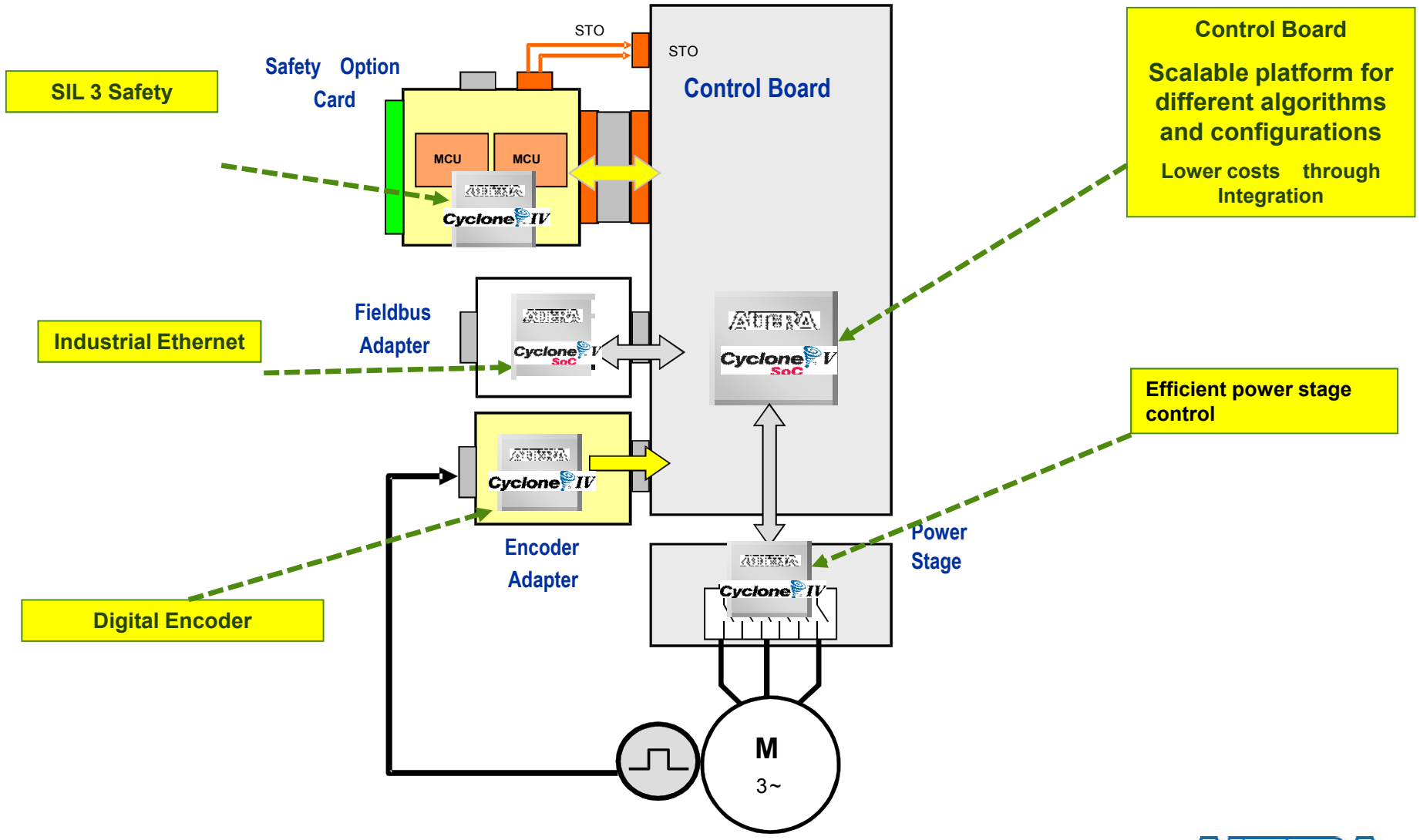
Drive Content Expansion with FPGA

Open



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Altera Industrial Ethernet Solution

Industrial Ethernet Solution 2013

SLAVE Protocols

Profinet RT/IRT
Powerlink
Ethernet/IP
ModBus TCP/IP
Profibus

&
EtherCAT

All protocols enabled by the same CPLD – one at a time
All protocols have a common SW API and a common HW interface

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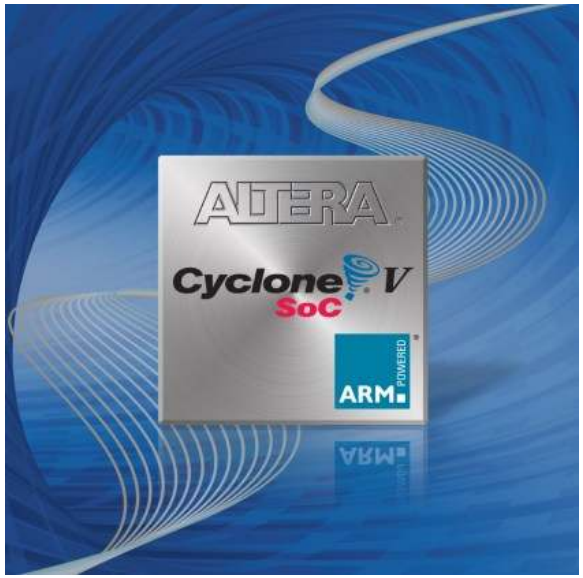
Altera Industrial Ethernet Roadmap



2013

- **Include EtherCAT within the same model**
  - One CPLD for ALL protocols
- **Optimize protocols for CV SoC**
  - Use the hard IP – HMC, EMAC, A9

2014

- **Optimize protocols for next generation low cost components**

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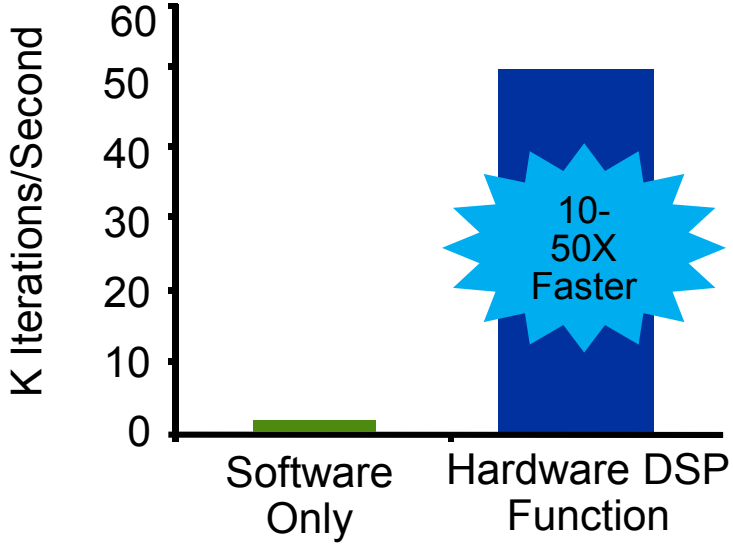
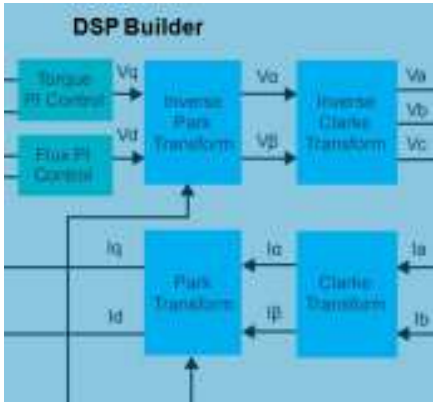
FPGA Co-Processors for CPU/MCU

- **Offload DSP algorithm from CPU**
  - Custom hardware block implements complete DSP datapath, **offloads CPU** to run other tasks
  - Memory mapped register access between CPU & hardware
  - Floating-point and variable width fixed-point arithmetic supported





FOC DSP Co-Processor

Algorithm	Folding	LE Usage	Multiplier Usage	Algorithm Latency (µs)
Floating-point single-precision	None	20K	56	1.0
Floating-point single-precision	Enabled	7.5K	5	1.73
16-bit fixed-point	None	3K	16	0.22
16-bit fixed point	Enabled	2K	1	0.88

…scales to multiaxis at close to zero additional cost/latency

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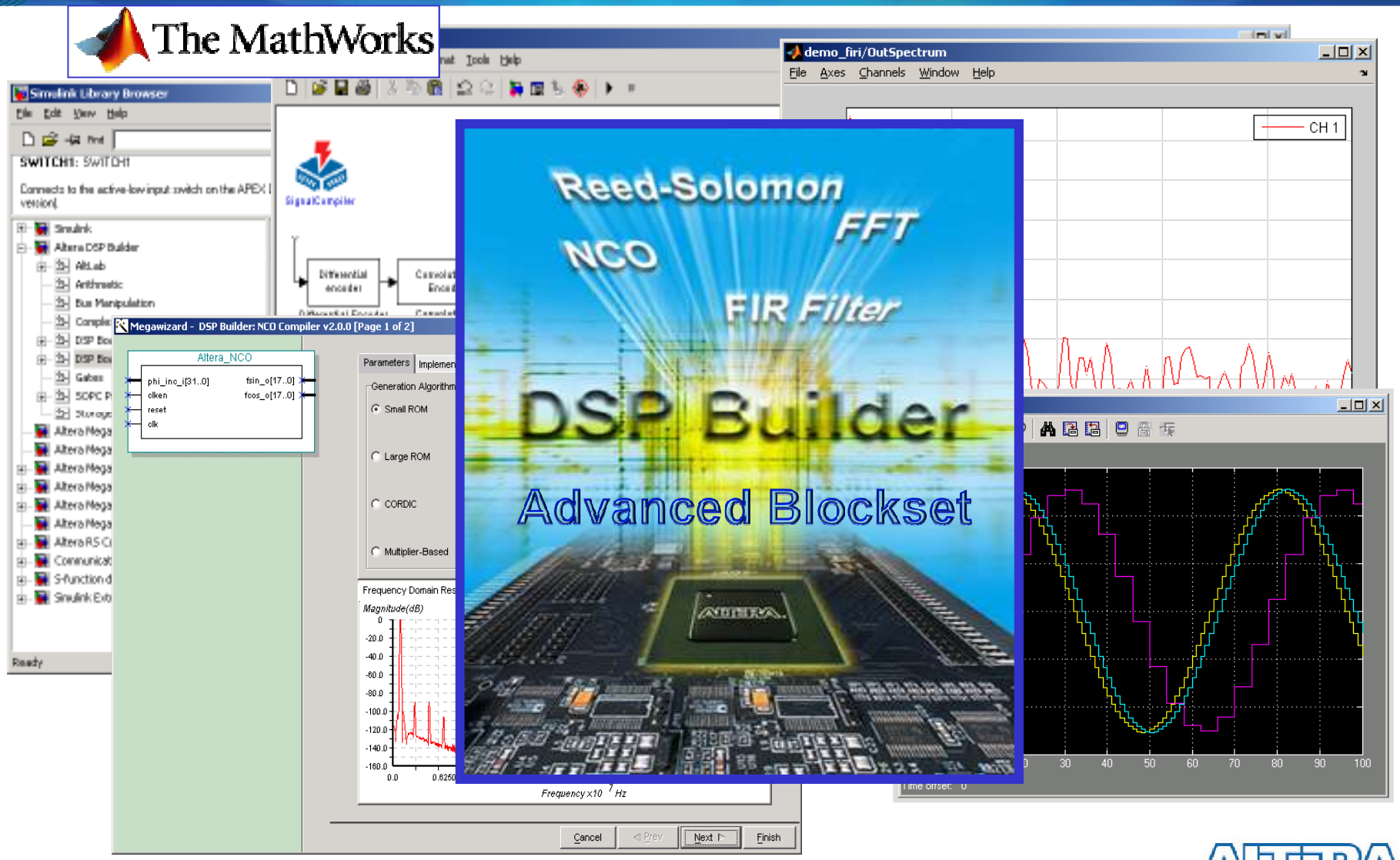
Altera DSP Builder – Quick Algorithm Implementation



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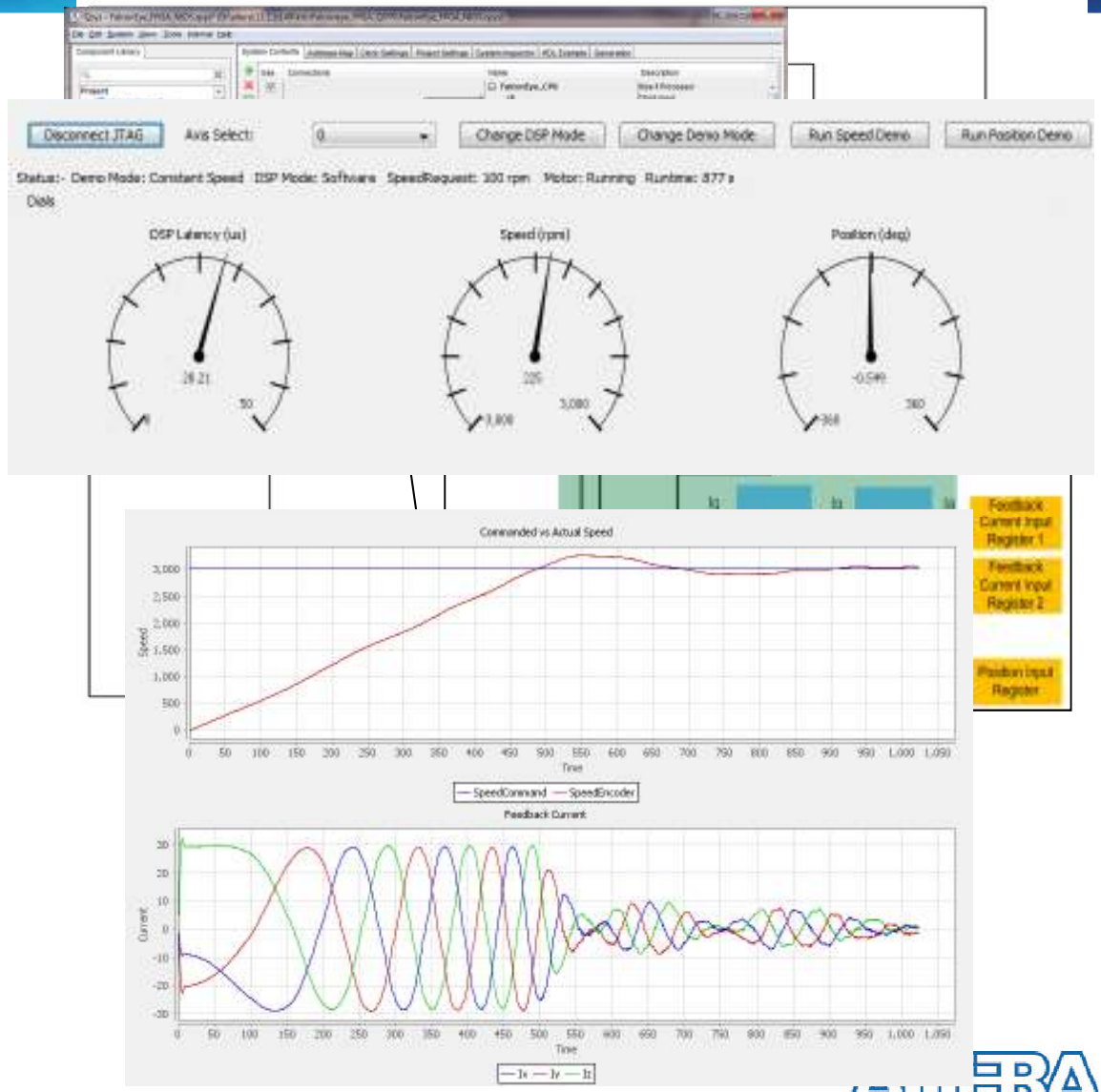
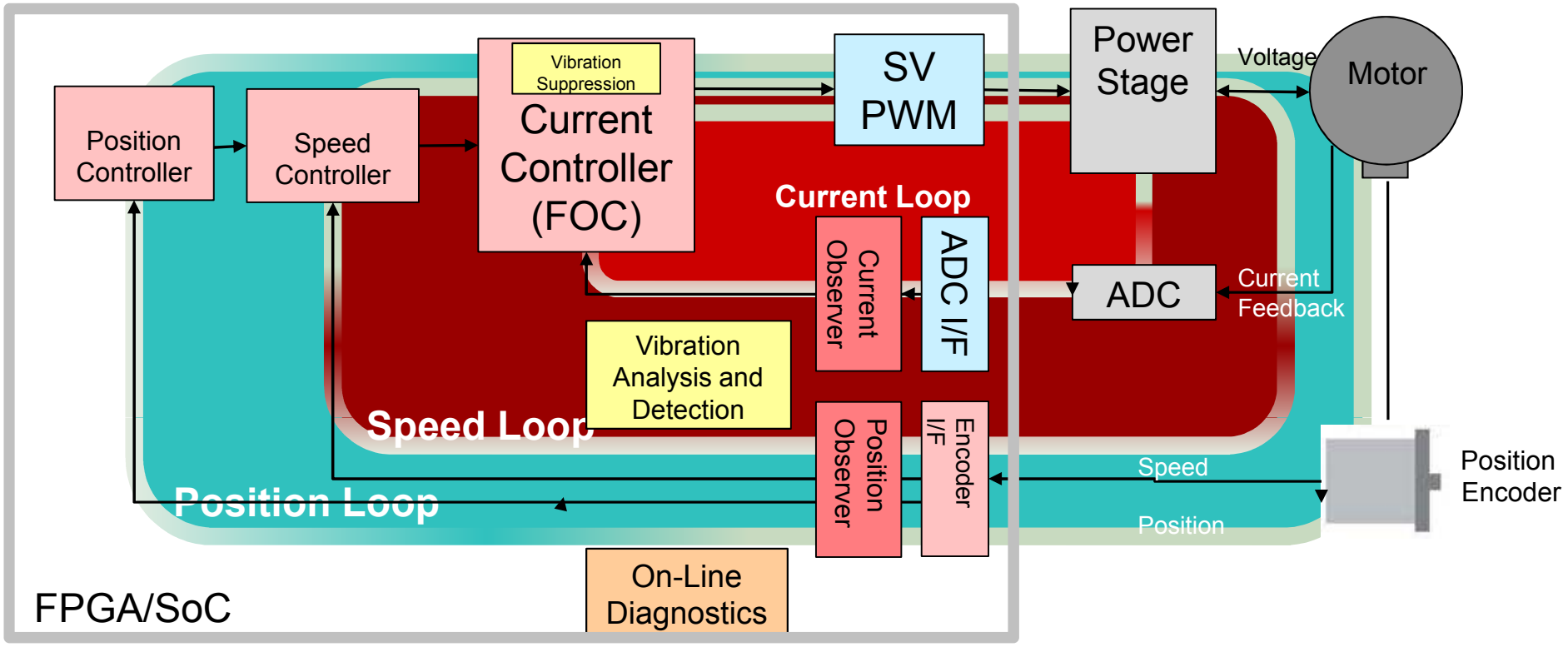
Drive-on-a-Chip Reference Design Overview

- **Integrated Multi-Axis Drive-on-a-Chip on Cyclone FPGA**
  - Software-only and FPGA Accelerated Implementations of multi-axis motor control
  - Motor Control IP Suite
    - FOC Control Loop IP
    - Sigma-delta ADC I/F, PWM, Drive System Monitor
    - Encoder IP (Partners)
  - Interactive Drive-on-a-Chip System Debug Tools



Fast, Parallel Computation – Do Much More in Less Time



Fast, Parallel Computation – Do Much More in Less Time

Current Control

Speed Control

Position Control

Encoder I/F

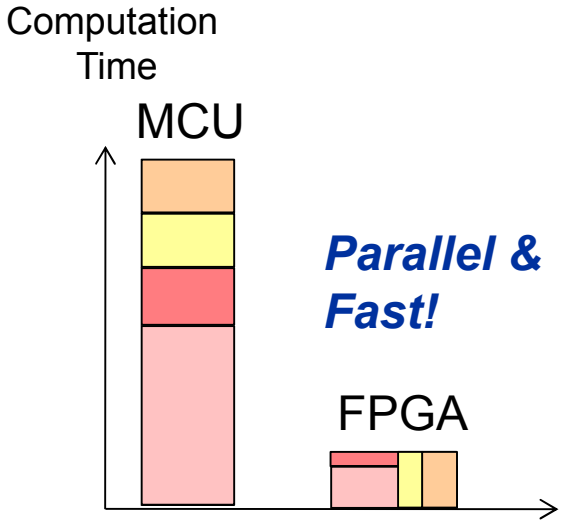
Current Observer

Position Observer

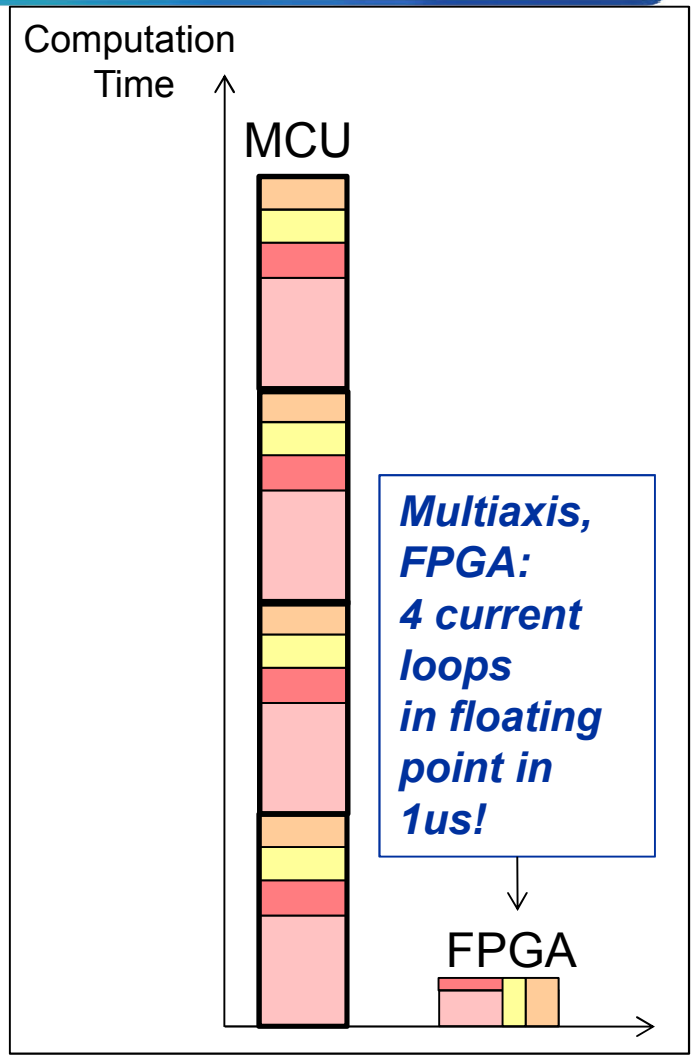
Vibration Suppression

Vibration Analysis and Detection

On-line Diagnostic

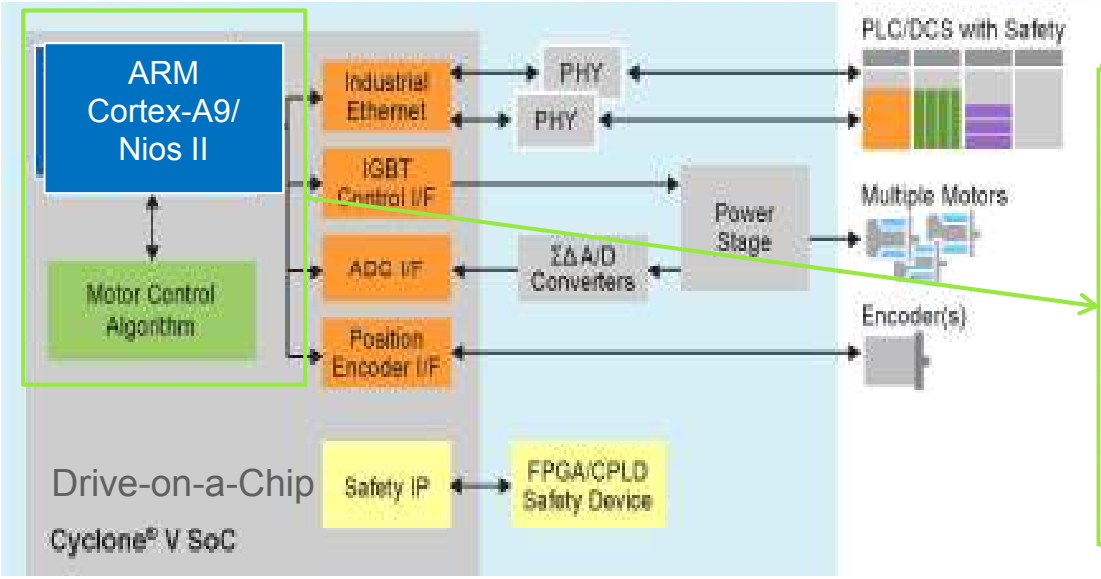


Parallel & Fast!

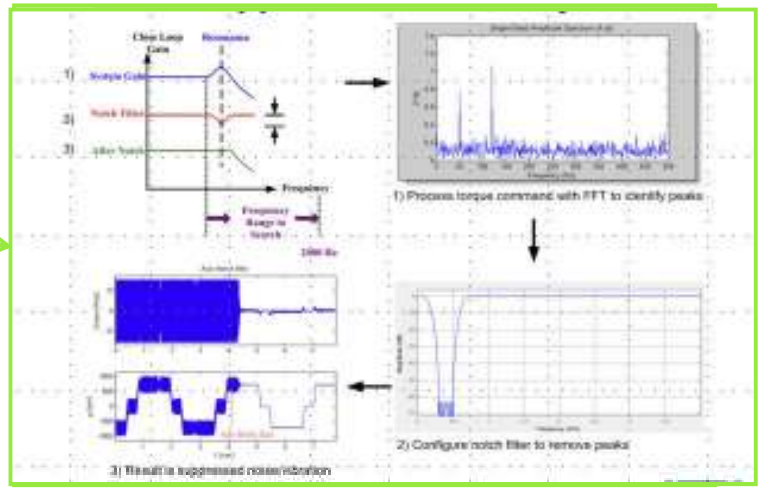


Multiaxis, FPGA: 4 current loops in floating point in 1us!

Altera FPGA Drive-on-a-Chip – Scalable Performance



Multiaxis Field Oriented Control
Vibration Suppression



Requirement	FPGA Benefit
Fast Dynamic Response for **Precise and Efficient** Motor Control	•Ultra-low latency control loops (FOC <1us) – support for **higher switching frequency, optimal sampling in time** •**Efficient Floating Point** •Current Observers **reduce measurement lag** •**High precision/resolution current and position feedback** •Vibration Suppression actively **removes artifacts in sensed current** •Advanced **motor state estimation**
Cost-effective Multiaxis	Time-sharing of FOC DSP coprocessor **– control 2,4,8,16 axes at close to zero latency/resource overhead**
On-Line Diagnostics	**Parallel monitoring and detection** of wider system vibration, stator winding, bearing wear without loading CPU

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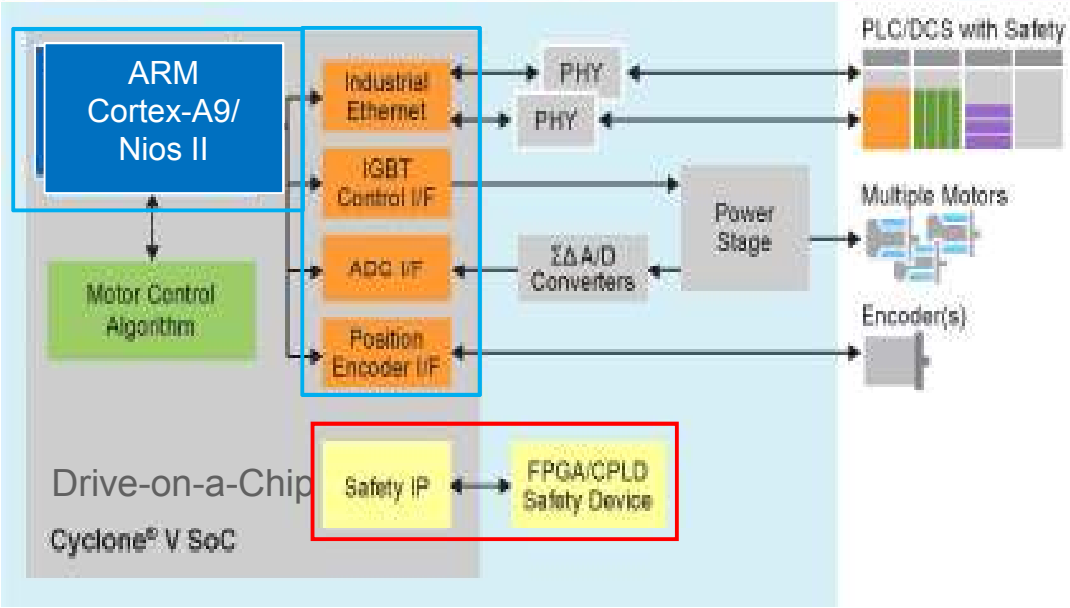
Altera FPGA Drive-on-a-Chip – Flexibility



Flexible fieldbus, encoder, connectivity and power interfaces

EtherCAT · EtherNet/IP · HIPERFACE DSL · SERCOS interface · PROFINET · EnDat · ETHERNET Powerlink · Modbus-IDA · BiSS INTERFACE

Flexible safety and diagnostics

TÜVRheinland® Precisely Right.

Requirement	FPGA Benefit
Multiple Ethernet Protocols	All major protocols, custom switch implementations in FPGA fabric
Varying and evolving power stage interfaces	“Limitless” PWM interface count, 2L/3L inverters, flexibility in ADC support requirements
Varying Encoder Protocols	High Performance Endat, BiSS, Hiperface Master support, configurable number of interfaces/axes, Custom/Proprietary interfaces
Functional Safety	Reduced Cost, T2M & Risk - Functional Safety Data Package, Safe/Non-Safe Partitioning

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Available Hardware Platforms

Altera Multiaxis Motor Control

Falconeye Motor Control

Reference Design	Board Support	Comments
Altera Multi-axis FOC in fixed and floating point	INK CIV, Altera CV + Multiaxis Motor Control Board	MMC Board available for sale end Q1. Est Price: 2000 USD
Altera Single-axis FOC in fixed and floating point	Falconeye Motor Control Kit supporting CIV, CV (Feb'13)	Single-axis variation of multiaxis design. (Price 2500, includes CIV/CV FGPA Board)
EBV/U Cologne Drive Reference Design Single-axis, Nios II floating-point design with custom instructions	Falconeye Motor Control Kit (CIV, CV)	Reference design ships with Falconeye Kit (Price : 1800 EU before shipping)

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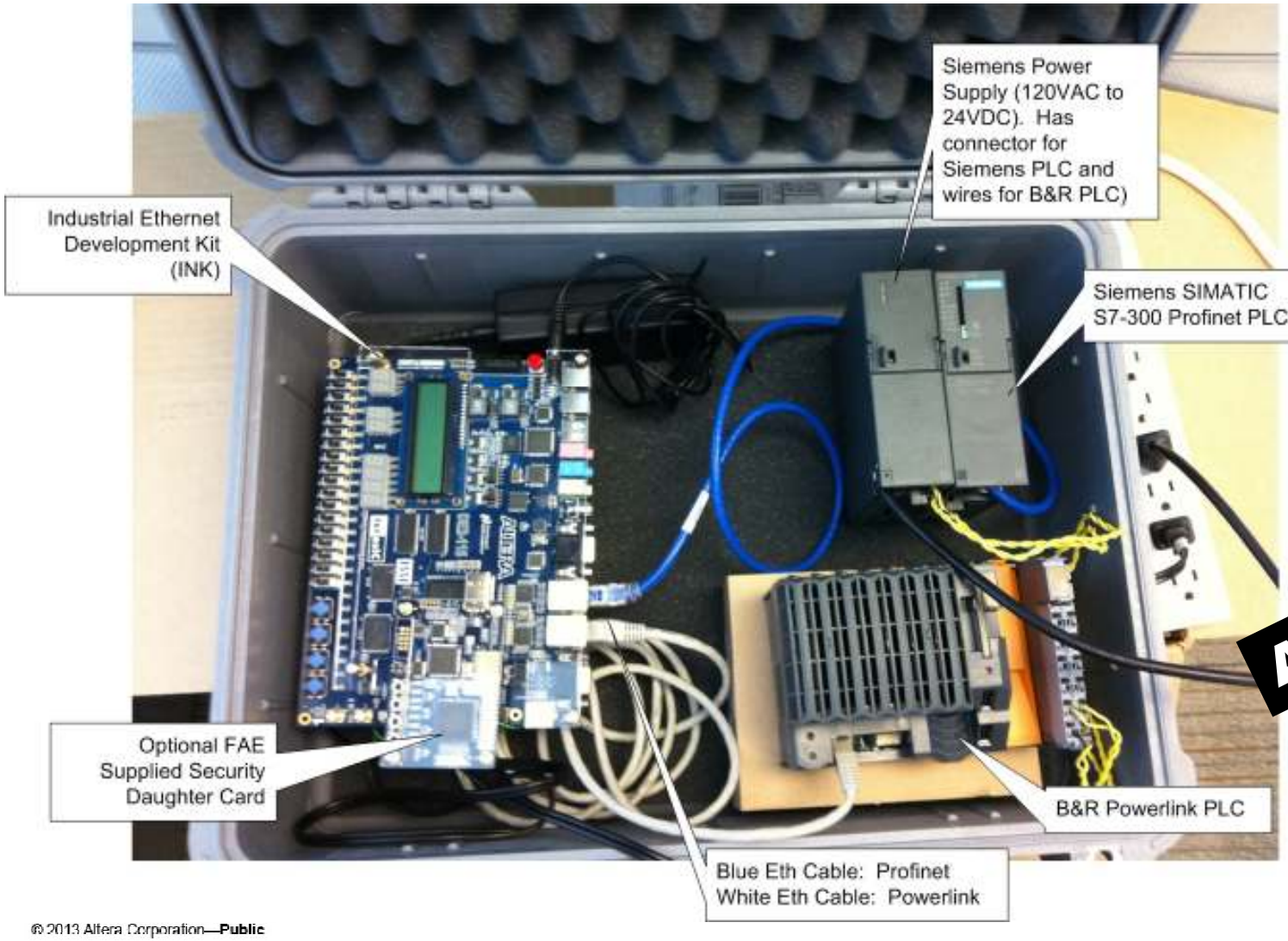
Field Demo Kits – Industrial Ethernet



Available

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Thank You