



# DisplayPort MegaCore

Altera Technology Roadshow 2013



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# Agenda

- **DisplayPort Background**
- **Introducing DisplayPort MegaCore**

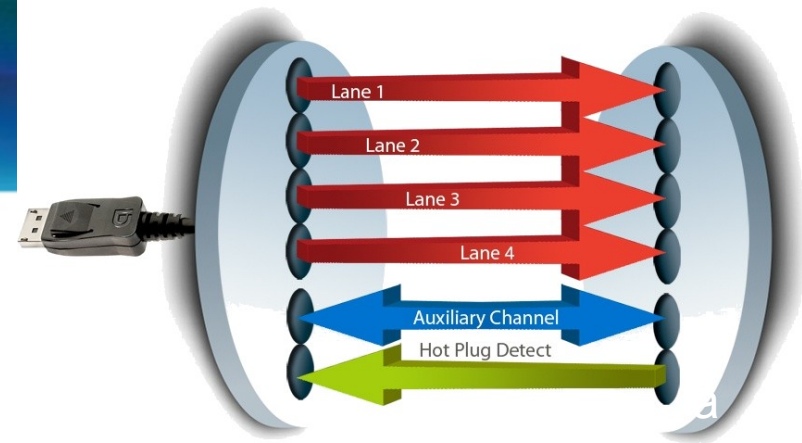
# DisplayPort Background



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# Display Port: What is it?



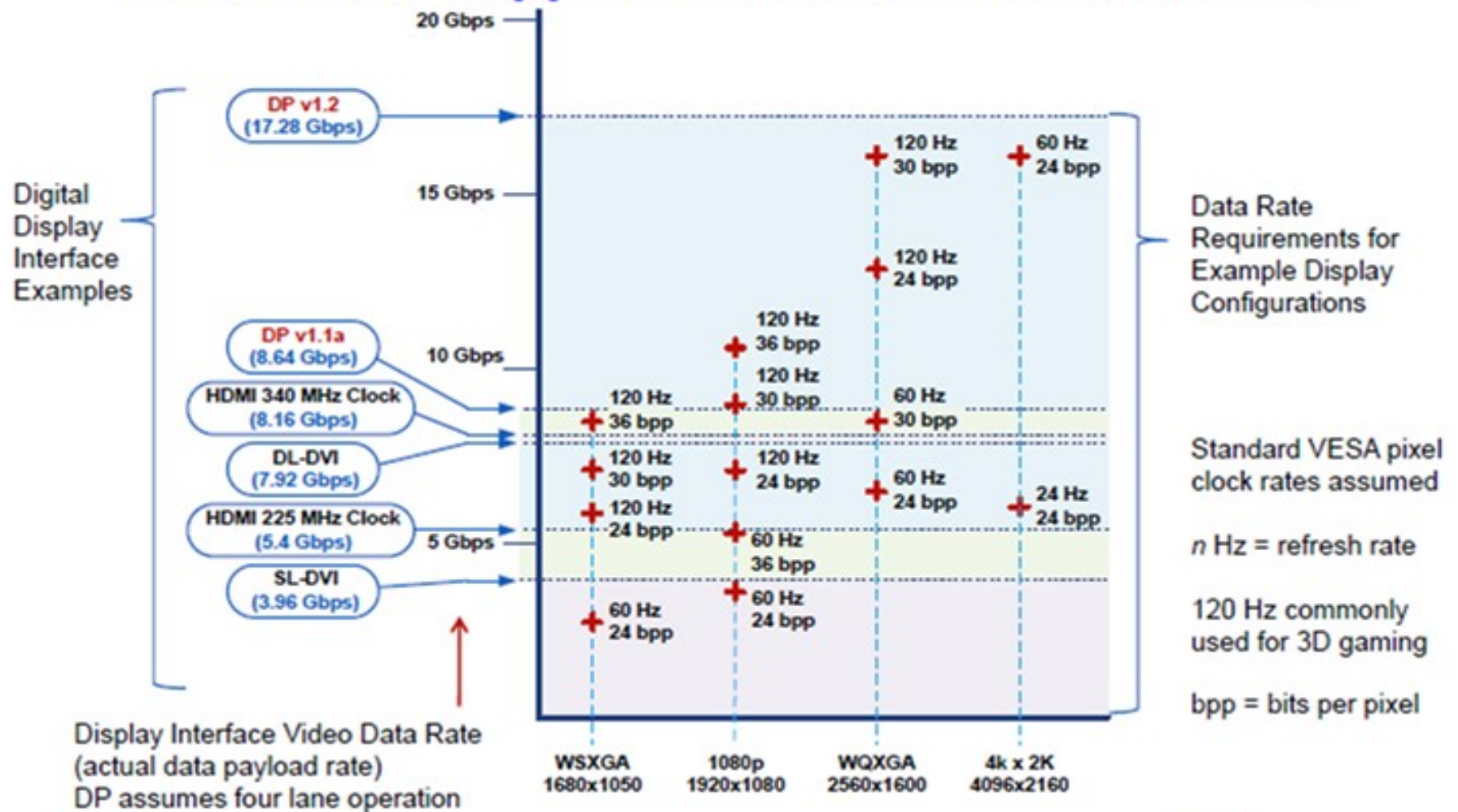
## ■ Next generation video display interface technology

- Scalable Main Link for data
  - 1,2 or 4 Lanes
  - 1.6, 2.7 or 5.4\* Gbps per lane with embedded clock
  - Both Audio and Video streams
- Auxiliary channel for two way communications
  - Link and Device management
- Hot plug detect
  - Used by Sink to announce their presence
  - Used by source to initiate link configuration
- AC coupling and low EMI
- Defined by VESA ( Video Electronics Standards Association)

\*Display port 1.2 (HBR2 – High Bit Rate 2)

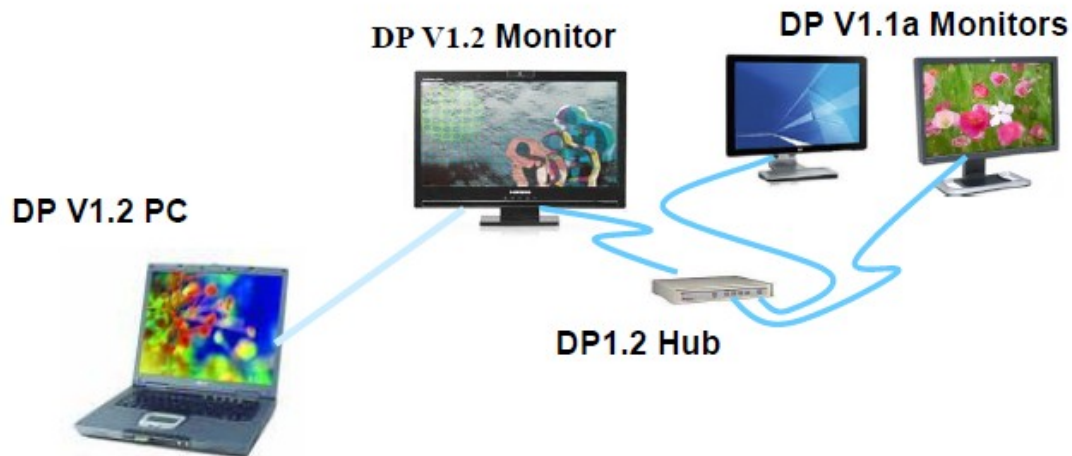
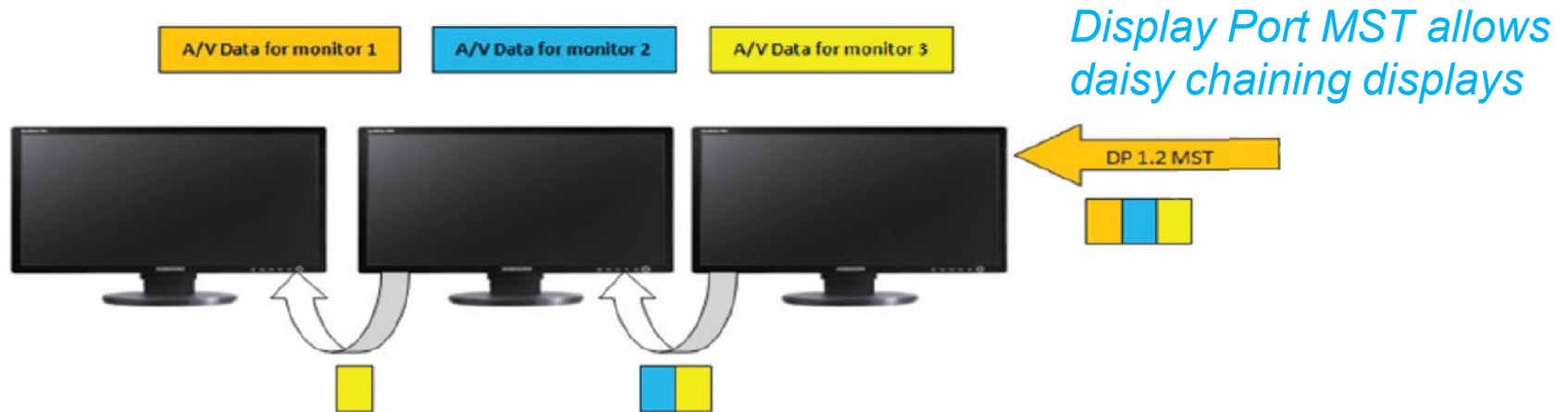
# DisplayPort Physical Layer Overview

## Resolution Support vs. Interface Data Rate





# Display Port v1.2 differentiating features

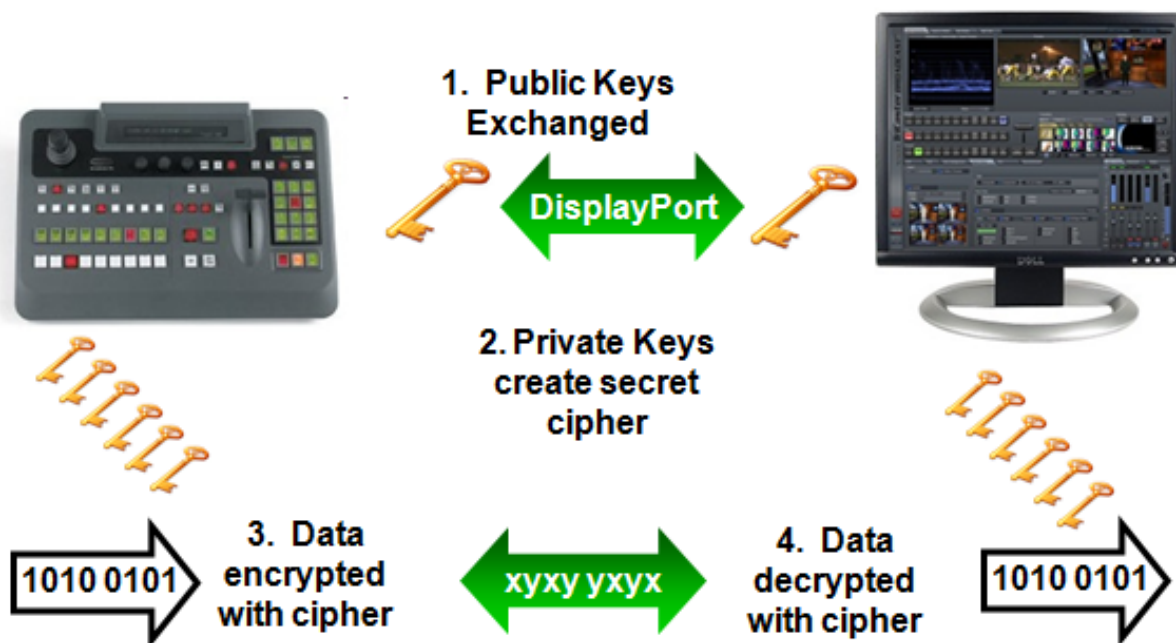


## ■ Real time continuous encryption

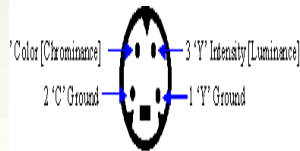
- Constant “key negotiating” takes place between source and destination

## ■ HDCP Implementation

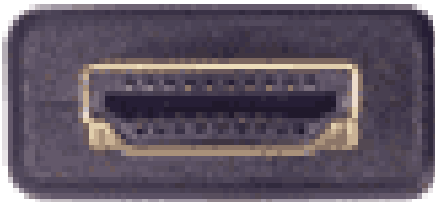
- HDCP license restrictions prevent sharing of source code / implementation on HDCP



# DisplayPort vs HDMI



HDMI



- Video + Audio on same cable
- Full HD, 4k24fps and 3D support
- Popular on consumer devices
- Offers Media content protection

- Users pay royalty
- Controlled by HDMI consortium

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Display Port



- Video + audio
- Full HD, 4k60fps and 3D support
- Appearing newer Laptops/PCs
- Apple big proponent
- Offers Media content protection

- No royalty
- Controlled by VESA

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# DisplayPort Variants

## ■ DP 1.2a vs 1.1a

- DP 1.2a is the current version of the DisplayPort standard
- HBR2 (5.4G) and Multi-Stream (MST) are the most significant additions
- Altera core is 1.2a compliant, but will only support up-to HBR (2.7G) with a Single-Stream (SST)
- HBR2 support for Stratix V coming in 13.0, Arria V in 13.1

## ■ DP++

- DP++ supports driving HDMI sinks with a DP source
- Essentially muxes HDMI source with DP source
- Adapter cable required
- Altera will support when we productize an HDMI MegaCore

## ■ eDP

- Embedded DisplayPort
- Emerging standard based on DisplayPort
- Adds feature extensions useful to closed “embedded” systems
- PSR – panel self refresh

# Introducing DisplayPort MegaCore



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# DisplayPort Value Proposition vs ASSP

## ■ FPGA

- Flexible lane number configuration, color depth, data mapping and video resolutions
- Proven high speed transceiver technology
- Fast adaption of newer DisplayPort features and standards
- Integration with Altera's VIP suite and other IO protocols
- Multiple DisplayPort source / sink devices integration in single FPGA with single or dual mode



## ■ ASSP

- Dual mode not available
- High volume, short lifespan consumer devices
- Fixed link rate, lane count, color depth and video resolution

# MegaCore Packaging - Standard IP deliverables

## ■ Core

- MegaWizard and Qsys support
- Clear text top-level instantiating encrypted Bitec core and XCVR PHY

## ■ Example designs

- Compilation and simulation examples demonstrating correct use of XCVR reconfiguration IP and connection to VIP Clocked Video Input/Output
- HW demo using Qsys to generate a video system with Nios control
- Targeting Stratix V and Arria V FPGA development kits

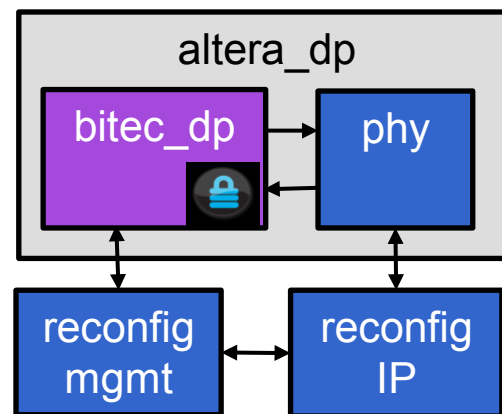
## ■ Software

- Pre-compiled library of source/sink management functions
- Top-level link master example program

## ■ User Guide

# Core Overview

- **Simple clear text Verilog module instantiating Bitec DP core and XCVR PHY IP**
  - Allows users to modify XCVR implementation when using non-standard source/sink packing
- **Bitec DP core is encrypted and called bitec\_dp**
  - All Verilog modules use bitec\_dp as their prefix, which will be visible in Quartus
  - Simplifies integration of Bitec code drops
- **PHY IP uses Native PHY with 20-bit low-latency interface**
  - 40-bit interface required to support 5.4G in Arria V
  - New datapath being developed for 13.1
- **XCVR reconfig IP outside the core**
  - Required because of 28nm HSSI architecture
  - FSM provided to control reconfiguration

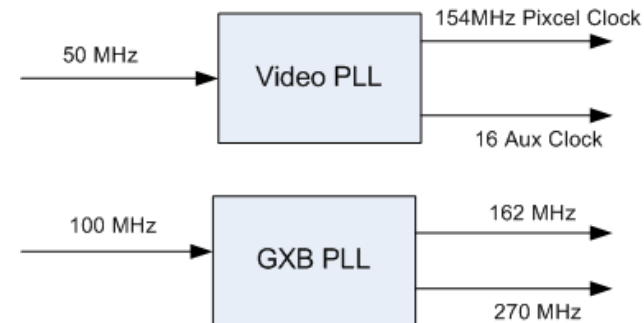




# Clock Requirements

## ■ Video PLL

- 154MHz Pixel clock
  - Clock resource for the video data path
- 16MHz AUX clock
  - Clock resource for AUX channel

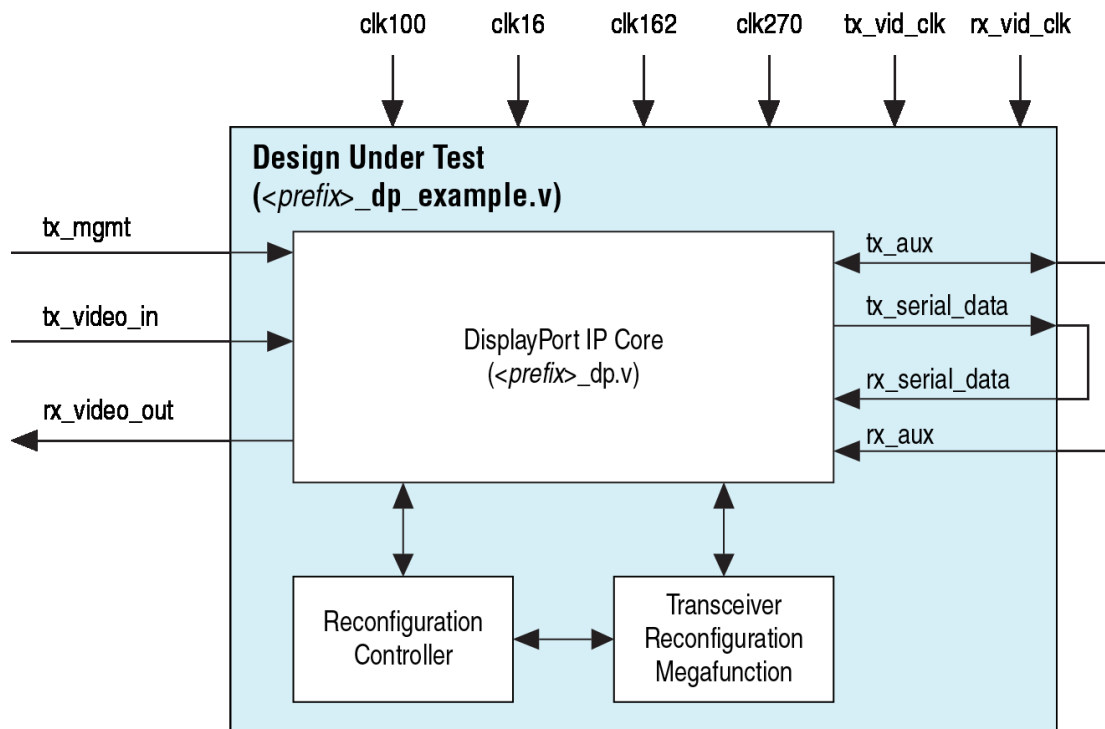


## ■ XCVR PLL

- 162MHz and 270MHz outputs
- Combined as input clock resource for PHY
- Use the reconfiguration block switch between two

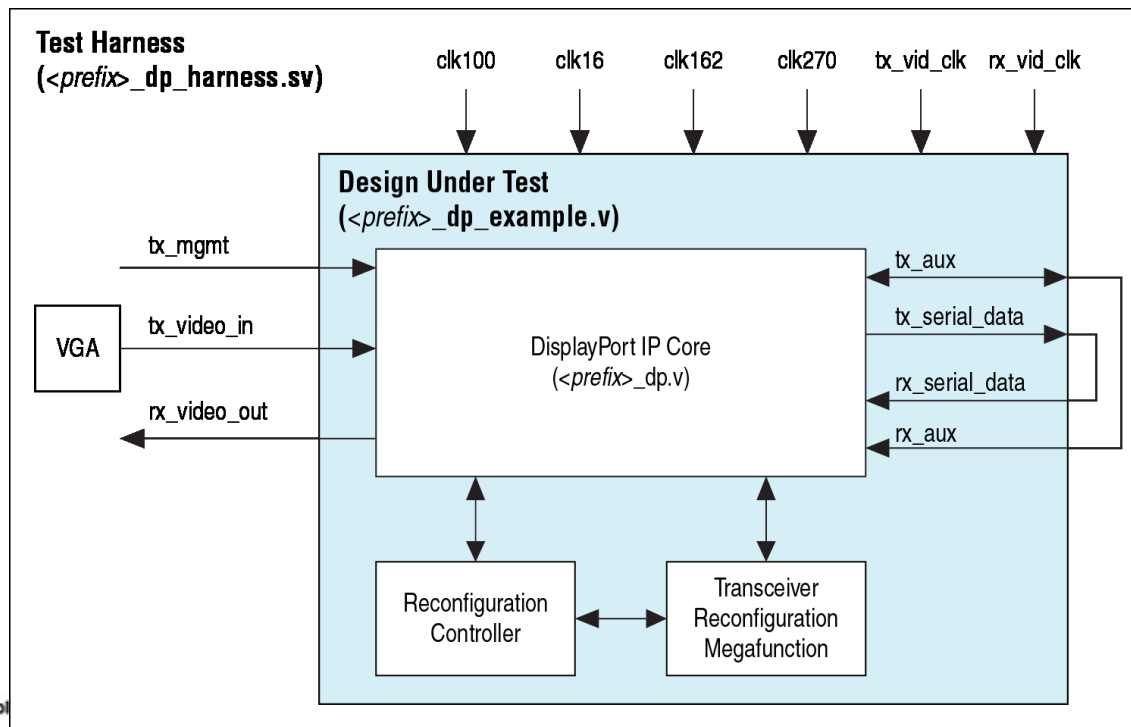
# Compilation Example

- **Minimal Verilog design instantiating:**
  - DisplayPort and XCVR reconfiguration IP
  - A reconfiguration controller implemented as an FSM
- **Useful starting place for understanding reconfiguration requirements**



# Simulation Example

- Simple testbench design built in SystemVerilog
- Simulates XCVR reconfiguration to switch link rates
- Terminates after sending 3 frames of video
- CRC logic in the core checks for correct video



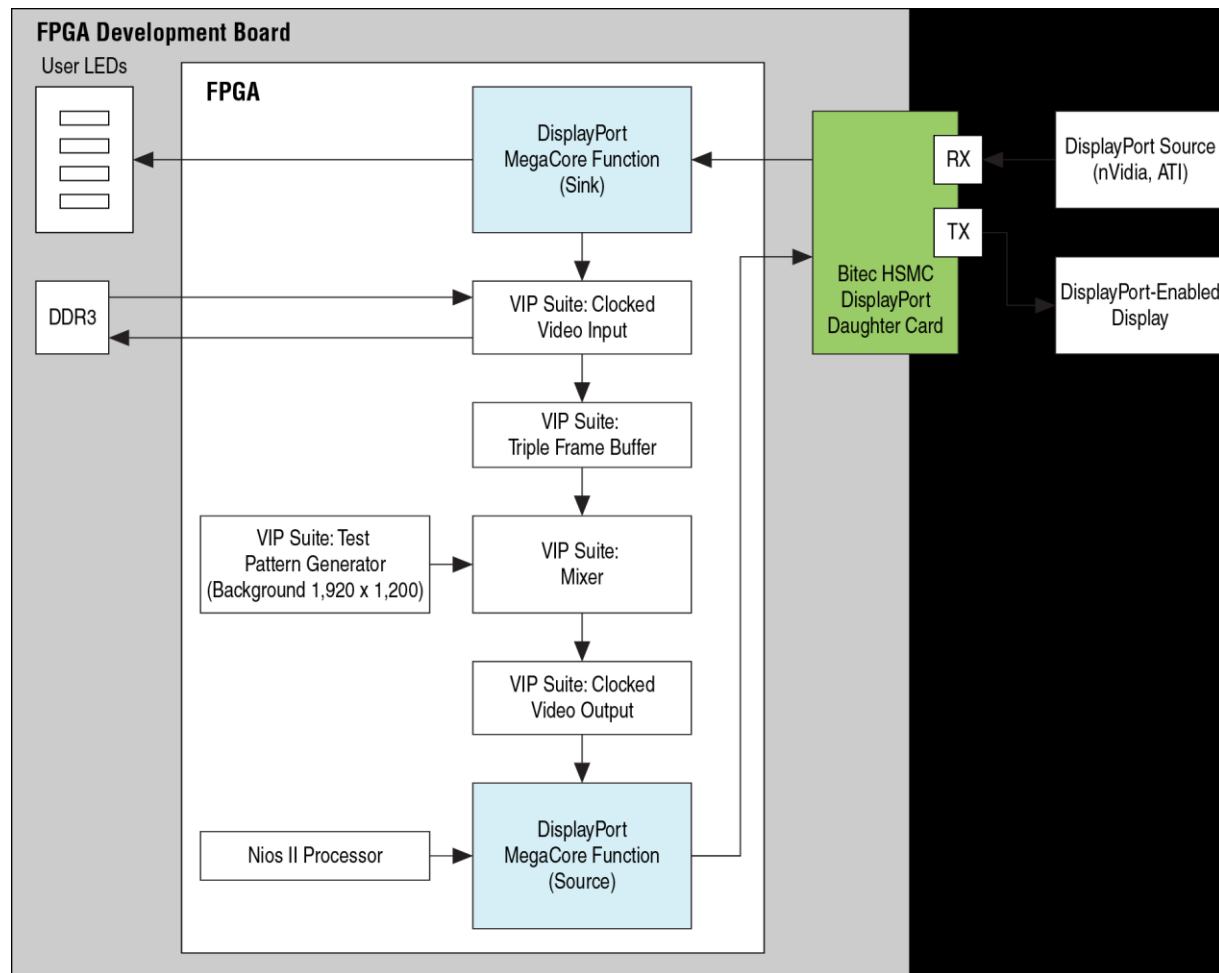
# Hardware Demo

## ■ Purpose:

- Demonstrate core in a realistic system

## ■ Required Hardware:

- SV or AV devkit
- Bitec HSMC card
- DP graphics card
- DP monitor
- DP cables (2)



# Hardware Demo Overview



Test pattern captures user video in “picture-in-picture” mode

## ■ Top-level Verilog

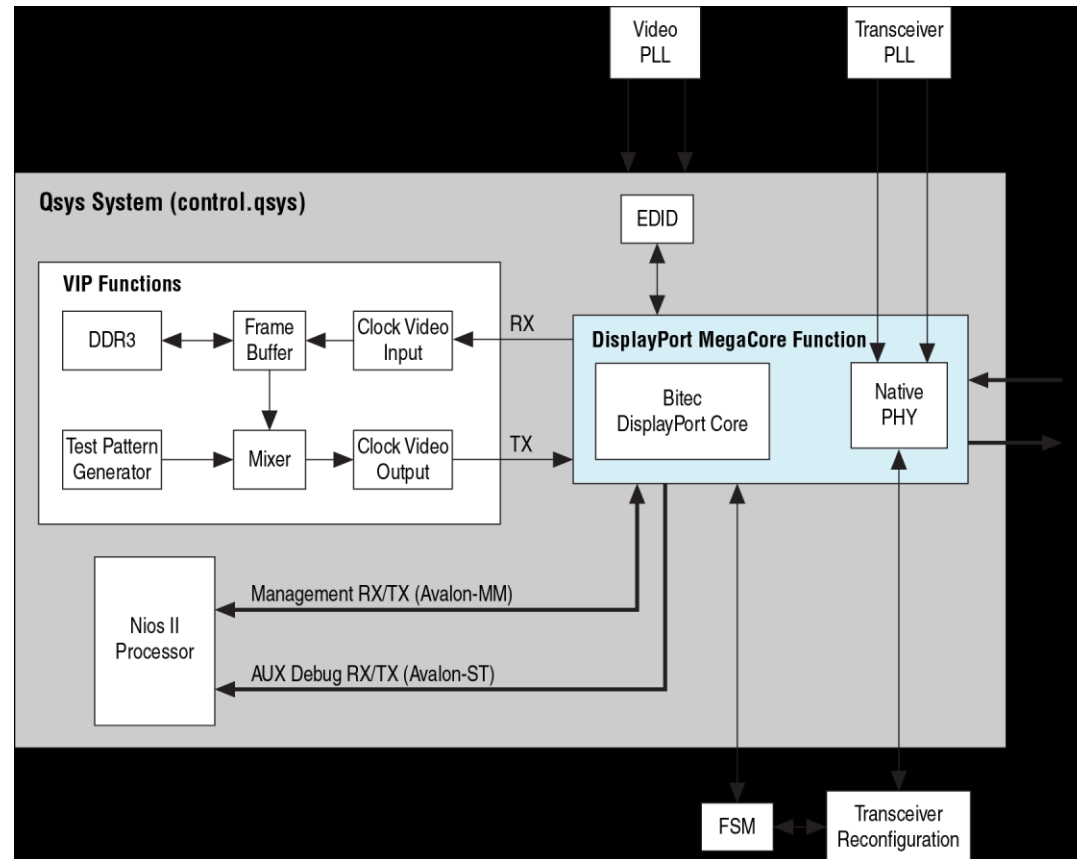
- Instantiate Qsys system, PLLs and reconfig logic

## ■ Qsys generates a video system

- Standard VIP functions
- DDR3 used for frame buffer
- Connect to DP source and sink devices

## ■ Nios provides control and debug

- Implements link master
- Captures AUX traffic
- Displays MSA attributes





# Altera DisplayPort MegaCore Ordering Code / Pricing

## ■ IP Name

- Video Interface – DisplayPort

## ■ Part Number / Price

- IP-DP: \$15,000
- IPR-DP: \$7,500

## ■ IP Description

- DisplayPort Video Interface (up to 5.4 Gbps)

## ■ Video IP Bundle Promotion (Expires Sept 31<sup>st</sup>, 2013)

- 33% to 50% off Video IP bundle with VIP Suite and SDI
- Customer can renew Video IP individually after

# Video IP Bundle

Special price  
until 9/31/2013

## ■ Promotional price

- For customer evaluation and adoption

Special Video IP Bundle	Part Number	Price	Saving	Starts	Expires
VIP Suite + SDI II	<b>IP-VIP-SDI</b>	\$6,000	33%	Now	Sept 31 <sup>st</sup> , 2013
VIP Suite + DisplayPort	<b>IP-VIP-DP</b>	\$10,000	50%	v13.0	Sept 31 <sup>st</sup> , 2013
VIP Suite + SDI II + DisplayPort	<b>IP-VIP-SDI-DP</b>	\$12,000	50%	v13.0	Sept 31 <sup>st</sup> , 2013

***Contact Altera Representative for Video IP Bundle***



# Getting Started in v13.0

- **Request DisplayPort Demo from Altera field**
  - Demo with S5GX / A5GX dev kit using DP example design
  - Demo with A5GX starter kit using UDX 6.1 (Format conversion RD)
- **Download “How to get started” Application Note**
- **Open DisplayPort MegaCore and go through user guide**
  - Altera OpenCore Plus program for free evaluation



# Thank You



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