## Abstraction of Concurrency and Communication in VHDL

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Me	essage passing mechanism (	1)
<ul> <li>Alternative 1: introduce new mechanism</li> <li>– eg, message channel, send &amp; receive operations</li> </ul>		
	<b>channel</b> elevator_call : floor_number; <b>channel</b> elevator_location : floor_number;	
	elevator : process is begin	
	<b>receive</b> calling_floor <b>from</b> elevator_call; <b>send</b> current_floor <b>to</b> elevator_location;	
	end process elevator;	
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