

Miniaturised Microcontroller based Read-out Electronics for Space Applications

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Classification code: ?

Keywords: particle detector, read-out electronics, ASIC, microcontroller

Wordcount: 2515

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Abstract

The Particle Detector Front End (PDFE) ASIC together with a 8052 based microcontroller forms a chip set being developed by the European Space Agency (ESA) for compact low cost scientific energetic particle instrumentation. The architectural system analysis and trade-off has resulted in a chip set well suited for implementation of flexible and highly integrated instruments.

Driving requirements of low noise and power consumption led to the selection of a single configurable analog channel followed by an internal 8-bit ADC. Low mass and volume necessitated for space applications require on-chip integration of supporting functions such as discriminators, independent coincidence event detection and an efficient serial control interface. Further digital processing such as binning, control and monitoring of several PDFEs combined with direct communication to the spacecraft are all realised in the microcontroller, enabling in-flight instrument reconfiguration of an instrument.

1. Introduction

Miniaturisation of scientific instrumentation is required to meet the increasing demands for lowering the cost of space missions. However, the significantly high non-recurring development cost associated with miniaturisation requires that modularity and re-usability be adequately considered. For the specific case of particle detection front-end and back-end electronics, the European Space Agency (ESA) is developing a chip set drastically reducing

size and power consumption without compromising the scientific performance requirements. The set comprises a single-chip particle detector front-end and an 8052-based microcontroller. This activity push toward higher integration in a single Application Specific Integrated Circuit (ASIC) compared to previous ESA particle science ASIC developments [1], [2].

2. Architectural design drivers and trade-off

With the long-standing strong scientific involvement and space hardware contribution from the ESA Space Science Department in Solar Science (e.g. space missions like HEOS, ISEE-3, Ulysses, WIND, SOHO and Equator-S), the energy range from 15 keV to around 1 MeV [Si] is of high importance. To accurately cover the lower energy ranges, the read-out electronics noise must be less than 600-1000 electrons. Another basic requirement is the maximum count rate of 250,000 events per second. It has not been possible, however, to maintain this requirement the largest energy range due to pile-up in the analog chain.

The choice of processing technology is another important aspect. Bipolar technology is generally considered more radiation tolerant and less noisy than CMOS. However, implementing digital functions, lower power consumption and larger industrial availability (with subsequent lower cost) makes CMOS the process of choice. This in turn requires special attention to low noise techniques for mixed mode CMOS design where feed-through

noise from digital circuitry on the same Si substrate as the analog electronics can affect the analog processing seriously.

Keeping in mind the functionality, low total chip-count, low mass and volume of a complete particle detection chain for a space born instrument, the integration of an on-chip ADC is necessary. Keeping the ADC outside the analog chain ASIC would have resulted in a significant increase of the chip-count for synchronisation and generation of various reference voltages. Another architectural consideration is whether to use a high-speed ADC (must be of full flash topology to meet count rate requirement) multiplexing between several analog chains. However, it was found that the advantages in assigning a dedicated ADC to each analog chain (w.r.t. processing synchronisation and predictability, instrument level design flexibility and lower noise due to lower processing speed) by far outweighs the penalty in terms of power consumption. This conclusion is also drawn from lessons learnt in a previous mixed signal ASIC development [3] with a multiplexed ADC that showed poor performance due to noise in the preceding analog memory associated with each channel.

To make the implementation of the front-end ASIC in various instrument designs possible, easy scalability to various particle telescope arrangements was necessary. Hence, a low speed and low noise serial link that is cascadable for several ASICs has been implemented for configuration, control and discriminator settings.

From the other end of a typical space instrument, the interface circuitries for telecommands, data exchange and power supply to a typical satellite bus normally occupy a significant amount of printed circuit board area and hence contributes heavily to the total volume/mass of

an instrument. Integrating some generic serial telecommand and telemetry interfaces for communicating with the spacecraft in the onboard instrument controller was also seen as necessary. By using a single rail +5V supply to the instrument, the power supply circuitry could also be simplified thus reducing the total power consumption.

For the digital processing part, the high speed processing of event data such as coincidence logic and binning need for reasons of low power consumption and noise to be hard-wired but possibly in-flight re-configurable for mission flexibility. This in turn reduces the real-time processing power needed for the instrument microprocessor and an 8-bit microcontroller was selected.

The space radiation environment also makes some special adaptation necessary for protecting the digital electronics against Single Event Effects (SEE) such as Single Event Upsets (SEU) and Latch-Up. Hence, circuitry for Error Detection and Correction (EDAC) was integrated in the microcontroller for RAM access, a watchdog timer and parity checking/majority voting or control registers. The analog circuitry also needs to be sized for various Total Ionising Dose (TID) induced radiation effects such as parasitic CMOS transistor field-oxide leakage and gate oxide threshold voltage shift.

Finally, the resulting quality and reliability of the ASICs must be possible to assure through high-reliability screening and test methods. Hence, taking testability into account early in the design through validation and test vector design, dedicated test logic has also been implemented.

3. Particle Detector Front-End (PDFE)

The low noise particle detector front-end contains two analog charge amplifying chains, one performing the charge amplification, pulse shaping and digitisation while the second one is used for (anti)-coincidence gating. The large dimensions of the input FETs (W/L of 9000/1.7 μm) in combination with the internal 0.5 pF charge integrating capacitor is needed to fulfill the low noise requirement. A 4th-order shaping filter performs the subsequent pulse shaping. After that, pulse polarity (pin-selectable), gain adjustment ($\pm 5\%$, 5-bit) and level shift take place before the internal discriminator (8-bit, max 20% of full range). So far the two parallel chains are identical. The main channel discriminator can then be gated (through a PDFE configuration setting) from the (anti-) coincidence chain before peak detection and Sample and Hold (S/H) stage. The topology of the linear 8-bit ADC is double flash with a primary coarse 4-bit conversion followed by a fine 4-bit conversion with a target for linearity of 0.1 LSB. The choice of the ADC type followed a trade-off between noise, speed, power consumption and accuracy requirement. The PDFE needs an external 4 MHz crystal but the clock oscillator is integrated on-chip for lowest induced clock noise.

Direct TTL outputs from the discriminators are available from both the main- and coincidence channel for possible H/W gating of another PDFE.

To keep the digital noise to a minimum, the PDFE is completely event driven. Out of the approximately 1500 digital gates on-chip, only some 30 flip-flops are continuously active during analog processing while the remaining digital part and ADC are kept in a quiet state until the S/H circuit has latched the analog peak value.

Table 1

The chip is configured and monitored through a low speed synchronous serial interface suitable for cascading, while output data are provided on a parallel interface to be directly connected to e.g. binning PROM or a microprocessor. Output data can either be latched suitable for a data bus or direct output without latching. All digital high current output drivers are implemented with TTL levels and extended rise and fall times. Special effort has been made to minimize the number of external reference voltages needed since this in turn will reduce the total chip count.

An analog input and output capable of driving a short 50-Ohm coax cable are also integrated mainly to allow effective testing of the ADC and analog processing chain, respectively. The analog input could also be used in-flight for reading out other low frequency analog signals such as housekeeping temperature sensors and voltage/current monitors.

Fig. 1, PDFE block diagram

Manufacturing is done in the commercial 0.7 μm mixed signal CMOS process from Alcatel Mietec (B) as part of a Multi Project Wafer. Total ionising dose irradiation exposure of a similar prototype design has indicated an adequate radiation tolerance for the selected process [4]. The chip will be extensively irradiated, followed by electrical characterisation to establish the total dose tolerance and SEE sensitivity. The main concern for the final ASIC

performance remains digital signal feed-through to the analog chain and SEE sensitivity, parameters that do not fully lend themselves to computer simulations but will require extensive testing. For flight parts, an approach with high reliability packaging and screening procedures, together with dedicated analog chip testing and calibration methods is being established.

4. Onboard Microcontroller

For the onboard microcontroller, reusability for future developments was considered of major importance due to long development times of a space project in contrast to rapid changes in semiconductor technologies. Hence, a fully synthesisable core (“soft core” implemented as an Intellectual Property Cell or “IP” cell written in the VHDL hardware description language) is more attractive than a “hard core” where the layout and hence also the implementation technology is less flexible. Other key ingredients in choosing a microcontroller is the instruction set, processing power, chip area and power consumption, multi-sourced IPs, wide user base, cost of the soft core and availability of development tools. The final choice of the 8-bit 8052 microcontroller [5], [6], a twenty year old architecture, maybe not represents the state-of-the-art in modern processing power but was found to be the most suitable compromise between the aforementioned requirements.

The microcontroller will initially be implemented in a Field Programmable Gate Array (FPGA), a solution with several disadvantages (e.g. slower, higher power consumption and larger chip area) compared to a full ASIC implementation but is more cost efficient and flexible for small volumes.

In addition to the standard features in the 8052, such as timers, asynchronous bit serial and parallel interfaces, the microcontroller on-chip and off-chip memory is protected by an on-chip EDAC.

Further, several serial interfaces suitable for interfacing the spacecraft (S/C) and to configure and monitor one or more PDFEs are provided. Each interface is supporting protocols such as RS232/422 and TTC-B-01 [7]. The inclusion of direct S/C interface on-chip was considered essential since the S/C interface in most space instrumentation is based on discrete circuits and tend to occupy significant PCB area. The relatively low communication rate through these serial interfaces should not pose a problem since the data normally should be pre-compressed and packetised by the microcontroller.

For (de-) packetisation of command and data exchanged with the S/C, an on-chip Cyclic-Redundancy-Code (CRC) accelerator is also implemented.

To accommodate various internal instrument interface functions, an area on the FPGA is reserved for externally accessible user defined logic with direct memory access to a 256 bytes internal fast RAM. Due to gate count limitation of the target FPGA, the user defined logic and access to this RAM area is currently configured as either a 16 separate 32-bit counters

(Hamming code protected) or 32 separate 32-bit unprotected counters. The counters are directly accessible by the microprocessor core for further processing (e.g. compression, dump to S/C memory etc.).

The number of interrupts has been expanded compared to the standard 8052 architecture and four external H/W interrupts are available to the user. An internal watchdog monitoring of the microprocessor against unexpected lock-up (e.g. caused by SEU) is available through an internal timer.

In addition to conventional verification methods, the 8052 microcontroller soft-core is being validated in a S/W tool using randomly generated stimuli [8], an efficient method in terms of simulation CPU time while still providing high fault coverage. To ensure interface compatibility between the microcontroller and the PDFE, board level simulation using the combined VHDL models is foreseen.

The microcontroller design is targeted towards a radiation tolerant European process, but will initially be implemented in an FPGA to demonstrate the feasibility of the concept and to validate the functionality.

Table 2

Fig. 2, Microcontroller block diagram

5. Instrument system architecture

The system architecture has been optimised with respect to a low chip count which will reduce board area and mass. This is achieved by as far as possible providing seamless interfaces between the different chips as well as to the spacecraft platform. The compliance with established spacecraft interfaces will reduce the effort associated with spacecraft level assembly, integration and verification. To accommodate varying scenarios, the system architecture allows in-flight reconfiguration and software uploading. The commercial and freeware software development tools that exist for the 8051 family allow significant cost reductions for the development of scientific instruments. Even though a rudimentary run-time S/W core is being developed for the microcontroller, a supporting development of a comprehensive set of low level driver S/W is foreseen.

6. Applications

The chip set is a candidate for several scientific space instrumentation in the field of Solar science and planetary missions including planetary surface landers. It will enable the development of new compact low cost energetic particle spectroscopy instruments and radiation environment monitors. The system architecture has been proposed for several projects and should also be suitable for university developments and micro-satellites where cost is a driving factor. Both the PDFE and the microcontroller could find other applications.

“Drop-in” micro-controllers such as the one developed could also be useful in other onboard applications with low real-time processing power requirements but with programmability and high interface integration such as antenna steering, protocol converters and bus couplers.

7. Acknowledgements

The PDFE is being developed by IMEC (B) and the Katholieke Universiteit Leuven (K.U. Leuven) (B) within the framework of the ESA General Support and Technology Programme. The microcontroller is being developed by ADV Engineering (F) as part of a ESA Telecommunications research programme. Even though the microcontroller is targeted to telecom applications, the suitability for scientific applications is also considered in the detailed design. Both developments are expected to reach completion in autumn 1998.

The preparation of the graphical drawings of J. Heida (ESTEC/SSD) is gratefully acknowledged.

Tables

Table 1

(Caption) PDFE key specifications

Noise:	2.5 keV FWHM (Si) at 0 pF, with a slope of 30 eV (Si)/pF
Conversion gain:	890 mV/MeV (Si)
Detection range:	2.25 MeV (Si)
Digitisation:	event driven internal 8-bit conversion
Counting rate:	maximum 250 000 events/second (lower energy range only)
Power consumption:	approx. 50 mW average at max count rate
Package:	52-pin flat package

Table 2

(Caption) Microcontroller key specifications

Processing power:	> 3 MIPS
Number of logic gates:	approx. 30,000
Power consumption:	approx. 300 mW
Package:	256-pin CQFP for FPGA implementation

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