VHDL to Hardware: A TIREP Success Story

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ABSTRACT

Electronics obsolescence in military systems is one of the most expensive and elusive challenges facing the Department of Defense today. This one issue is costing millions of dollars a year in re-engineering, special orders, volume buys and redesign costs. Development of new techniques, tools and processes for maintenance of legacy systems and integration of new technology in an era of life cycle extension and funding reduction is essential. The Technology Independent Representation of Electronic Products (TIREP) project was funded by the Standard Hardware Acquisition and Reliability Program (SHARP) and the Flexible Computer Integrated Manufacturing (FCIM) program offices to address these repair, reliability, and obsolescence issues in the maintenance of legacy systems. TIREP is a joint effort between the Naval Research Lab (NRL), Washington DC, the Naval Air Warfare Center - Aircraft Division Indianapolis (NAWC-ADI), and the Naval Surface Warfare Center (NSWC) - Crane Division. TIREP has developed a seamless process to cost effectively recreate a form, fit, and function replacement of electronic circuit card assemblies from a digital functional behavioral description such as the Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) along with other related standards.

OBJECTIVES

The DoD has set as one of its goals the movement from physical inventory to design-to-shelf products. The concept of design-to- shelf is that new technology innovation can be developed and virtually prototyped and then held in a low or pre-production state until the need is established. The availability of programmable logic components, such as Programmable Logic Arrays (PLAs) and Field Programmable Gate Arrays (FPGAs), provides an attractive vehicle to implement this methodology. If a standard module based on this technology were available, inventories would only require a small number of different part types that would be programmed for specific functions as needed. Also, commercially available standard components that provide equivalent functionality could be procured at a fraction of the cost of special component buys. This concept has obvious life cycle cost advantages. By modeling the circuit card assemblies using VHDL, a technology independent functional representation can be developed. From this model, a functionally equivalent circuit that is "plug compliant" with the rest of the system can be synthesized into a chosen current technology. The bit-stream to program a programmable logic device can also be generated from VHDL. A major objective of the TIREP project was the development of a VHDL Modeling Guide. The modeling guide was developed to provide a means to standardize the documentation of the business rules and processes required to share information between multiple organizations. The VHDL standard only defines the syntax and semantics of the behavioral or structural information. Variations in implementation or modeling styles can impede successful use of this standard information. TIREP created the modeling guide around industry standards such as VHDL (IEEE Std- 1076), Waveform and Vector Exchange Specification (WAVES, IEEE Std-1029.1), EIA-567A Commercial Component Specification, the VHDL Data Item Description (DID, DI-EGDS-80811), and the VHDL multi value logic system package (IEEE Std-1164). The TIREP VHDL modeling Guide was created to assist organizations in developing transportable, sharable, and platform independent models that can support a product throughout its life cycle. Another important requirement of the TIREP project was the development of a VHDL-to-manufacturing interface. The design or storage of VHDL models without the ability to efficiently transfer the information to the manufacturing facility is non- productive. The functional definition and the physical constraints had to be accurately modeled and then transferred to the production facility. To prove the interface, the TIREP project completed VHDL modeling, production,

and testing of a "format A" Standard Electronic Module (SEM) 12-bit population counter, hereafter referred to as the "FBG module". The Rapid Acquisition of Manufactured Parts (RAMP) Printed Wiring Assembly (PWA) facility at NAWC-ADI was used as the production site for the new design. The TIREP Design-to-Manufacture process is illustrated in Figure 1.

MODELING APPROACH

Navy Standard Electronic Modules (SEM) were used as a conceptual testbed for the TIREP process. Thirteen "SEM-A" modules of medium to high obsolescence risk were chosen for their low complexity and urgent need for replacement parts. The candidate modules were purely digital and range in complexity from 2-input NAND gates to basic functional units such as multiplexers and ALUs. The modules or circuit card assemblies were modeled in accordance with the TIREP VHDL Modeling Guide. The completed models were then exchanged between the three participating activities to test the transportability and platform independence of the TIREP approach. A methodology for redesign was developed and proven by the manufacture and test of the FBG SEM module. The same procedure can be applied to other larger format SEMs and commercial format modules. The TIREP project emphasizes model reuse through the use of industry standards such as VHDL, WAVES, EIA-567A, VHDL-DID, and IEEE-STD-1164 MVL package. By defining a standardized modeling approach, the models can be used again in the future to synthesize new components and subsystems into the current available technology. In order to maintain a technology independent representation of the SEM, the models were developed along the guidelines of EIA-567A. This implementation requires a functional "core" model with electrical, physical, and timing characteristics defined in VHDL packages. These packages are wrapped around the core model and values are passed down from the top "board-level" as generics. Therefore the core model remains purely functional and can be used in the synthesis of subsequent components. The EIA567A standard packages contain definitions of object types to facilitate assigning DC parametrics and timing information. The logic levels are defined in IEEE-STD-1164 and the test bench and test vectors are written as a WAVES dataset. After the VHDL models were written, they were exchanged between the three participating activities for review, simulation, and evaluation. This was done to verify functionality, portability between VHDL toolsets, and to evaluate differences in VHDL modeling approaches. Each model was evaluated using the requirements of the DID and EIA567A. The evaluations were then compared and a "standardized" modeling procedure was agreed upon by the TIREP team.

MANUFACTURING APPROACH

Once the VHDL models were revised to reflect the standard modeling procedure, the "core" model was then used for synthesis to target a new component. The synthesis resulted in one of three implementations: one-for-one replacement of the parts, new technology insertion, or programmable devices. At least three of the SEMs modeled have been targeted to Altera or Xilinx FPGAs and are ready for manufacturing when the need arises for spares. The FBG SEM module was chosen to be the first "proof of concept" module to be manufactured and tested. FBG was chosen because of an immediate need in the fleet. The FBG modeler chose an ATMEL AT27HC641 UV-EPROM as the target technology for the FBG redesign. Then a Pascal program was written to generate the vector file for the WAVES testbench. The vector file was verified using the testbench. Since synthesis tools were not available, as they are in the case of FPGAs, the output operation of the Pascal program was then modified to generate the ASCII hex file to program the EPROM. Once the functionality of the FBG module was captured in the new EPROM, the validated VHDL models, which also contain the physical design information, and a complete parts list for the module were provided to the RAMP facility at NAWC-ADI for manufacturing of the new FBG design. The frame and connector type from the old module was retained in order to provide a form, fit, and function replacement for the old module. A standard convention for VHDL file names and directory structures was also established in order to interface with the RAMP Product Data Translation System (RPTS). RAMP RPTS can extract information from the EIA567A physical view VHDL package to create the necessary board layout and 3D models for the manufacturing floor. As a result, five new FBG modules were manufactured using the ATMEL EPROM.

TEST AND EVALUATION

After the new FBG modules were manufactured, they were evaluated for conformance to the electrical requirements of the original FBG module [1]. Parameters that were tested include input current, output short circuit current, power supply current, output voltage, propagation delays, transition times and a functional test. The evaluation process was performed at the Naval Surface Warfare Center, Crane Division's Module Test Branch. When tested, the functional behavior of the new FBG module was equivalent to the original FBG module; however, there were numerous variations when evaluating the DC parametrics. For example, the high-level input and

output short circuit currents were greater than that of the original hardware. On the other hand, the power supply current and transition times were less than that of the original hardware, but the propagation delays met the requirements of the original hardware. These variations can be expected when upgrading technologies as a result of component obsolescence. The original FBG module consisted of TTL components, while the new FBG consists of a single CMOS device with pull-up resistors on each input. To determine if the parametric variations would limit interchangeability of the new FBG design, a new FGB module was placed in an actual system to see how it would perform. Interchangeability tests concluded that the new FBG module was faster and showed higher noise immunity than the original FBG design, and met or exceeded all system performance requirements [2].

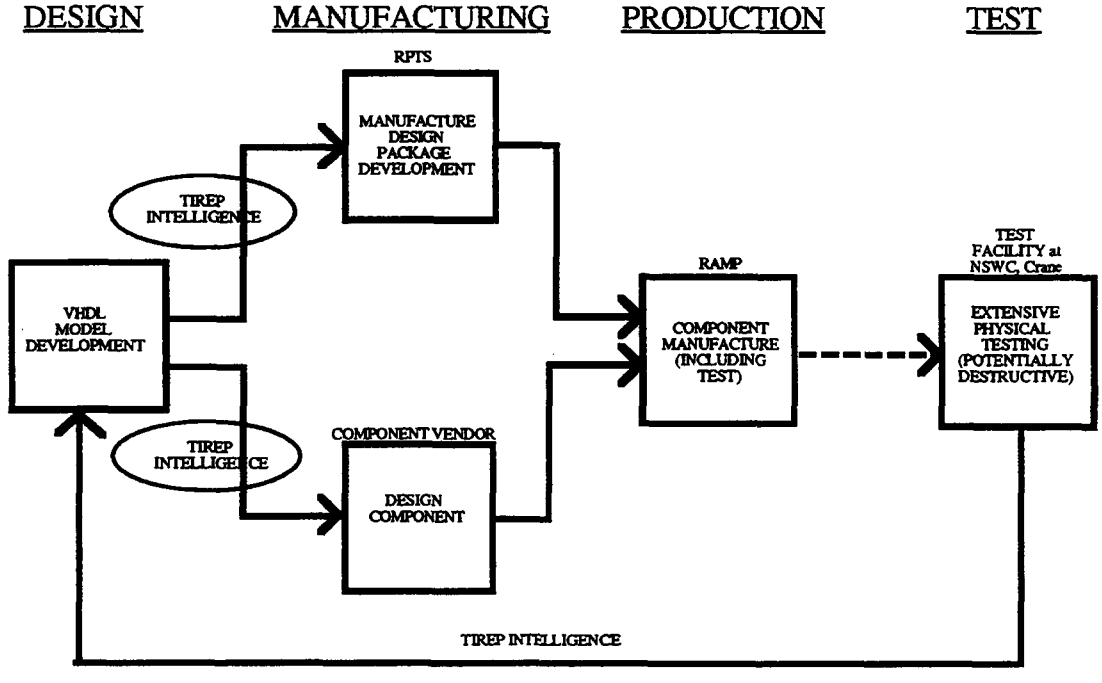
CONCLUSION

TIREP was established to address the costly issue of component obsolescence in military systems. By using industry standards such as VHDL and WAVES in the redesign of electronic circuit card assemblies we not only make full use of the Computer Aided Engineering (CAE) tools that are available today, but we also address the problems of future obsolescence. The efforts of TIREP in developing a set of business rules and processes with which to represent "standardized" behavioral and structural information and develop a design-to-manufacture interface has passed one successful milestone in the redesign of the FBG module. With the interfaces that exist between VHDL and PLAs, PLDs, and FPGAs, systems can be redesigned with greater part redundancy, resulting in inventories with a smaller number of part types. With the shift to programmable logic, component consolidation in systems can be accomplished to greatly reduce redesign-for-obsolescence costs, as well as reduce system failure rates as the number of fallible components decreases.

REFERENCES

[1] "Military Specification. Modules, Standard Electronic. Adder, Discrete-Sum, Digital, Key Code FBG." MIL-M- 28787/175.

[2] Little, Keith F. Memorandum to D. Dunnell, 3 March 1995.



Summary of Design-to-Manufacture Process for TIREP

Figure 1