ASIC 120: Digital Systems and Standard-Cell ASIC Design

Term: **Winter 2006**
Lecture Room: **RCH 309**
Instructor: **Jeff Wentworth,**
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Course website: **www.asic.uwaterloo.ca (under the Resources tab)**

Course Summary:
These lectures will start by covering the basics of digital circuits, and will progress quickly through more advanced digital design, FPGAs, practical implementation and debugging techniques. The idea of these tutorials is not to go line by line through code, nor fill blackboards with lots of proofs and mathematical equations. We aim to provide a comprehensive grounding in digital systems design that goes above and beyond, but is complementary to, the fundamentals you will learn in courses like ECE 223, 222, 324 and 427.

Lecture slides will be posted to the website. Lectures will be recorded and available for download in MP3 format.

The tutorials are free, open to anyone who's interested, and there's no obligation to attend future tutorials. Invite your friends!

Course Outline:

LECTURE 1: INTRODUCTION TO DIGITAL CIRCUITS
When: Wed, Jan 25, 17:30 - 19:00
Where: RCH 309
Summary:
- digital design and its relation to ASICs
- overview of combinational and sequential systems and why they're useful
- logic gates: NOT, AND, NAND, OR, NOR, XOR, XNOR
- basic combinational structures: mux, half adder, full adder
- sequential structures: flip flops and state machines
- HDLs and why they're useful

The remaining tutorial topics are tentative and may be customized to the students demands. Dates and times to be decided, but a tutorial or lab will be held roughly every week.

LECTURE 2: INTRODUCTION TO VHDL
Summary:
- covering again most of what was taught in Tutorial 1, but relating it to VHDL
- the idea is to separate VHDL from traditional programming languages like C and Java by showing that the thought process involved in digital design is fundamentally different

LECTURE 3: INTERMEDIATE VHDL 1
- loops
- std_logic_1164 signal levels
- numeric data types
- attributes
- modular VHDL

LECTURE 4: INTERMEDIATE VHDL 2
- more on data types
- replicating hardware: if-generate, for-generate, loops
- test benches
- VHDL 1987 vs. 1993 vs. 2000

LECTURE 5: DIGITAL SYSTEMS CONCEPTS
- the FPGA: LEs, buffers and routing, other resources
- bus interfaces
- register files
- FPGA hardware features in more detail: clocks, memories, memory interfaces
- soft- and hard-processors in FPGAs

LECTURE 6: PRACTICAL DIGITAL DESIGN
- software tools: Quartus, ISE, NC-VHDL (ideally, I will demonstrate them all, with focus on one of them)
- hardware tools: logic probe, oscilloscope, logic analyzer (not to be demonstrated, but discussed with pictures)
- putting these together in board-level digital design
- from VHDL to an ASIC

Labs:
Lectures will be complemented by practical exercises held in one of the on-campus labs, using Altera FPGA development boards. The labs will focus on aspects of digital design presented in prior lectures, but with scope broad enough to allow students to explore more on their own.

Text Book:
None.

Reference Material:
Will be provided during the course.