Sequential Systems

- A **combinational system** is a system whose **outputs** depends only upon its **current inputs**.
- A **sequential system** is a system whose **outputs** depends on the **current inputs** and the system's **current state**.
- All systems we have looked at to date have been **combinational** systems.

Flip-Flops/ Latches

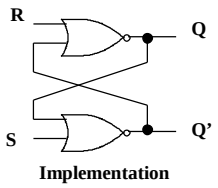
- Latches and Flip-Flops are devices that can have two internal states (0,1)
- The output of a latch or a Flip-Flop (FF) is dependent upon its **CURRENT STATE** and **CURRENT INPUTS**.
- Latches and FFs are the simplest examples of sequential systems.

Set/ Reset Nor Latch (SR Nor Latch)

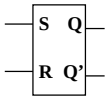
S	R	Ps	Ns
L	L	Q	Q
L	H	X	L
H	L	X	H
H	H	X	-

Present State / Next State

S	R	Ps	Ns
0	0	Q	Q
0	1	X	0
1	0	X	1
1	1	X	-

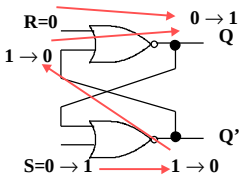


Implementation

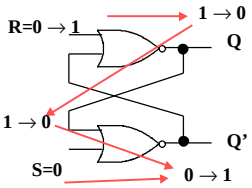


Symbol inputs,outputs high true.

SR latch Operation



SET operation



RESET operation

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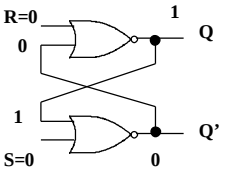
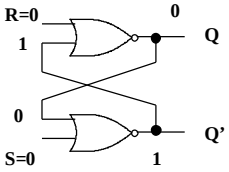
SR latch Operation (cont)



Stable when S=R=0, Q=1



Stable when S=R=0, Q'=1

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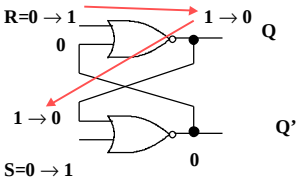
What about S=R=1? (Set,Reset both true?)



Assume that S, R both transition to 1 simultaneously.

Q becomes '0', but Q' remains '0'! Outputs are no longer complements of each other.

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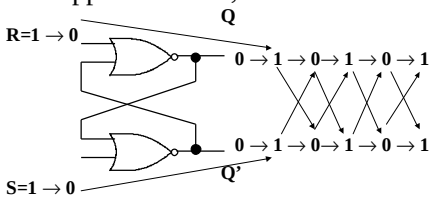
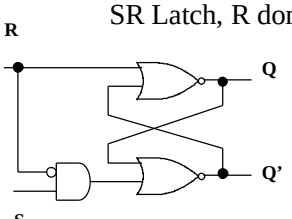
What happens when S,R return to 0?



Oscillation occurs is S,R return to 0 simultaneously! At some point the system will settle into a stable condition. The bottom line is that S=R=1 is an illegal input condition (or design the SR latch such that one input is DOMINANT).

SR Latch, R dominant



S	R	Ps	Ns
0	0	Q	Q
0	1	X	0
1	0	X	1
1	1	X	0

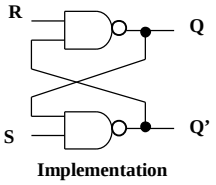
When S=R=1, then acts as a RESET (R is dominant)

Set/ Reset Nand Latch (SR Nand Latch)

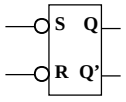
S	R	Ps	Ns
H	H	Q	Q
H	L	X	L
L	H	X	H
L	L	X	-

Present State / Next State

S	R	Ps	Ns
0	0	Q	Q
0	1	X	0
1	0	X	1
1	1	X	-

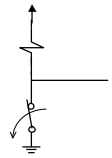


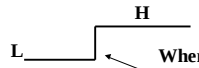
Implementation



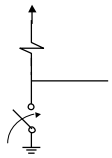
Symbol inputs low true, outputs high true

Switch Bounce



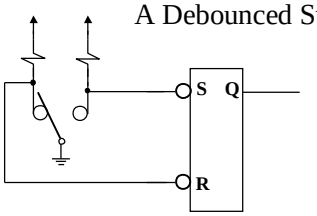


When switch opens, clean transistion from Low to High



When switch closes, mechanical bounces can causes pulses on output for several milliseconds before finally stabilizing at LOW.

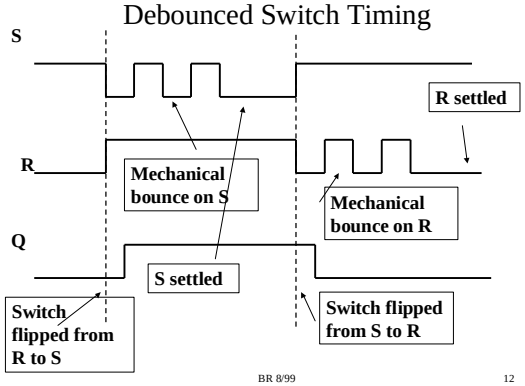
A Debounced Switch



When switch is in R position, Q is low.
When switch is in S position, Q is high.

When switch is flipped, mechanical bounce occurs on either the S or R terminal. SR Latch prevents bounce from being seen on Q output.

Debounced Switch Timing



Terminology

- **A *bistable memory device* is the generic term for the elements we are studying**
- **Can use the term latch or flip-flop to refer to these devices**
  - **latch: bistable memory device with level sensitive triggering (no clock)**
  - **flip-flop: bistable memory device with edge-triggering (with clock)**
- **Warning: Your author (Roth) uses the terminology Flip-Flop and Clocked Flip-Flop instead of latch and Flip-Flop**
  - **latch, flip-flop more standard**

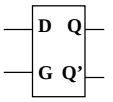
D-Latch (Data Latch)

G	D	Ps	Ns
0	X	Q	Q
1	0	X	0
1	1	X	1
1→0	D	1	D

When G=0, retain old value

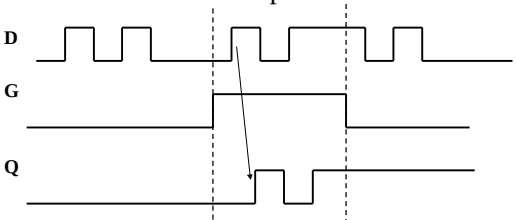
When G=1, Q follows D (transparent mode)

When G=1→0 (falling edge), latch D value



D is the Data input
G is the Gate input

D-Latch Operation

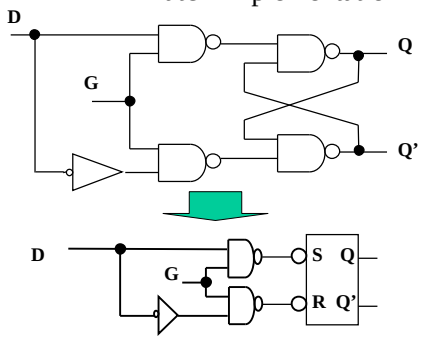


G is low, D has no effect on Q

G is high, Q follows D (transparent mode)

G is low, Q retains D value when G went 1→ 0

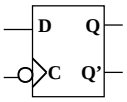
D-Latch Implementation



Data Flip-Flop (DFF, falling edge triggered)

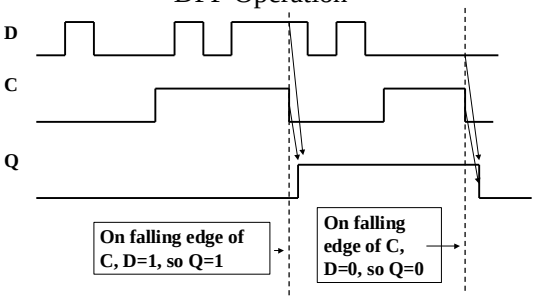
C	D	Ps	Ns
0	X	Q	Q
1	X	Q	Q
1→0	D	X	D

Only time DFF changes state is on a CLOCK EDGE. This DFF is falling edge triggered. Changes state to whatever the D value is.

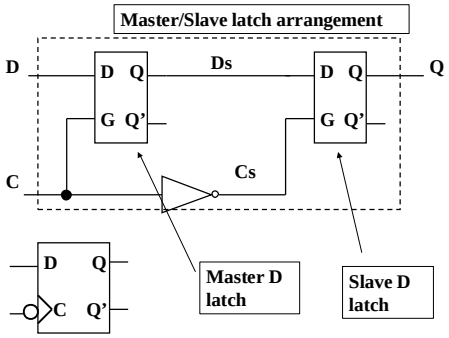


C is the clock input. D input is only sampled at a clock edge.

DFF Operation



DFF Implementation (falling edge triggered)



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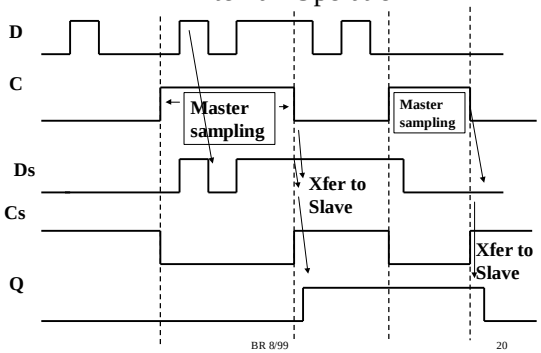
DFF Internal Operation



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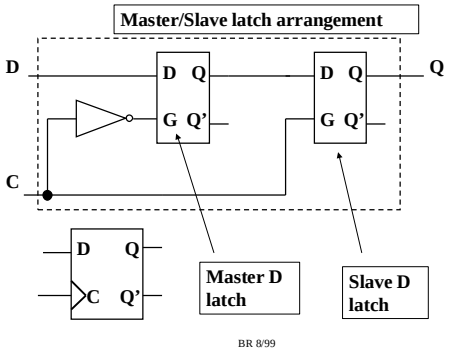
DFF Implementation (rising edge triggered)



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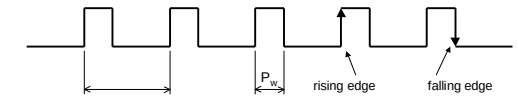
A Clock Waveform



voltage

time

τ - period (in seconds)

P_w - pulse width (in seconds)

f - frequency pulse width (in Hertz)

$f = 1/\tau$

duty cycle - ratio of pulse width to period (in %)

duty cycle = P_w / τ

millisecond (ms) 10^{-3}	Kilohertz (KHz) 10^{3}
microsecond (µs) 10^{-6}	Megahertz (MHz) 10^{6}
nanosecond (ns) 10^{-9}	Gigahertz (GHz) 10^{9}

Slide by Prof Mitch Thorton

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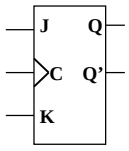
JK Flip-Flop (rising edge triggered)

C	J	K	Ps	Ns	
0	X	X	Q	Q	Retain State
1	X	X	Q	Q	
0→1	0	0	Q	Q	Synchronous Reset
0→1	0	1	X	0	Synchronous Set
0→1	1	0	X	1	
0→1	1	1	Q	Q'	Synchronous Toggle



C is the clock input. J,K inputs are only sampled at a clock edge.

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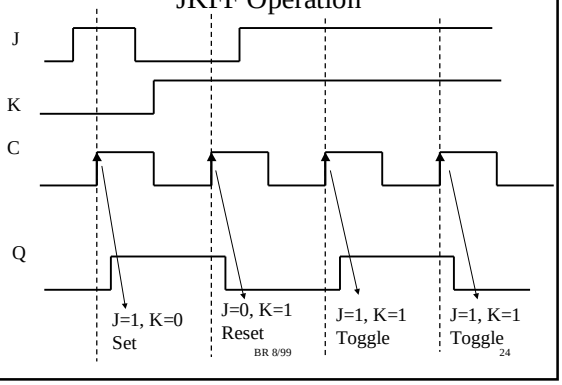
JKFF Operation



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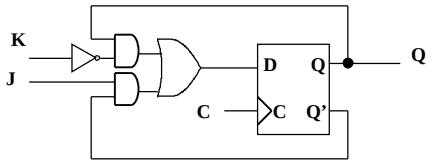
JKFF Implementation



This is a rising edge triggered JK FF. Just substitute a falling edge triggered DFF to make a falling edge triggered JKFF.

We will derive this implementation at a later date.

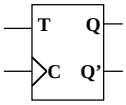
Togggle Flip-Flop (rising edge triggered)

C	T	Ps	Ns
0	X	Q	Q
1	X	Q	Q
0→1	0	Q	Q
0→1	1	Q	Q'

Retain State

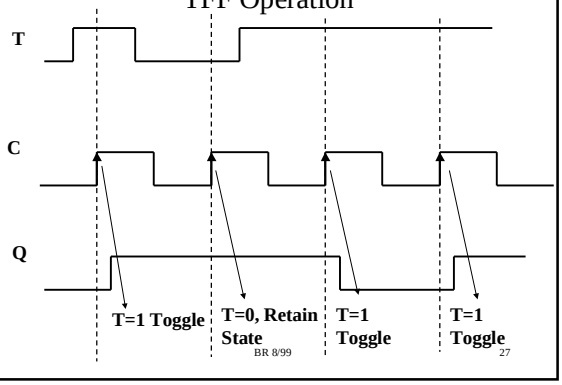
Synchronous Toggle

TFF

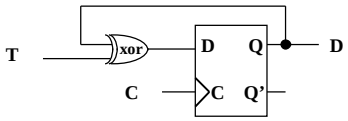


C is the clock input. T input only sampled at a clock edge.

TFF Operation



TFF Implementation



We will derive this implementation at a later date.

What do you have to know?

- **Definition of a sequential system**
- **SR Nand latch, SR Nor latch, D latch, DFF, JKFF, TFF**
  - **Operation all of the above**
- **Implementation of SR Nand, SR Nor, D latch, DFF**
- **Switch Debouncing**
- **Clock waveform characteristics**