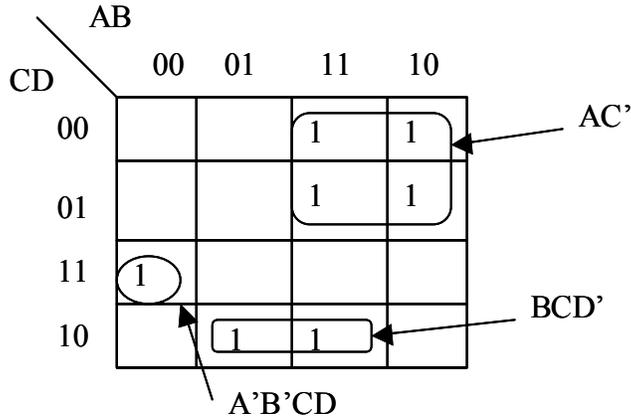


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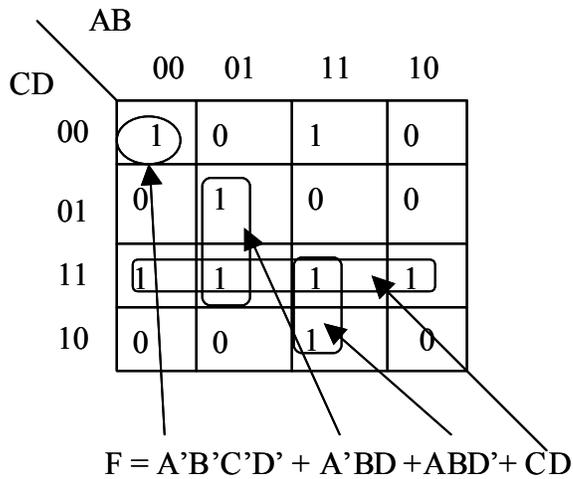
Work all problems.

1. (6 pts) Plot the following function on a K-Map.

$$F(A,B,C,D) = A'B'CD + AC' + BCD'$$



2. (6 pts) Minimize the following K-map to produce a minimal SOP form.



3. (6 pts) Simplify the following K-map to get a **minimal** POS form.

		AB			
		00	01	11	10
CD	00	1	0	0	1
	01	0	0	0	1
	11	0	1	0	0
	10	1	1	0	0

$$F' = A'B'D + BC' + AC$$

$$F = (A+B+D')(B'+C)(A'+C')$$

4. (6 pts) On the following map, identify the following (give the product term) for a minimal SOP equation:

- a. ESSENTIAL Prime Implicant $C'D$ or AC
- b. NON-ESSENTIAL Prime Implicant. AD

Remember that a PI cannot be combined with another group, and a non-essential PI does not have to be included in the minimal equation. AD is a non-essential PI because all of its '1's are covered by other PI groupings.

		AB				
		00	01	11	10	
CD	00	0	0	0	0	Essential PI: $C'D$
	01	1	1	1	1	Non-Essential PI: AD
	11	0	0	1	1	
	10	0	0	1	1	Essential PI: AC

5. (6 pts) I would like to implement the functions 'F', 'G' below in one or more memory devices. Note that F, G share some variables (inputs 'A', 'B' are common to both F, G).

$$F(A,B,C) = AB + CA + CB$$

$$G(A,B, D, E) = A + B + D'E'$$

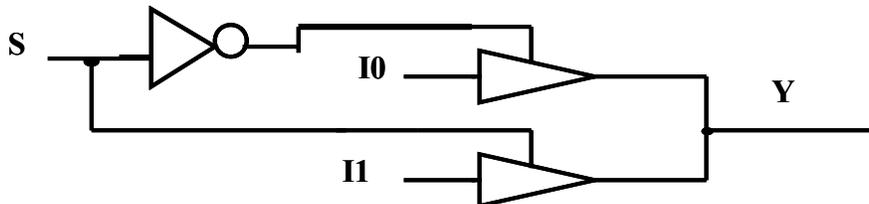
a. What sized memory (K x M) would be needed to implement both F and G in ONE MEMORY chip?
 32 x 2 (2⁵ x 2) --- There are 5 common variables, 2 outputs.

b. What sized memory (KxM) would be needed to implement only equation 'F'?
 8 x 1 (2³ x 1) There are 3 variables, 1 output.

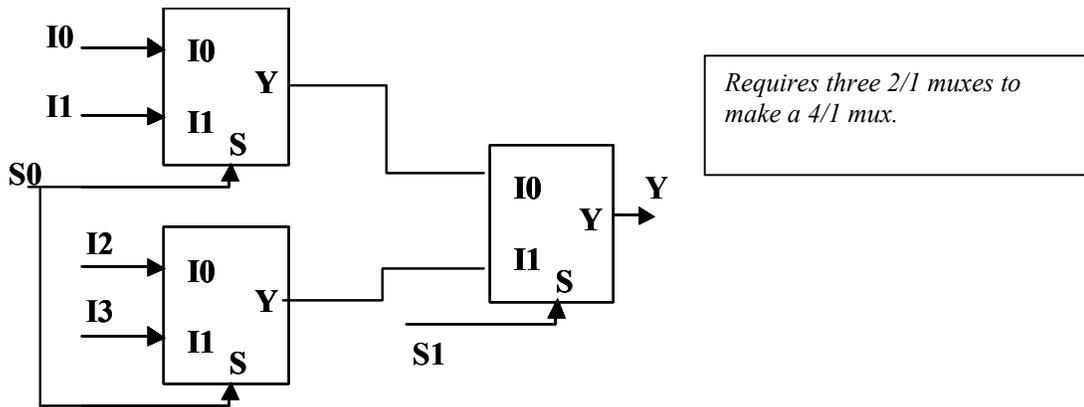
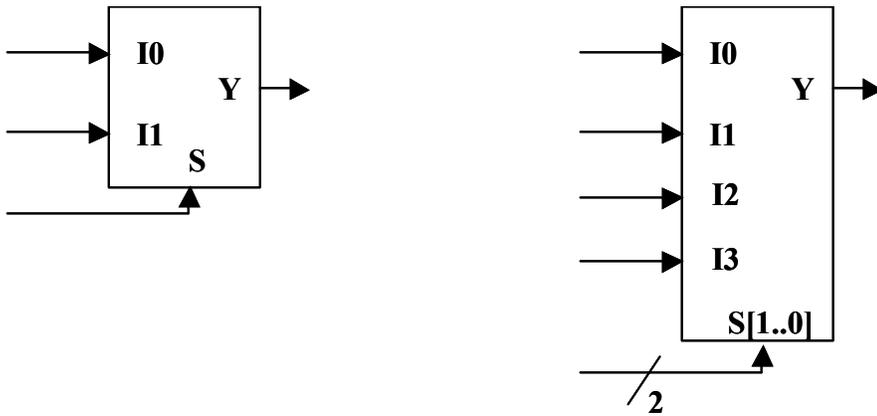
6. (10 pts) Fill in the blanks using terms from the following list:

INEFFICIENT, Volatile, 1, JEDEC, Non-Volatile, 0, VHDL, tri-state buffer, EFFICIENT, PLD, PRODUCT TERM, Memory, Intact, Fuse, POS, SOP, Non-Intact

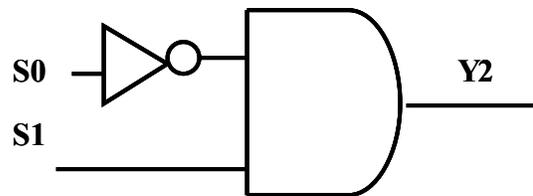
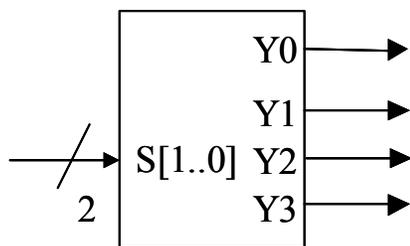
- i) When all fuses are blown, the value of a product term in a PAL is **ONE** (a blown fuse leaves its input as a '1' value, all '1's to a product term produces a '1').
- ii) A **PLD** is efficient at implementing wide Boolean functions and multiple functions of independent variables.
- iii) A programmable logic device is **non-volatile** if it retains its programming on power down.
- iv) A **tri-state buffer** has three output states: '1', '0' and high impedance.
- v) **VHDL** is a language used for specifying boolean equations which can be mapped to programmable logic.
7. (6 pts) Show via a schematic how the 2/1mux equation $Y = I_0 S' + I_1 S$ can be implemented using tri-state buffers.



8. (8 pts) The symbol on the left is for a one-bit 2/1 mux. The symbol on the right is for a one bit 4/1 mux. Draw a schematic showing how to create the 4/1 mux using 2/1 muxes.



9. (6 pts) The symbol below is for a 2 to 4 decoder. Show the gating necessary to implement the Y2 output.

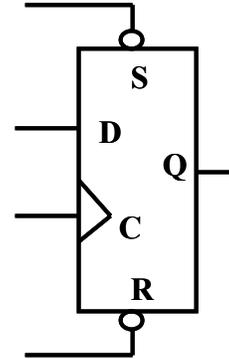


$$Y2 = S1 S0'$$

$$Y2 = 1 \text{ when } S = 10$$

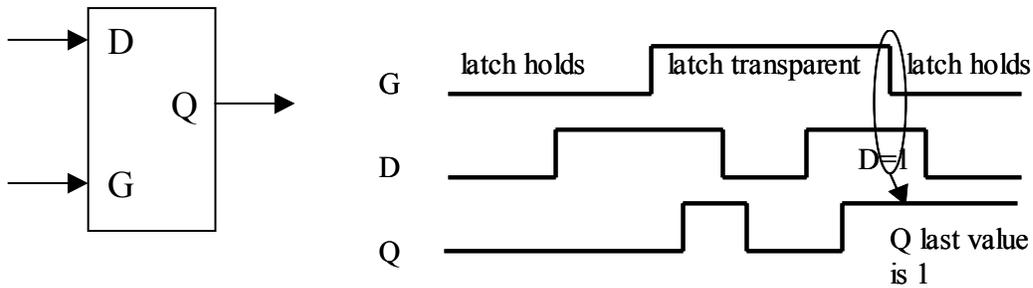
10. (8 pts) For the device shown below, fill in the VOLTAGE truth table for the inputs. Use 'L', 'H' for level inputs. For a rising edge needed on an input pin, use "L→H", for a falling edge needed use "H→L".

Output result	Inputs			
	C	D	S	R
Force output to a L regardless of clock	X	X	H	L
Force output to a H regardless of clock	X	X	L	H
Set output to a H on next active clock edge	L→H	H	H	H
Set output to a L on next active clock edge	L→H	L	H	H

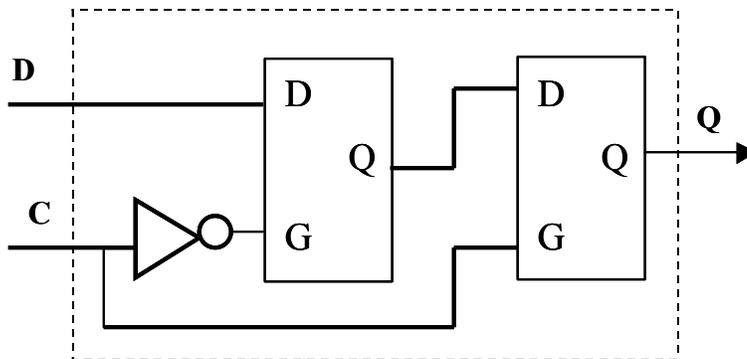


Set, Reset are NEVER don't care inputs. They always affect the DFF.

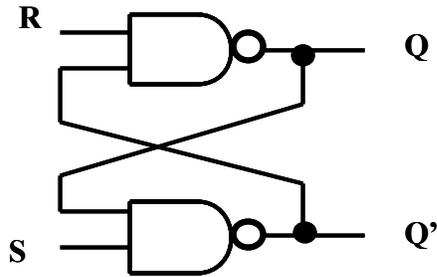
11. (6 pts) Complete the timing diagram below for the device shown:



12. (6 pts) Draw the schematic for a rising edge triggered DFF using two D-latches.



13. (6 pts) Draw the gate schematic for a Set/Reset latch with LOW TRUE INPUTS.



14. (5 pts) A clock has a period of 40 ns ($1 \text{ ns} = 10^{-9} \text{ s}$). What is the clock frequency in Mhz ($1 \text{ Mhz} = 10^6 \text{ Hz}$)

$$\text{Clock freq} = 1 / (40 \times 10^{-9}) = 0.025 \times 10^9 = 25 \times 10^6 = 25 \text{ MHz}$$

15. (3 pts) For the device shown in problem 10, what input(s) have a setup/hold associated with it?

Only input D has a setup and hold time associated with it. Input D has satisfy setup/hold times in relation to the rising clock edge in order for correct operation.

16. (6 pts) For the device shown in problem 10, what input(s) have a propagation delay associated with them?

Inputs C, S, R have propagation delays – changes on these inputs can cause the output to change.