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Routing Results For:

Silicore SLC1657 Evaluation Board for ORCA 3L FPGA

July 25, 2001

Test conditions:

Project:	CALCDEMO
Device:	Agere: OR3L165B7PS208DB
Synthesis tool:	Altium Accolade PeakFPGA 5.30a
Router:	Agere ORCA Foundry 2000

For more information, please refer to the SLC1657 Technical Reference Manual.

Timing Results (as reported by router):

Timing constraint (MIN):	5.000 MHz (MIPS)
Actual speed (MAX):	6.952 MHz (MIPS)

Device Utilization Results (as reported by router):

IO	35/517	6% used
	35/164	21% bonded
LOGIC	553/2048	27% used
PIO	35/512	6% used
PFU	353/1024	34% used
SLIC	200/1024	19% used

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