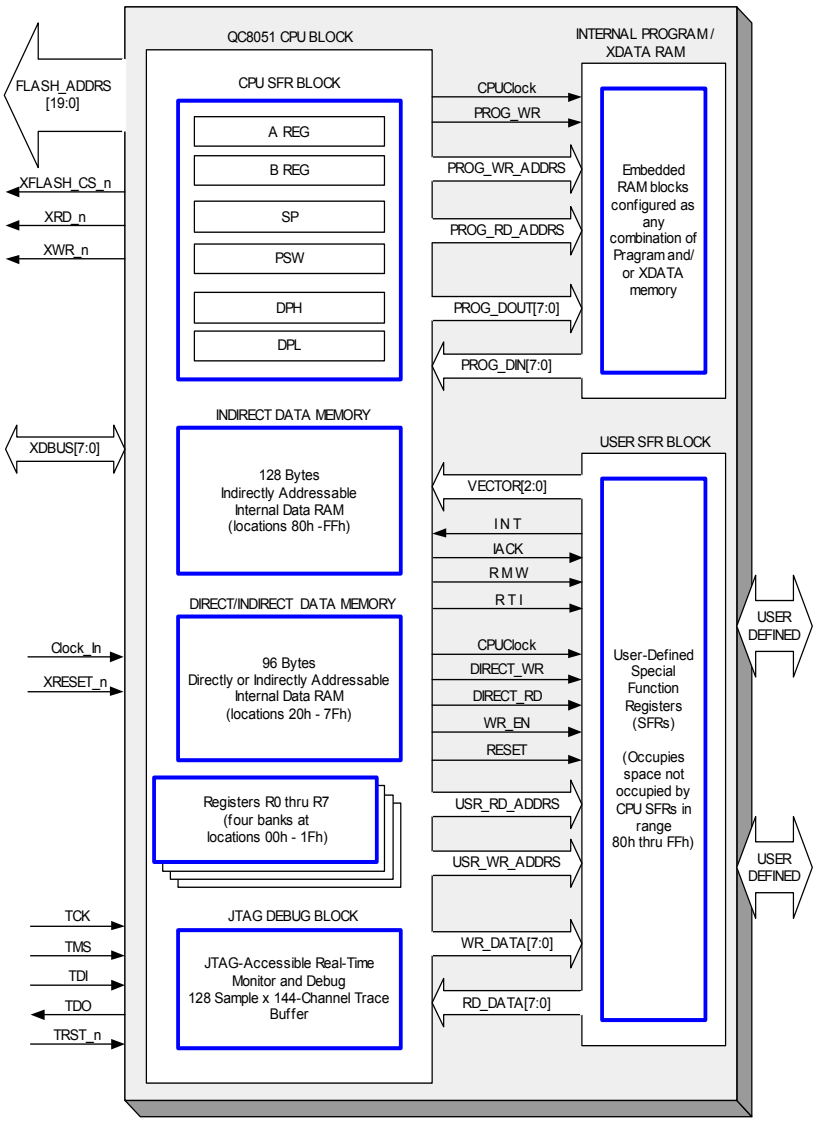
FPGA-8051 Soft Core

Real-Time Development Kit
For **Actel ProASIC^{PLUS}** * FPGAs

Features and Benefits

- Implement custom 8051 designs in an Actel ProASIC^{PLUS} FPGA using Actel Libero Development Environment Software and QuickCores QC8051 Real-Time Development Kit
- Compatible with Keil Software µVision2** debugger and C compiler
- Includes QuickCores small memory model (2K program reach) synthesizable QC8051 netlist library (compatible with Libero)
- Includes BoxView*** real-time "C" language debugger for QuickCores QC8051
- Includes target board with Actel APA-300 installed
- Flash-USB+ APA Device Programmer/Debugger (included in kit) :
  - Programs the Actel APA device
  - JTAG boundary scan controller (SAMPLE/PRELOAD monitoring)
  - JTAG real-time monitor/debugger interface
- 256KB (150ns) external flash memory for program/data storage
- 2-line X 16 character LCD
- 4 user buttons & 8 user LEDs
- RS-232 interface for user applications
- QuickCores QC8051 features:
  - Pipeline architecture allows most instructions execute in a single clock cycle
  - Customizable user SFR block
  - Real-time monitor architecture allows monitoring of internal operations without the use of embedded software routines via JTAG connection
  - Debug logic includes 128-sample deep X 144-channel real-time trace buffer
  - Traces 36-bit time stamp, PC, Instruction Register, PSW, SP, ACC, B, DP, Data RD address/data, Data WR address/data, interrupt acknowledge
  - Unlimited software breakpoints
  - Up to three hardware breakpoints



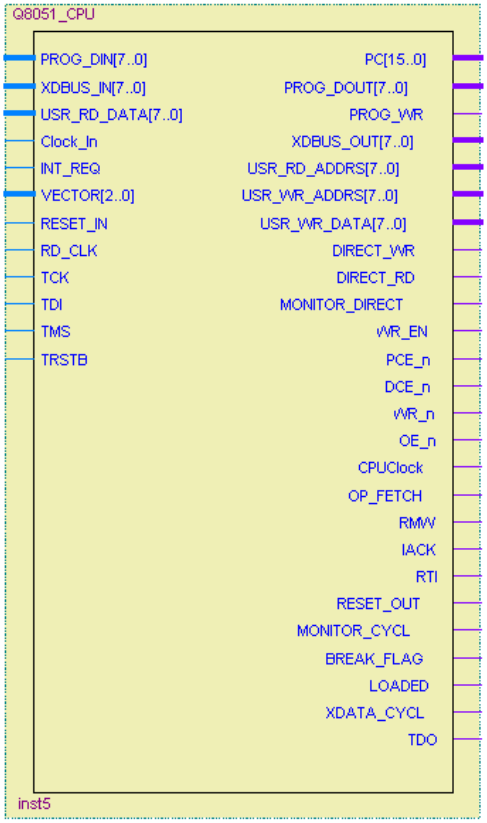
General Description

When used with Actel Libero integrated design environment software, QuickCores FPGA-8051 Real-Time Development Kit allows you to quickly create and debug custom 8051 designs in an Actel ProASIC^{PLUS} FPGA. The kit includes QuickCores small memory model QC8051 softcore, BoxView C language debugger which is compatible Keil Software 8051 C compiler and µVision2 IDE, target board and power supply. Example top-level 8051 references design programming files are also included. Large memory model QC8051 netlist library is available under a separate license.

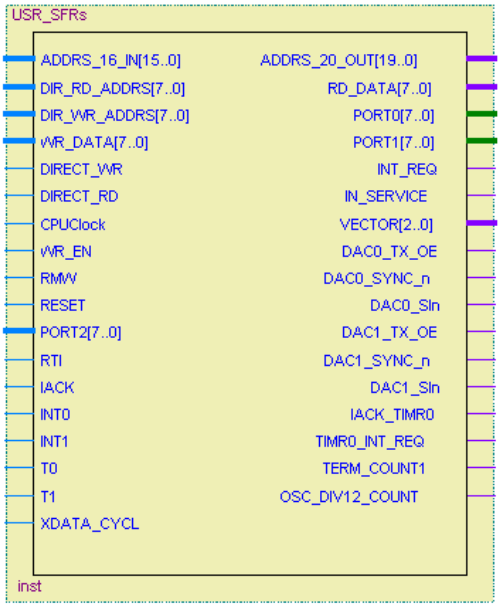
QC8051 CPU Module Signal Descriptions (instantiated at top level of your design)

Name	Dir	Description
PROG_DIN[7:0]	I	QC8051 program instruction bus input
PROG_DOUT[7:0]	O	QC8051 program write bus used by real-time monitor program write cycles
PROG_WR	O	Indicates program write during real-time monitor program write cycles
XDBUS_IN[7:0]	I	QC8051 external data bus input
XDBUS_OUT[7:0]	O	QC8051 external data bus output
PCE_n	O	Active low external program memory chip enable
DCE_n	O	Active low external data memory chip enable
OE_n	O	Active low external program/data output enable
WR_n	O	Active low external program/data write enable
USR_RD_ADDRS[7:0]	O	User SFR read address
USR_WR_ADDRS[7:0]	O	User SFR write address
USR_RD_DATA[7:0]	I	User SFR read data bus
USR_WR_DATA[7:0]	O	User SFR write data bus
DIRECT_WR	O	1 = internal data memory “direct” write cycle
DIRECT_RD	O	1 = internal data memory “direct” read cycle
MONITOR_DIRECT	O	1 = internal monitor data memory direct read cycle
WR_EN	O	1 = internal data memory write enable
Clock_In	I	External clock input
CPUClock	O	CPU clock output
MODE	I	1 = CPU clock = Clock_In / 1; 0 = CPU clock = Clock_In / 4 (use this for external interfacing)
OP_FETCH	O	1 = opcode fetch cycle
RMW	O	1 = read-modify-write cycle
IACK	O	1 = intrerrupt acknowledge cycle
INT_REQ	I	1 = interrupt request
VECTOR[2:0]	I	Bits [5:3] of the interrupt vector loaded into the program counter
RESET_IN	I	1 = reset
RESET_OUT	O	1 = reset; this signal internally gated by JTAG debug module
MONITOR_CYCL	O	1 = monitor cycle
XDATA_CYCL	O	1 = MOVX instruction; used by memory expansion circuit
TCK	I	JTAG TCK input
TDI	I	JTAG TDI input
TMS	I	JTAG TMS input
TRST_n	I	JTAG TRST_n input
TDO	O	JTAG TDO output

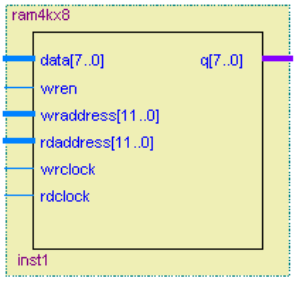
FPGA-8051 Real-Time Development Kit Netlist Library Top-Level Instantiation Symbols



Q8051 CPU (2K Memory Model)

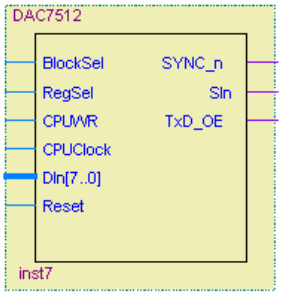


User-Definable SFR Block

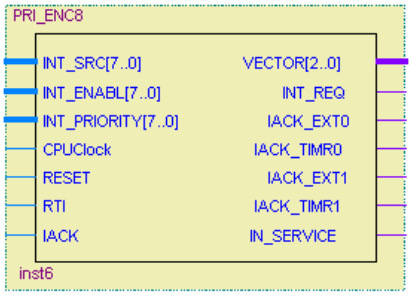


Various Size RAM Blocks for Program / Data Storage

User-Definable Special Function Register Block Symbols Included in FPGA-8051 Netlist Library

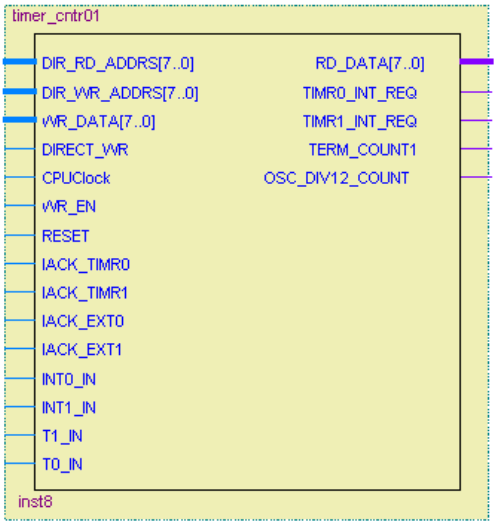


DAC7512 Serial Controller Port



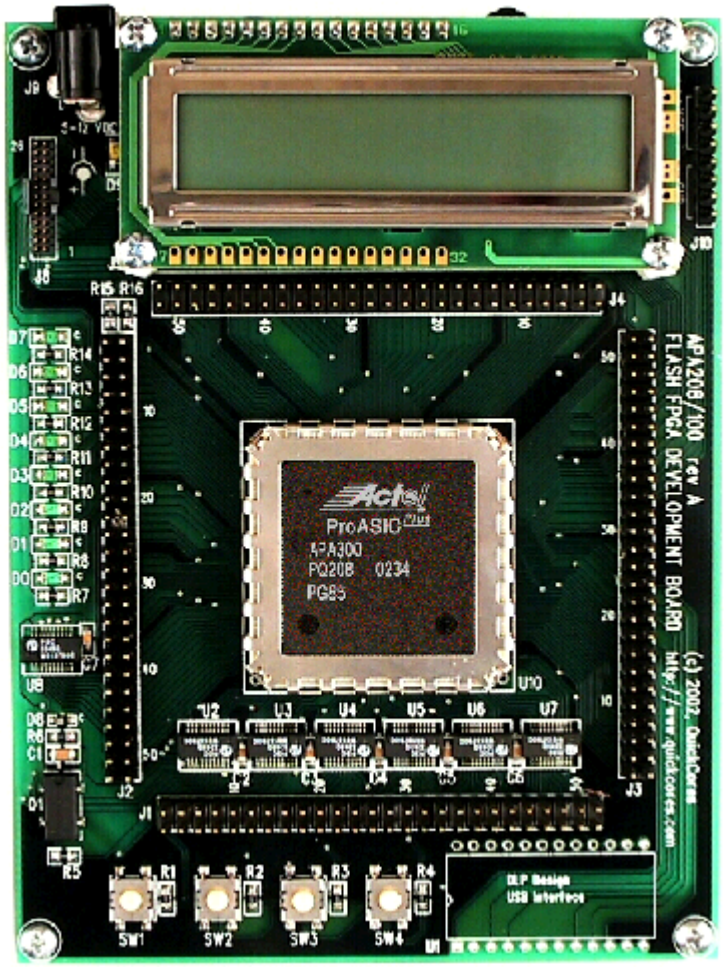
Interrupt Controller Block

Note: Other modules not shown include general purpose parallel port and external program / data memory extended address banking module. Large Memory Model Q8051 CPU and serial port available under separate license.



Dual 16-Bit Counter/ Timer Module

QuickCores APA-208 Target Board



ProASIC^{PLUS} APA208 Target Board Description

The QuickCores FPGA-8051 Real-Time Development Kit for Actel ProASIC^{PLUS} FPGAs includes the APA208 Target Board pictured above. Programming the flash-based ProASIC^{PLUS} device is through the FlashUSB+ programming/debug pod included in the kit. Once the device is programmed with the desired QC8051 design, the implemented QC8051 design user application software can be programmed and debugged using the same FlashUSB+ pod. JTAG boundary scan (SAMPLE/PRELOAD) monitoring of the ProASIC^{PLUS} APA device pins is also by way of the FlashUSB+ pod interface.

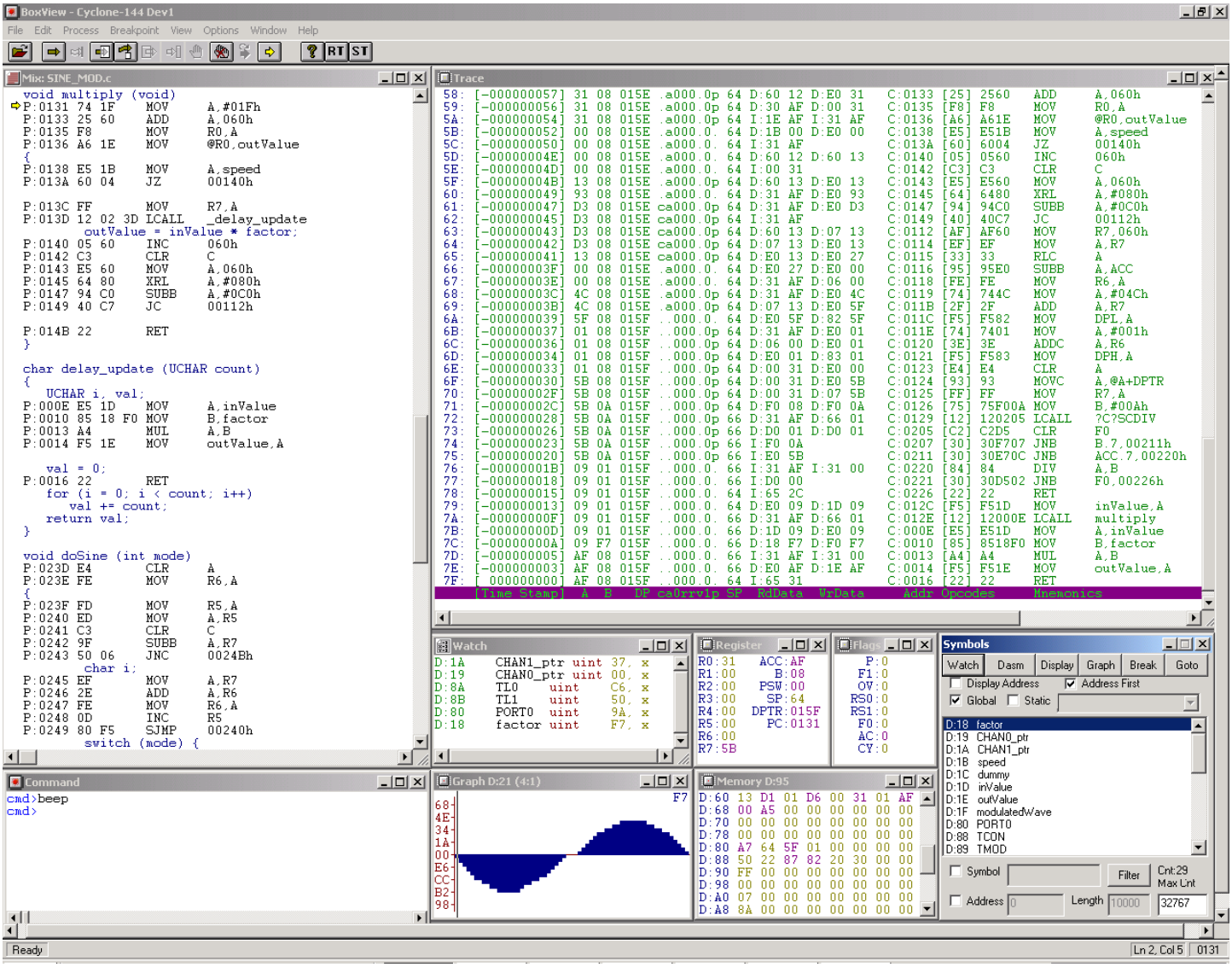
Provided on the APA208 Target Board for your use are 128 Kbytes (x16 bits) external flash memory, 2-line X 16-character LCD, four user buttons and 12.288 MHz oscillator.

Although the QuickCores QC8051 Real-Time Development Kit includes an Actel APA-300 ProASIC^{PLUS} FPGA, small (2k-reach) memory model QC8051 netlist library which you can use to create your own designs, the APA208 Target Board is shipped with a large memory model QC8051 programmed into the ProASIC^{PLUS} APA device and on CD.

FPGA-8051 Real-Time Development Kit
For **Actel ProASIC^PLUS** FPGAs

QuickCores

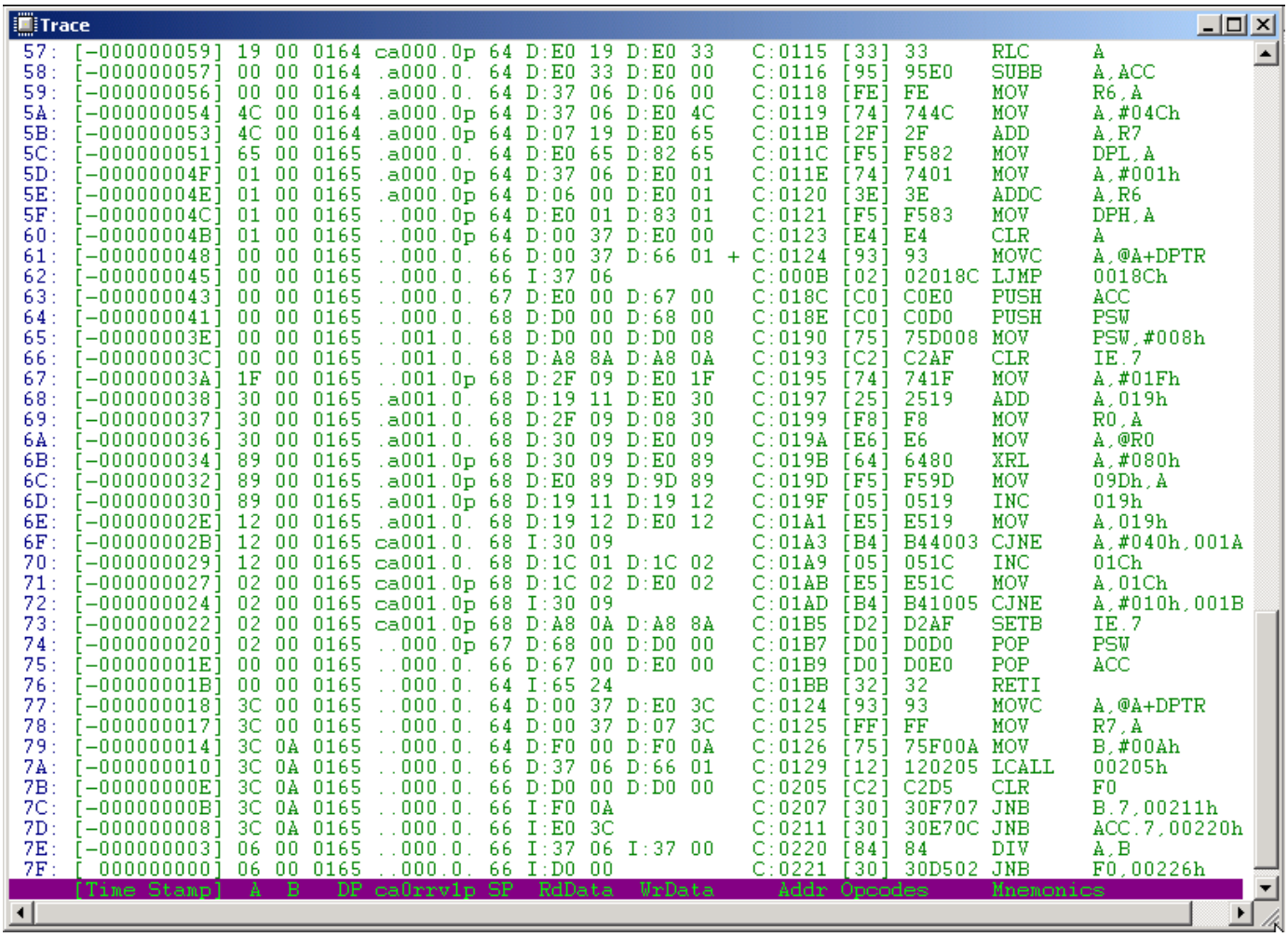
BoxView C Language Real-Time Debugger



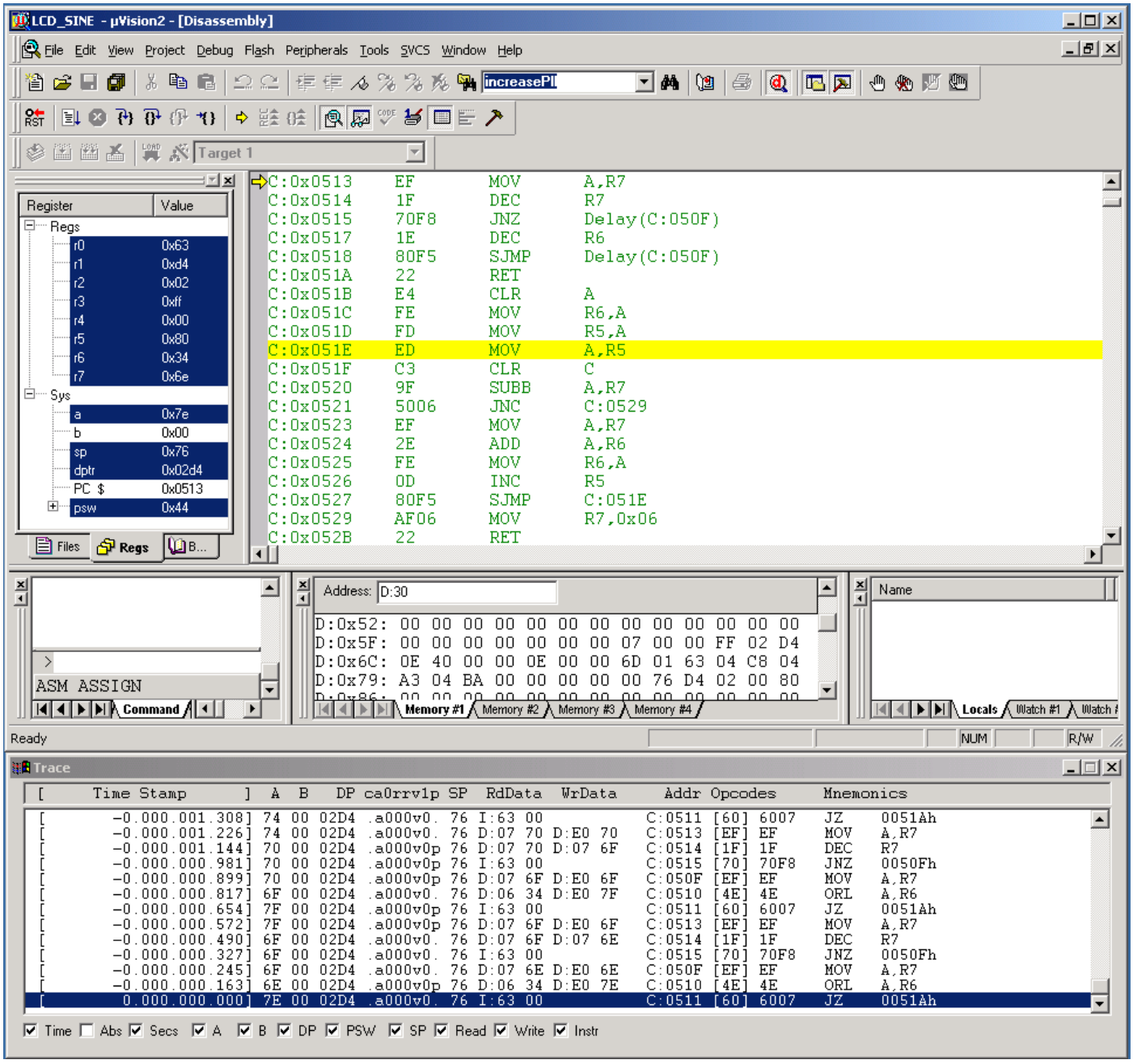
BoxView Real-Time C Language Debugger Key Features

- Built-in STAPL player programs the target APA device via QuickCores Flash-232+ or Flash-USB+ pod.
- Real-time trace buffer displays 36-bit time stamp, ACC, B, DP, PSW, SP, Data RD address and data, Data WR address and data, PC and Instruction Register contents
- Supports concurrent and remote monitoring and debugging of multiple CPUs
- Code window with source, mixed or assembly display mode
- “Symbols” widow allows you to quickly set breakpoints, disassemble, or watch
- Multiple memory windows for data, code, indirect, or external locations
- Graphic display of any memory region allows animation in real-time mode
- On-the-fly monitoring and editing of registers and memory
- Robust JTAG command and scripting language with data logging for automated testing

FPGA-8051 Debug Module 128 Sample X 144-Channel Real-Time Trace Buffer



Keil Software µVision2 IDE Supports QuickCores FPGA-8051 Soft Core



Keil Software µVision2 IDE Key Points

- Provided with the FPGA-8051 Real-Time Development Kit are the appropriate .dlls which will allow seamless operation with Keil Software µVision2 IDE and C51 compiler
- Concurrent real-time monitoring and debug of multiple CPUs is supported when µVision2 IDE is used in combination with Domain Technologies BoxServer and BoxView Debugger
- The FPGA-8051 real-time trace buffer is supported under µVision2 “Peripherals” menu item

FPGA-8051 Real-Time Development Kit for ProASIC^{PLUS} Contents

The FPAG-8051 Real-Time Development Kit for ProASIC^{PLUS} comes with the following items:

- QuickCores APA-208 target board with APA-300 ProASIC^{PLUS} FPGA installed and preprogrammed with large memory model QuickCores FPGA-8051 microcontroller
- BoxView real-time C language debugger with integral STAPL player device programmer/driver
- QuickCores small (2k program reach) memory model netlist library targeted Actel ProASIC^{PLUS} FPGAs and restricted for use with Libero
- Flash-USB+ APA device programmer/debug pod
- 9-volt power supply
- Target board schematics
- User Guide
- Example large memory model FPGA-8051 top-level and user SFR designs in Verilog and compiled .rpd file format
- Required dlls for use with Keil Software µVision2 IDE

QuickCores Design Services

Along with its microcontroller IP, QuickCores also offers non-recurring engineering (NRE) design services to assist customers with integrating QuickCores microcontroller IP into their designs. This service is available on a quotation basis. Other services include development of custom application software, both on the host PC side and on the target embedded application side.

Ordering Information

FPGA-8051 Real-Time Development Kit part number (small memory model): **QC8051-RTDK-APA-S**

Contact Information:

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Discount Coupon

Purchase a QuickCores QC8051 Real-time Development Kit (small memory model) before December 1, 2003 and receive 25% off the list price of $595.