



## The Intelligent VHDL Design Entry and Verification Environment

## **Increase Productivity**

VHDL Studio<sup>™</sup> provides advanced design entry with design wizards and incremental analysis. Design wizards streamline the design entry process by automating tedious and time-consuming tasks. With the incremental analysis continually analyzing your code as you edit, VHDL Studio<sup>™</sup> can provide early error detection on-thefly as well as access to up-to-date design navigation.

## **Reduce Overhead**

VHDL Studio<sup>™</sup> integrates design entry with fast VHDL'93 behavioral and structural (VITAL/SDF) simulation. With a single seamless environment for both design entry and verification, less time is spent learning and using two difapplications.



## VHDL Studio™

## **Project Management**

#### • Project Creation Wizard

Existing designs can be easily imported into VHDL Studio<sup>TM</sup> with the project wizard, which determines all the files and libraries required by a given top-level entity/architecture.

## **Design Entry**

#### • VHDL Editor

The built-in editor performs color high lighting of VHDL source code to facilitate reading, and automatic identifier completion to reduce typing.

#### WHDL Studio File Edit Options Project FSM Buffer Debug Help ÷ Target: hc11(behavior):Hc11.vhd subc(B : byte, A : byte, r : byte, carry : boolea $\square$ else hc11.prj -hc11.vhd read\_op16(mode,X); setflags16(X); end if; end if; when ADDIADC => prn\_msg(show\_instructions,"ADD(C)"); read op8(mode,arg8); if (instr\_b(6)='0') then addc(Å,arg8,Å,(class\_i=ÅDC)); addc(B,arg8,B,(class i=ADC)); - Behavior of onchip ram - Bonchip address : integer rw : bit mem\_array is array of Demm\_array is array of Deprom1 : eprom + Sciki : clock INIT : byte HPIO : byte CCR : byte pending : bit int no : natural end if; when SBC[SUB => prn\_msg(show\_instructions,"SUB(C)"); - reset read\_op8(mode,arg8); if (instr\_b(6)='0') then subc(&,arg8,&,(class\_i=SBC)); -read write - ready 🔁 burst subc(B,arg8,B,(class\_i=SBC)); 🔁 clk end 1f; when ADDD => D(15 downto 8):=A; D(7 downto 0):=B; -bus id 🕒 oe - we FSM Pro 🛢 int no : natural ► ► • □

#### • State Machine Editor

The most intuitive way to design a state machine is with a state machine diagram. VHDL Studio<sup>™</sup> includes a graphical state machine diagram editor for intuitive state machine entry that automatically and transparently generates a VHDL implementation.



#### Project Browser

The browser provides a quick overview display of the project. Each file in the project and its contents are displayed, including libraries external to the project.

#### Automatic Build

VHDL Studio<sup>™</sup> automatically calculates file dependencies and determines the correct compilation order for the selected target.

#### Error Navigation

Compilation errors are easily located by double clicking on error messages to jump to the error's location in the source file.

#### • On-the-fly Error Detection

Using incremental analysis, VHDL Studio<sup>™</sup> can instantly detect syntax errors as you type and eliminate the tedious compile, locate error, and edit cycle.

#### • Auto-prompting

Auto prompts provide you quick information about previously defined subprogram signatures, and signal/variable types without leaving your current editing position to locate the definition in another location or even in another file. Auto prompts are always up-to-date due to VHDL Studio's incremental analysis engine.

# VHDL Studio™

#### • Instance/Component Creators

Component and instance wizards make component declaration and instantiation a snap. Just select any entity from your project and the component creator will insert a matching component declaration in your design. The instance creator provides a simple graphical interface for assigning local signals to

face for assigning local signals to the ports of the instantiated entity for fast, errorfree component instantiation.

#### Graphical Testbench Designer

The testbench designer provides a graphical waveform editor for simple and intuitive testbench design. In interactive mode, the simulator updates output waveforms as you edit the

inputs. Timing checks and data checkpoints are also easily added to the waveform diagram. You can run the testbench within VHDL studio for a graphical display of timing and data violations or run the automatically-generated VHDL testbench yourself.

### **Design Navigation**

#### • Hierarchy Browser

The hierarchy browser provides a complete structural view of your design's units, blocks, instances and processes, as well as type, signal, variable, and subprogram information. Double clicking on

any item in the browser instantly brings you to the file and line number where the item is defined. Thanks to VHDL Studio's incremental analysis, the browser is always up-to-date with changes made in the editor.

#### • Hypertext Navigation

In VHDL Studio<sup>TM</sup> your VHDL is more than plain text, its hypertext! If you forget the type of that signal, or the arguments to that function,



simply right click on its name to instantly jump to its definition.

#### • Navigation History

Even with all the advanced design navigation features of VHDL Studio<sup>™</sup>. you'll never get lost with the "back" button, which will

quickly return you to your

previous location in the design.

### Simulation

#### • Native VHDL'93 Compiler

VHDL Studio<sup>™</sup> includes a new version of the Green Mountain VHDL Compiler for fast, direct-compile simulation.



#### • Waveform Display

Graphical waveform display makes simulation results easy to browse and understand.

#### • Source-Level Debugging

Source-level debugging provides statement-bystatement execution for detailed debugging. Source-level debugging includes breakpoints to quickly simulate to the point of interest for detailed, statement-by-statement debugging.

## VHDL Studio™

#### • Tcl/Tk Scripting

The simulator provides Tcl/Tk script support to enable unlimited customization and automation.

#### • VITAL Optimization

The new version of the Green Mountain VHDL Compiler in VHDL Studio<sup>™</sup> includes VITAL specific optimizations and built-in VITAL libraries delivering performance up to **7 times faster** than the previous version.

#### • SDF Backannotation

Post-route simulation with timing information is provided through standard SDF backannotation.

## **Product Support**

Free Technical Support

E-mail support is provided at no charge.

• Free Minor-Release Updates

VHDL Studio<sup>™</sup> owners have access to the most recent minor release via our support Web pages.

• No Maintenance Fees

Technical support and minor release upgrades are provided with no annual maintenance fees.

## **System Requirements**

#### Windows

- Pentium PC/64MB of RAM
- Microsoft Windows 98, Me, NT 4.0, or 2000
- 20MB of hard-disk space (installation only).
- CD-ROM

### Linux

- Pentium PC/64MB of RAM
- Linux 2.0 or greater

- 20MB of hard-disk space (installation only)
- CD-ROM

#### Solaris

- Sparc V8 or better/64MB of RAM
- Solaris 2.7 or 2.8
- 20MB of hard-disk space (installation only)
- CD-ROM

#### **Components**

- On-line VHDL Tutorial
- On-line VHDL Reference Manual
- On-line User's Guide
- Project Wizard
- Project Manager
- Design Browser
- VHDL Editor
- Incremental Analysis
- State Machine Editor
- Instance Wizard
- Test Bench Generator
- VHDL'93 Simulation
- Source-Level Debugger
- Waveform Viewer
- VITAL/SDF Simulation
- Tcl/Tk Scripting

## **Contact Information**

For more information or to order call **800-656-5380** (fax: 802-434-5071), visit our Web site at: http://www.gmvhdl.com

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