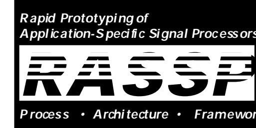
Application Of DFT To RASSP Benchmark 3

R. J. Tarzaiski
(609) 338-4046
rtarzais@atl.lmco.com
3/28/96

Benchmark 3 System Definition

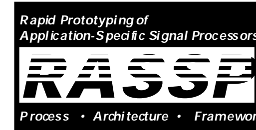


- Functional Element (FE) consisting of 2 Arithmetic Processor boards (FPCAP) and 1 Controller board (FPCTL) to upgrade AN/UYS-2A processor FE
- Multiprocessor DSP applications
- High speed I/O, high processing throughput
- Fabricated as 3 SEM E boards
- Must meet memory and logic fault coverage specs during field deployment
- Must self check periodically
- Uses ASICS with BIST, MCMs, some non-BS components

Topics Addressed

- Selecting a Testability Architecture
- Defining Consolidated Requirements
- Construction of TSD0 and its derivatives
- Defining a Singular Test Philosophy
- Evaluation of available test means
- Role of Dependency Modeling

Requirements, Strategies, and Architectures



Reqts

Consolidated Reqts

DM

Test Strategy

Testbench Arch

Testability Arch

Tester Arch

BS Path
BIST
Control

TSD

BIST/BS

Test Means

Testbenches

Test Vectors

Test Vectors

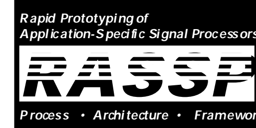
STP

Test Plans

Select Actual
Test Means

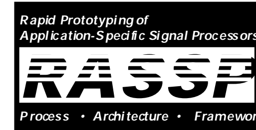
Test Procedures

Procedure For Requirement Consolidation



- Design, manufacture, and field reps complete phased requirements template set
- Merge flaws/faults in phases where possible using common test means and test support
- Formulate preliminary Singular Test Philosophy across phases
- Negotiate agreement on STP and add phase-specific supplements to STP where needed
- Add conformance requirements and generate formal document

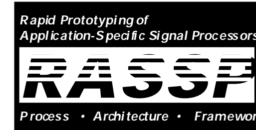
Consolidated Test Requirements Contents



- Specific flaw/fault model for each requirement
- Quantitative metrics for detection, isolation, and correction requirements
- Customer and derived requirements for design, manufacturing and field tests
- Allocation of available test means to each requirement
- Conformance requirements

- **Requirements Template used to formalize complete quantitative statement of requirement**

Consolidated Requirements and TSDs for RASSP Systems

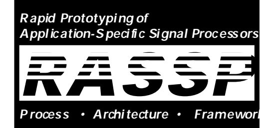


- BM3 consolidated requirements and TSD0 can be entered into a reuse library to serve as basis for design of future systems
- Provide standards for DFT introduction into a project
- Impose a maximum reuse philosophy on available test means during all project phases
- Ensure positive contribution from test area toward performance improvement and cost reduction

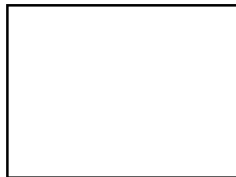
Test Strategy Diagrams

- TSD describes effectiveness of test means for detection, isolation, and correction of flaws/faults
- TSD implemented as EXCEL workbook
- TSD0 begins with 3 worksheets
  - Requirements
  - Predicted values
  - Differences between requirements and predictions
- TSD0 will evolve to TSDn as system is better defined
  - Addition of worksheets to support monitoring verification and measurements at lower architectural levels
- Downward and upward data flow provided by EXCEL intersheet communication process

Typical TSD

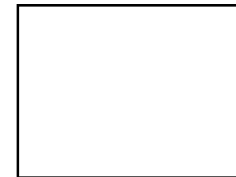


Sheet 1



Requirements

Sheet 3



Deviations

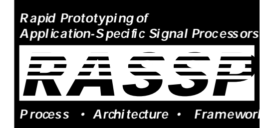
Sheet 2

Roll-ups

User
Comments

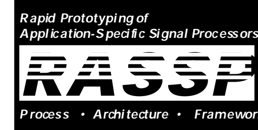
User entries
Pred, Verif, Meas

TSD Data Sources



- Consolidated Requirements document
  - supplies test means
  - supplies transfer function values to requirements sheet
- Test Time and Cost analysis for design, manufacturing, and field deployment phases
  - Project specific
  - Company specific
- Dependency model
  - aids in allocation of time and cost among test means

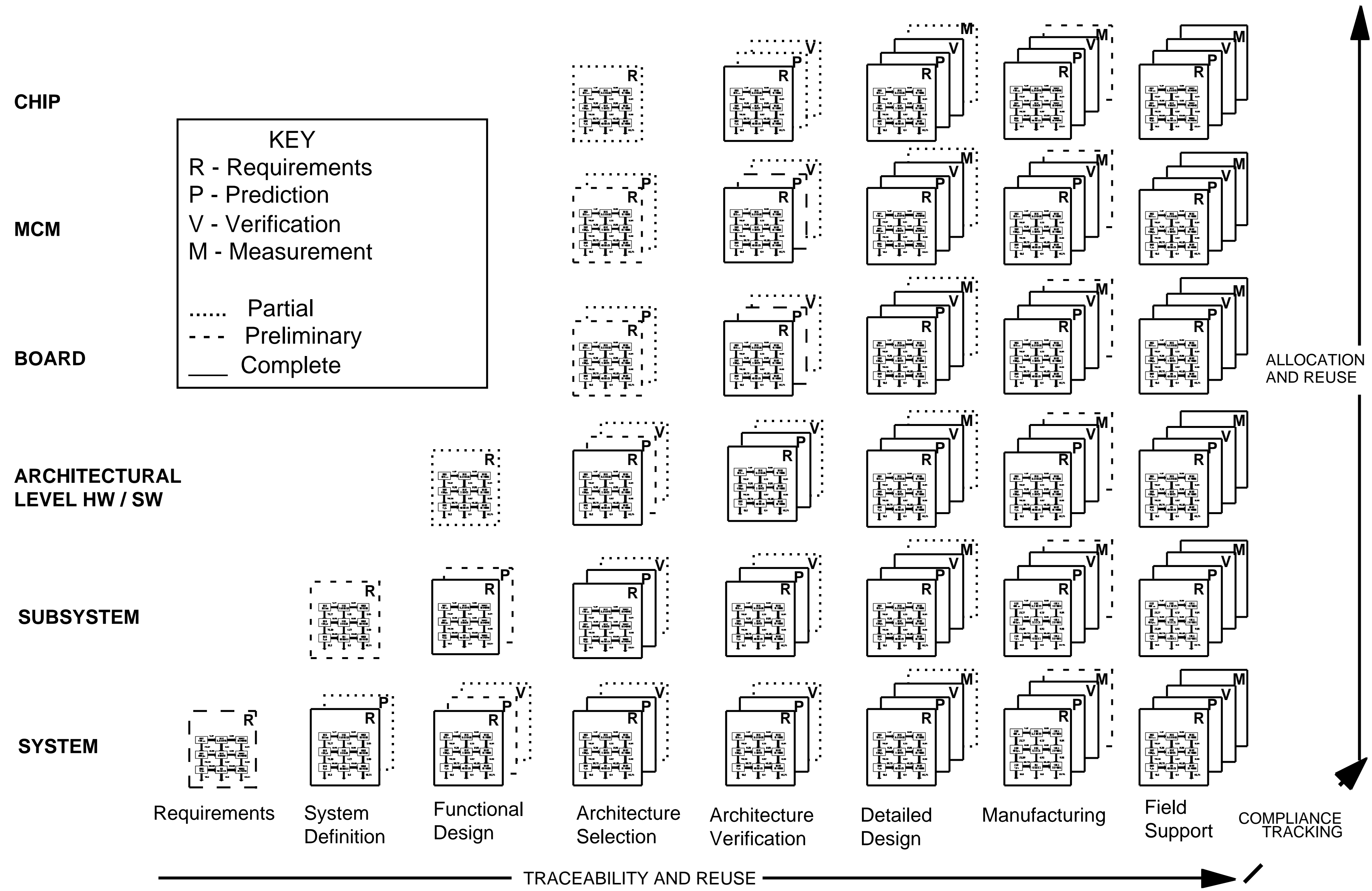
Role of TSD



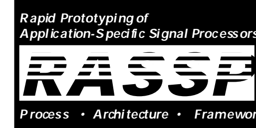
- Document the **Singular Test Philosophy** for all phases of a project
- Establish a monitored test strategy which will result in complete satisfaction of the consolidated requirements
- Compare predictions, verifications, and measurements to requirements throughout program life cycle
- Flag significant deviations from requirements
- Inform designer what is expected from different levels of test
- Ensure that test process is validated and accepted by designers

Hierarchy of Test Strategy Diagrams

Rapid Prototyping of Application-Specific Signal Processors
RASSP
Process • Architecture • Framewor

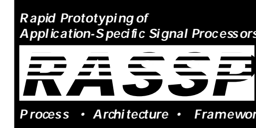


TSD Application



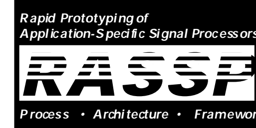
- Original plan for TSD was complete population
  - Still valid concept where required
- TSD is a strategy evaluator and planning tool
  - Allocates cost, time, and fault coverage to test means
  - Allows consideration of effects of means interchange and fault coverage reallocation
- Hierarchical in nature to allow its use at various levels of packaging as required
  - All entries to all levels of system phases and packaging levels may not be needed
- TSD usage extent is **project** and **Company** specific

TSD Value Population



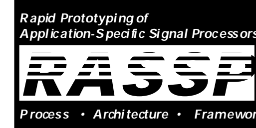
- Three quantitative measures used in BM3 TSD structure
  - Transfer Function for fault coverage
  - Cost Attribute
  - Time Attribute
- **Transfer function** values selected from experience base or specific knowledge of test means coverage
  - First assignments will be Predictions - subject to modification
- **Cost attribute** values assigned on basis of economic analysis of the proposed application of test means sequence
  - may be based on previous experience
  - fixed (test equipment) and variable costs (labor)
- **Time attribute** value assigned primarily from experience base

Test Means Sequence



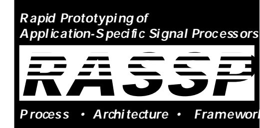
- General Rule : Assign test means in order of "effectiveness" measured by
  - — shortest test execution times
  - — highest coverage
- Always minimize the number of faults passed on to expensive, time consuming tests (where possible)
  - — Manual usually most expensive and slowest - reserve for last
  - — For BM3, the preferred performance sequence is :
    - – BIST, BS-ATE, ATE, MANUAL
- Transfer functions combine as :
  - — Total Coverage = (1 - TF1)(1 - TF2)(1 - TF3) ...(1 - TFn)
- Sequencing and magnitude variations trade-offs are a significant feature of the TSD
  - — Time and economic effects become manifest

Preliminary Economic Models for Prediction



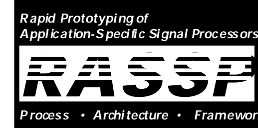
- Must be based upon a specific project (e.g., BM3) , a Company testing model (available test means) and the TSD structure for the project
- For BM3 the following test means are available
  - Inspection
  - BIST
  - BS-ATE
  - ATE
  - MANUAL
  - SIMULATION
  - OPERATIONAL TEST

Primary Economic Assumptions



- Number of FEs to be produced - 500
  - Total number of boards - 1500
- Labor rate - $75.00 per hour
- Production Interval - 1 year
- ATE Investment for project - $500000
- Test Means are **always** Applied Where Specified in the TSDs - No Tests Skipped
- Some Overlap Exists Among Faults Detectable by Test Means - Efficiency Better than simple application implies
  - Use efficiency factor to estimate this effect

Fixed Cost Model

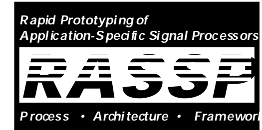


Test Means	Fixture Cost	Non-Recur Labor	Test Eq	Cost/Board
INSPECTION	1000	3000 (40 hr)	0	2.60
BIST	1000	15000 (200 hr)	1000	11.33
BS-ATE	4000	30000 (400 hr)	20000	36.00
ATE	4000	30000 (400 hr)	500000	349.00
MANUAL	1000	6000 (80 hr)	5000	8.00
SIMULATION	0	30000 (400 hr)	0	20.00

OPERATIONAL TEST - Normal Field Operation - No cost

TOTAL FIXED COST / BOARD - $ 426.93

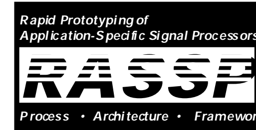
Test Time Model



Test Time Performance per Board

Test Means	Indiv Test Time	Alloc Factor	Effic Factor	Effective Time
INSPECTION	300 s	1	1/1	300 s
BIST	0.1 s	8	8/8	0.8 s
BS-ATE	120 s	6	3/6	360 s
ATE	300 s	6	3/6	900 s
MANUAL	300 s	8	4/8	1200 s
SIMULATION	0			
OP TEST	0			

Variable Cost Model



- Assumption - Variable cost is **test labor** time

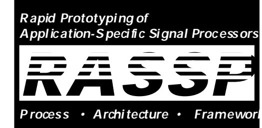
Test Means	Test Time	Test Labor Cost/ Board
INSPECTION	300 s	6.25
BIST	0.8 s	-
BS-ATE	360 s	7.50
ATE	900 s	18.75
MANUAL	1200 s	25.00

SIMULATION - Part of Design Engineering Effort

OPERATIONAL TEST - No additional cost for observation of results.

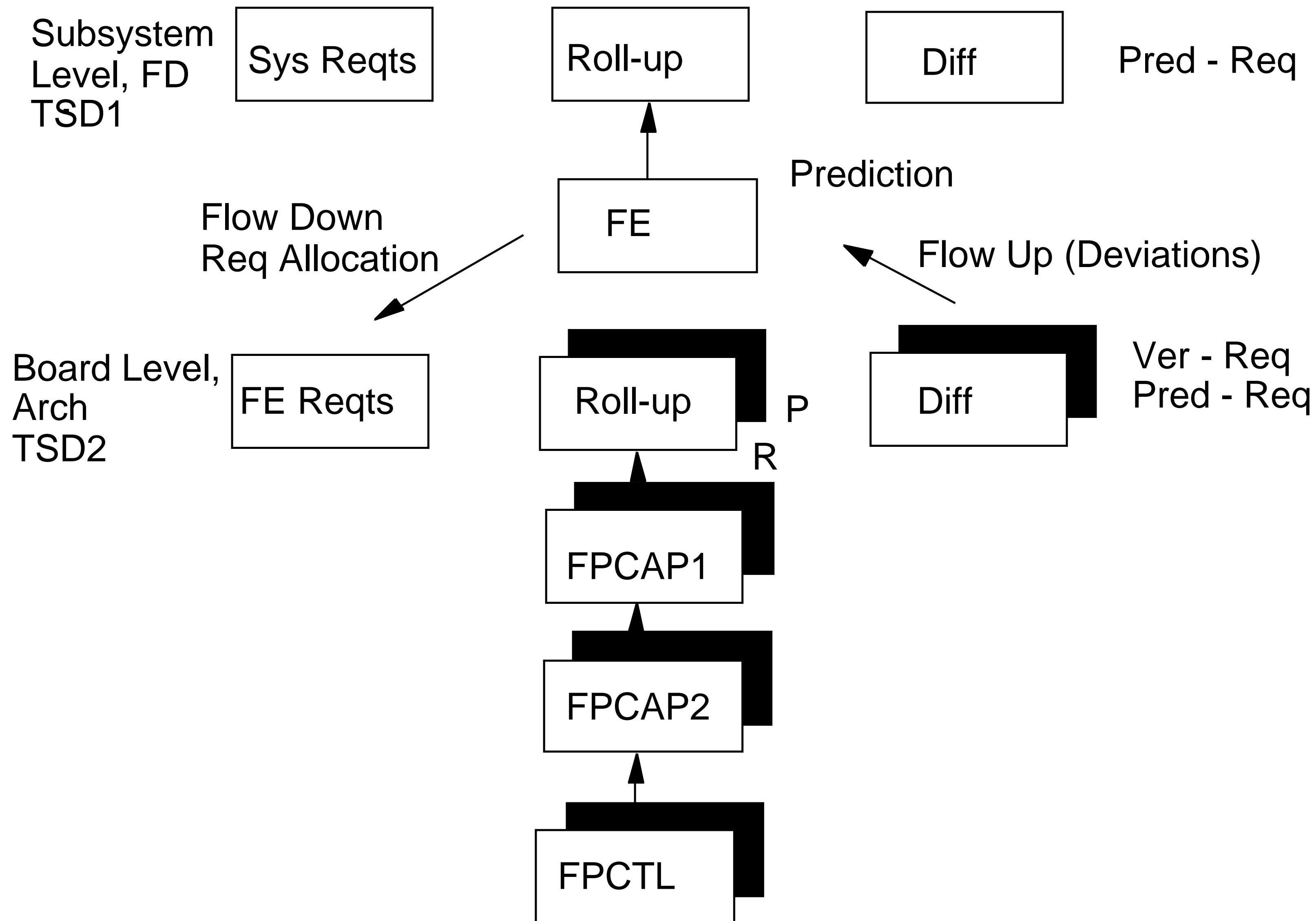
- Total Variable Cost/Board (All Project Phases) - 57.50
- Variable Costs lower than fixed costs in this case

Summary Of Test Cost For Model

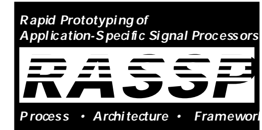


• Fixed Cost / Board	$ 426.93
• Variable Cost / Board	$ 57.50
• TOTAL COST / BOARD	$ 484.43
• Cost of Test for 500 FEs (1500 Boards)	$726,645

TSD Hierarchy

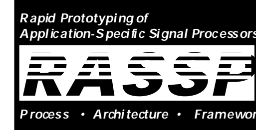


Top Level Test Philosophy



Anomalies / Test Means	Design Flaws	MFG-Open/ SA0-1/ Bridge	MFG-Dynamic	MFG-Netlist Violation	Field - Organiz. Level	Field - Depot
Simulation, VP, 1st Article	X					
BIST	P	X	X		X	X
BS-ATE	X	X		X	X	X
non BS-ATE	X	X	X	X		X
Manual	X	X	X	X	X	X

Tools For Singular Test Philosophy Implementation

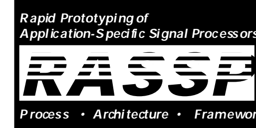


- STP ultimately is implemented with specific tools which can provide flaw/fault detection, isolation, and correction (detection, isolation, correction)
- Test means are applied to groups of flaws/faults which have been established as significant sources of failures
- Detection, isolation, correction coverages provided in varying degrees by a known collection of available tools
- Mapping of available tools to specific flaw/faults allows generation of a **detailed test plan** from which **test procedures** will be developed
- Following charts show application of tools to the Benchmark 3 project

Dependency Modeling (TDM)

- Dependency modeling is an independent means for evaluating system testability
- Usable at various levels of **packaging hierarchy** from system through board/module
- TDM offers **earliest** recommendations - can be used in parallel with early TSD generation
- **Suggests what needs to be tested and whether it is testable**
- Based upon criticality assignments (time, cost, and user preference) specified by the user
- Multiple tools available - WSTA, STAT
- Allows “what if” analysis of test point assignment alternatives

TDM to TSD to Fault Coverage Path

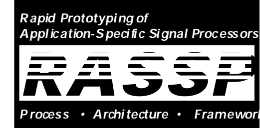


Dependency Model (TDM) → Preliminary Test Definitions and Recommended Test Strategy based on user specified values of cost, MTTR, MTBF, and system criticality

Consolidated Requirements → TSD → Singular Test Philosophy Using Generic Test Means Applied in a Specific Order

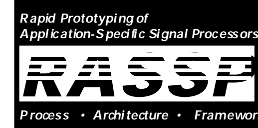
Expansion of Faults Detectable by Generic Means → Allocation of Available Specific Test Means

TDM Recommended Test Sequence



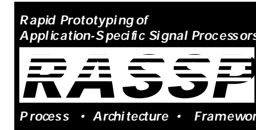
- Ordered set of tests based upon
  - — probability of component failure (MTBF)
  - — user specified importance of tests (TestX)
  - — test philosophy- cost/time criticality
- Test sequence proceeds to isolate faulty component
- Cost and time to repair are user inputs
- Testability analysis can proceed even if these quantities are not known (uniformity defaults)

Benchmark 3 Component Models for TDM I



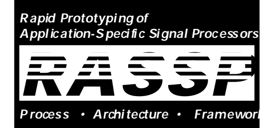
Component	Cost	MTBF	MTTR
FPGA	1000	$2x10^6$	2
Flash Mem	100	$2x10^6$	.5
1.2V PS	300	$5x10^5$	1
PAL	50	$3x10^6$	.5
Clk Osc	100	$6x10^6$	1
EDAC	100	$2x10^6$	1
PN MCM	5000	$1.1x10^5$	3
Comm MCM	4000	$1.2x10^5$	3
Comm ASIC	300	$.4x10^6$	2

Benchmark 3 Component Models for TDM II



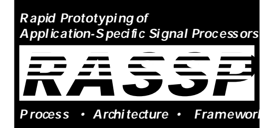
Component	Cost	MTBF	MTTR
FIFO	150	$1x10^6$	1
EPROM	100	$3.8x10^6$	.5
Clk Buff	50	$6x10^6$	.5
SRAM(8/set)	50	$1.3x10^5$	1
DRAM(10/set)	50	$1x10^5$	1
Scan Cntl	100	$6x10^6$	1
Xcvr	50	$9x10^6$	.5
FPCTL LBus	1000	10^7	4
FPCAP LBus	1000	10^7	4

TDM BIT Recommendations



- Selection of a set of tests based upon test strategy which can certify that the system under test is operational
- Tests follow success path (pass path of binary pass-fail test tree of test strategy) to no fault aspect
- Fastest verification of operational status

TDM Nodal Aspect Report



- Listing of possible faults remaining after execution of any given test
- Begins at root node which contains all aspects
- Proceeds to terminal nodes which specify faulty member of system under test
- Used with test strategy to evaluate remaining fault possibilities during test sequence