Latest FPGAs in the market

Owais Ahmed - 40040018

COEN 6501 – Digital Design and Synthesis

September 15, 2018

Table of Contents

Introduction

The Field Programmable Gate Array – FPGA debuted from 2.0-micron technology in 1985, the first FPGA from Xilinx Inc., XC2064 had 1200 logic gates, 64 logic cells and 58 I/O pins [1]. Today, the process has outgrown to 14 nm tri-gate fabric and products have up to 5 million logic cells, 1640 user I/O pins, 137 Mb of block RAM (BRAM), 3,600 DSP blocks, etc. [2]. The technology advancements have taken over the FPGA industry by storm in last couple of years and a collaboration of leading manufacturers has announced their next product on 7nm node size which will be out in the market within less than a year [3], leaving the existing products obsolete which were not even 5 to 7 years old.

This report mainly discusses the exponential growth of the FPGA industry and their latest products in the market which were not older than 3 years or so. The report also provides a comparison between product families of the two top notch manufacturers. It was quite challenging to provide a comparison among products from different companies as both are doing equally great with the features and it is just a matter of the time as to when the competitor came up with something better than the existing one. However, this report describes in detail the technological enhancements and why a product is classified into its respective family. The concept that was considered equally important along with comparing these latest products is the direction in which the FPGA industry is leading. The world's largest chipmaker (i.e. Intel) had acquired one of the biggest FPGA manufacturer (i.e. Altera) to set new records in the market and opening a new room for prospect application in supercomputing where even high-end microprocessors and SoCs were lacking to fulfil the requirements.

Looking at the big picture, two previously invented but recently produced technologies ruling the market discussed in this report are: (1) Hybrid FPGAs, in which an FPGA core is coupled with a hard implementation of an ARM processor and other peripherals provided with very high-speed communication on a single chip of silicon. (2) Three-dimensional stacked FPGAs, in which three or four FPGA dies are stacked side-by-side on a single piece of silicon with interconnections. However, different manufacturers are exploiting these technologies in different ways and have named them differently. Nonetheless, detailed explanation, variations and fusion of these technologies are out of the scope of this report. Moreover, it is also assumed that the reader have the basic knowledge of FPGA's building blocks.

The content of the report are as follows: Chapter 2 reviews the literature regarding FPGA industry covering the recent acquisitions, future estimations, application sector reaping benefits and the growth barriers to the industry. Following chapters cover the latest product portfolio of FPGAs in the market by two big companies and their comparison. These chapters further highlight the strong ties of both companies with third parties to push the industry to the next level.

FPGA Market Insights

Considering the scope of this report, this chapter focuses on Compound Annual Growth Rate Comparison (CAGRC) of FPGA industry. The market share of top five vendors in the industry were taken into account and a thorough research with respect to their annual sales for the fiscal years 2015 and 2016 was conducted to find their respective share. It should be noted that these figures exclude sales of all the products other than FPGAs which may include one-time programmable devices and other power modules. Next, the percentage growth from 2015 to 2016 for each company was calculated.

Table 1: Listing of yearly sales of different FPGA manufacturers along with market share and growth [4].

	2015		2016		
Vendor	**FPGA Total**	**Market share**	**FPGA Total**	**Market share**	**Growth CY15 to CY16**
Xilinx	$2044	53%	$2167	53%	6%
Altera -> Intel	$1389	36%	$1486	36%	7%
Microsemi	$301	8%	$297	7%	-1%
Lattice	$124	3%	$144	3%	16%
QuickLogic	$19	0%	$11	0%	-40%
Others	$2	0%	$2	0%	0%
TOTAL	**$3879**	**100%**	**$4112**	**100%**	**6%**

The numbers in Table 1 reveal a couple of worth-noting stats including the names of the giants in the market. It gives comprehensive information on the size of the market as to where and how fast it is growing. For a broader perspective, note that the growth rate from 2014 to 2015 was approximately 1.5% [5], thus the market outgrew by the factor of 4 to 6% in the year of 2016.

Looking at each company one by one, there is no doubt that Xilinx holds the biggest share in the market since a decade and outpasses Altera's market share (now Intel) for the last three node sizes. However, Intel had just made the greatest acquisition in the semi-conductor industry and it is too early to reap the benefits of Altera still, somehow managed to lead Xilinx's annual growth by 1%. This comparison also reflects the dive in the FPGA market during this tenure which was mainly due to the newly adopted direction of supercomputing (discussed in the next chapter). Lattice semiconductor survived this renaissance being one of the most exposed to the FPGA technology. In addition to this, Lattice managed to observe an annual growth of 16% which is much higher than Xilinx and Altera, despite being much smaller in size than both.

Recent Accretions

In 2016, the two long-time industry rivals Xilinx and Altera aced more than 90% of the market and continually dominated the market for more than a decade. However, there had also been other smaller yet prominent players in the market. Ranked third, Lattice semiconductor has established its recognition in the market for low-power SRAM-based FPGAs integrated with flash. They promoted their best performing FPGA as "High Value" for per unit cost. Lattice semiconductors further expanded their portfolio to extremely low power optically non-volatile FPGAs by acquiring SiliconBlue Technologies in 2011 for $62 million USD in cash [6].

Recently, Microchip Technology Inc. is predicted to emerge as a prominent FPGA vendor after acquiring Microsemi Corporation in March 2018 for a total enterprise value of $8.35 billion [7]. Microsemi one of the very few FPGA vendors to provide high-performance and radiation-hardened analog mixed signal integrated FPGA. Their renown portfolio totally complies with the aerospace and defence industry standards.

However, the news that caught the semiconductor world by storm was the acquisition of the leading FPGA manufacturer Altera by Intel Corporation in June 2015 for $14 billion USD [8]. The cost of this acquisition was almost 7 times the annual sales for fiscal year 2014 i.e. $1.93 billion. However, the reason that justifies Intel's huge investment was the prospective FPGA market in server computers. Intel is an undisputed leader in the production of data centre processors, while companies like AMD, Samsung, Nvidia dominate mobile processors. However, the acceptance of ARM processor has started catching attraction of server computers and analysts project that as early as 2016, 10% of all servers shipped would be microservers equipped with ARM chips. This prediction would have shaken Intel's position but, the reason why Intel managed to dominate the market so far is the software compatibility. Most of the codes that runs web servers are written for x86 architectures of Intel® Xeon® processors. Thus Intel took a significant advantage of this competitive edge until Xilinx or Altera came up with a competition.

First quarter of 2011, Xilinx Inc. introduced industry's first extensible processing platform, an FPGA-centric hybrid chip which integrates a complete dual-core ARM Cortex-A9 processor based on 28nm technology named as Xilinx Zynq-7000 All programmable SoC [9]. The new architecture combined the software programmability of an embedded processor with hardware flexibility of an FPGA, abstracting most of the hardware burden away of the embedded software developer. Knowing that, Microsoft had initiated a project named Catapult to transform Cloud computing and came up with estimation, marrying FPGAs with processors has shown dramatic increase in performance. Deployment of FPGA increased throughput of Bing (web search engine) by 95% with only 10% increment in power consumption [10]. Without delay, Intel acted to counter the threat posed; they tied with Altera in ARM-FPGA advances and announced successful production

of hybrid FPGAs in their foundries, which was named as SoC FPGA. This turned out to be a very strong selling proposition of ARM chips in datacenters and led to the acquisition of Altera by Intel.

In late 2011, conforming to the growing computational re-equipment's of the industry Xilinx Inc. lead the market once again by start producing 3D or stacked FPGAs [11]. To shrink the size and power consumption of FPGAs, Xilinx stacked several separately produced high density parts of FPGA in one package employing the technology for 3D construction. This approach got initiated by coupling 28Gbit/s serial transceiver with an FPGA, Virtex-7 HT, called heterogeneous FPGA [12]. Originally this technology was first invented by an American fabless chip start-up Tabula founded in 2003 in Santa Clara, CA USA [13].

Growth Estimation

The Global Field Programmable Gate Array Market is forecasted to have exponentially grow over a period of 7 to 8 years as per various research publishers and market analysis firms. According to the Variant Market Research Inc., California, US:

"The global market is expected to grow from 2016 to 2024 at compound annually growth rate of 7.3%, which will expand from $6.9 billion to 12.1 billion US dollars. Geographically, Asia-Pacific has been recognized as the largest market covering 39.7% of the share in 2016 which will continually dominate throughout forecast period till 2024. Moreover, the CAGR of this part of the world will also be a bit higher than Rest of the World which will be 7.9% and 7.4% respectively. The second largest market will be accounted as North America expanded over 27.8%, mostly driven by increasing number of internet user and telecommunication networks. Lastly, SRAM product type will be the most prominent out of all available in which data is stored statically in the form of logic cells [14]*".*

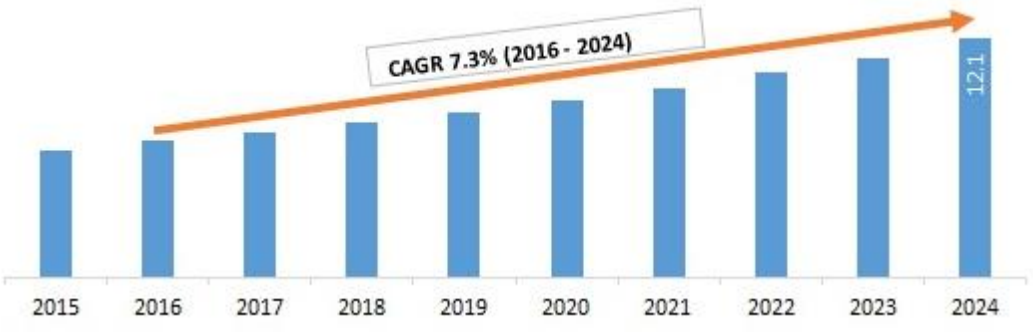

Figure 1: FPGA market size forecast by Variant Market Research [US $ Billion] [14].

Dominant Application Sectors

Today, FPGA is widely used in industries ranging from telecom to aerospace. The reason of its widespread adoption that it gives an advantage over ASIC in terms of design change even after the product has been deployed in the field. This feature allows the designer to upgrade from a remote location eliminating the need of fabrication from scratch. Another factor that fuels the growth of FPGA market is the demand of extensive computation in applications which gives a new direction to the FPGA industry. Knowing that, cloud computing and data processing in data centres will emerge as a fastest growing application sector of the industry, some other industries utilizing FPGAs in their products are reaping technological enhancement benefits at large.

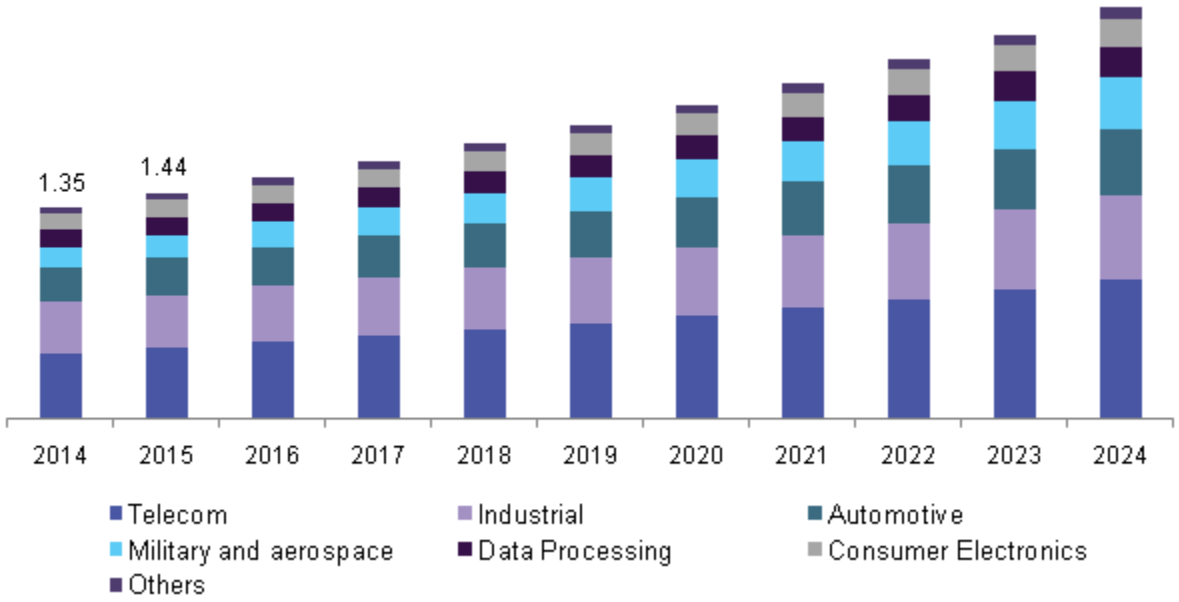

Figure 2: The proportion of application sectors comprises the complete FPGA market estimation [15].

According to Figure 2, three top FPGA application sectors that are forecasted to grow exponentially are telecommunication, military and aerospace & automotive. Next, let's take a closer look of each of these sectors along with the advantages, trends and challenges posed:

Telecommunication

The telecommunication sector captures the largest share of the FPGA market and the trend is expected to continue throughout the forecast tenure considered [15]. This growth trend is largely backed by the increasing demand of smartphone and internet access. The number of internet users is now increasing in rural areas as well and the new communication technologies including 3G, 4G LTE and 5G are being accepted all over the world, mostly North America and Asia Pacific. Thus, high demand in wireless telecommunication sector has led to high-bandwidth requirement

transceivers coupled with FPGAs. Different manufacturers in the industry have come forward addressing these needs, for instance, Altera (now Intel) offers a complete portfolio for such high-bandwidth protocol demands ranging from 600 Mbps to 30 Gbps [16]. While Xilinx Inc. introduced a newly adapted 3D process technology which combines separately built components on a single chip, started with combining an FPGA with transceivers termed as heterogeneous process technology to boost bandwidth with minimal increase in power [17].

Military and Aerospace

The differentiating features of FPGAs over ASIC make them very appealing for applications in defense and aerospace. The ability to get reconfigured and long deployment lifetime was itself enough to compete with other available programmable devices. Additionally, the FPGA manufacturers are working to make these devices tamper less to prevent reverse engineering. When it comes to military application, the two primary requirements that should be meet are: assurance of data security achieved by cryptography which keeps from decoding and, anti-tempering to secure deployed intellectual properties and enable to stay ahead of potential attackers [18]. Xilinx Inc. offers their complete range of FPGA products in military and defense grade as well. They are building their product to comply with DO-254, an industry standard for anti-tamper devices which are capable of self-destruction when an attempt is made [19].

However, an issue being addressed by the manufacturers is SEU – Single Event Upset which hinders the acceptance of FPGA in aerospace industry. The single event transient leading to upset could arise due to a number of reasons that have already been addressed over time by the VLSI design industry but the one most vulnerable to aerospace industry is exposure to cosmic radiations. This has become an area of focus for FPGA manufacturers as the technology approaches below 45nm because single unit may expand to multiple unit disturbance with reduction in size. Xilinx Inc. has a complete range of products where one widely accepted is Virtex-5QV FPGA [20], which is radiation hardened enough to comply with industry standards..

Automotive

The rapidly improving automotive industry accounts higher degree electronics in automobiles such as driver assistance, car-surrounding cameras, infotainment systems extended to battery management systems in electric vehicles. This industry seems to pose the highest demand of reconfigurable computers to be deployed in expensive cars which could be upgraded later, similar to a new operating system every year to please the drivers or probably to support release of entertainment episodes as per user requirement in a driverless car. Information coming in from sensors and cameras in vehicles at an increasing rate can no longer be adequately handed

by microprocessors or microcontroller alone. Therefore, to serve the growing number of automotive applications specifically, motor driven units has been introduced called Intel® Cyclone® 10 family [21].

Hindrances in Growth

The FPGA products are getting more complex to meet the market needs. Lately launched Virtex UltraScale+ family by Xilinx Inc. has boasted 3.6 million logic cells and 128 transceivers [22] while the MPSoC with multiprocessors like ZYNQ UltraScale+ have reached up to 600K logic cells per core [23]. This means longer turnaround time and expertise requirement for hardware design and quality assurance. However, lack of standardization in hardware verification technique is one of the major challenge faced by the FPGA market. The existing 15 years old verification techniques; constrained-random and coverage-driven simulation, formal property checking and assertion-based verification are lagging behind from the hardware advancements. Therefore, in pursuit of reducing the development cycle time of FPGAs, manufacturers are are actively seeking better verification techniques [24].

Secondly, despite much technology advancement in FPGA, their designs are - on average - 35 times larger than ASIC designs, 3.5 times slower and consume on average 14 times more power than ASIC [25]. Therefore, FPGAs have been reserved for low-volume applications where companies avoid paying huge premium for the fabrication process of ASIC rather than affording programmable chip. This is the reason why the FPGA market will outgrow 6% to 7% in the next 6 to 8 years, whereas ASIC sales is forecasted to grow 10.1% [26].

Xilinx Inc.

Xilinx Inc. is an American semiconductor manufacturer primarily known for their programmable logic devices. The company was founded in 1984 headquartered in San Jose, USA and known for inventing FPGA devices. In fact, they created the first fabless manufacturing model – the fabless manufacturing is the design and sale of semiconductor chips while outsourcing the fabrication of the devices to semiconductor foundry, both the leading FPGA manufacturers Xilinx and previously Altera (prior Intel acquisition) used Taiwan Semiconductor Manufacturing Company Limited for the fabrication process.

Xilinx offers a comprehensive multi-node portfolio to address requirements across a wide set of applications. Whether you are looking to design a high performance networking application needing highest capacity, bandwidth, and performance or require a low-power, cost effective, high volume chip you will find a suitable one from Xilinx FPGAs and 3D ICs with optimized performance.

In January 2016, Xilinx shipped their first 16nm Virtex UltraScale+ device which was industry's first high-end FinFET FPGA [27], classifying the devices into two main families; Virtex – the high-end 3D FPGAs and Kintex – the mid-range FPGAs. Moreover, the company termed their 3D heterogeneous FPGAs coupled with ARM processor as Zynq - All Programmable SoC which also falls under the scope of this report. And, the Xilinx's 7 series has also expanded in early 2017 with the addition of low-cost, high-volume Spartan 7 FPGAs.

Virtex UltraSCALE+

Virtex is the flagship family of Xilinx FPGA products, the new Virtex UltraScale+ model provides the highest transceiver bandwidth, highest DSP count, and highest on-chip and in-package memory above all devices available in the market. The device is equipped with up to 3.6 million system logic cells, 8GB of High-bandwidth memory (HBM) Gen 2 integrated within the package, up to 500 Mb of total on-chip integrated memory, 100G Ethernet MAC Integrated blocks and 16 PCI Express® Gen 3 blocks. The Virtex UltraScale+ is declared as the industry's most energy efficient machine learning interface providing 60% lower power and 3X system-level performance compared to 7 series Virtex FPGAs [28]. The highest DRAM bandwidth enables the integration of in-package 8GB DRAM with HBM (Gen2) up to the maximum bandwidth of 460GB/s, this is 10 times higher memory bandwidth than other discrete memory channels available, built on proven 3rd generation 3D IC technology. The enhanced DSP slices enable a massive jump in fixed-and floating-point performance for a variety of workloads providing up to 21.1 TeraMACs (38 TOP/s) of DSP compute bandwidth and double-precision using 30% less resources [29].

The product is a good fit for applications like Deep Neural Network (DNN) for Artificial Intelligence (AI), complex data analytics, 4K live streaming video and advanced networking and security features provided with hardware acceleration. Cloud services providers especially the renowned ones like Amazon and firstly, Baidu has announced the usage of this device as a hardware accelerator and smart network interface cards in their data centres [30].

Kintex UltraSCALE+

The Kintex UltraScale+ is the mid-range family providing range of devices almost with same features and block performance as the high-end Virtex UltraScale+ family. The key of the family is to provide right set of resources while enabling the devices to operate at comparatively low power and in smaller package, such devices fulfil the requirement in challenging, space-restricted environments. The wireless communications market could be a good example of such specification.

"Kintex UltraScale+ FPGA consolidated the capability of two Kintex-7 FPGAs into a single device. The low power consumption featured in the 16nm FinFET+ process is a significant advantage—but cannot come at the sacrifice of performance. Kintex UltraScale+ FPGAs have been designed to operate at low power consumption while still achieving the system frequencies important to wireless designs from 491MHz to the 737MHz required by many 5G systems. These devices can include up to 3,528 DSP slices capable of operating at nearly 900MHz, dramatically pushing the performance envelope of many wireless designs. Kintex UltraScale+ devices use a combination of 16.3Gb/s GTH transceivers and 32.75 Gb/s GTY transceivers, bringing 30+ Gb/s communication into the mid-range and ensuring the devices have the required bandwidth to support increasingly ubiquitous standards such as JESD204B [31]."

- Pushing Performance and Integration with the UltraScale+ Portfolio,
White Paper Xilinx Inc.

A prospective application with highlighted improvements could be a 1 GHz eBand Modem. The system integration can be reduced from 2 chips to 1 chip with system performance gain of 1.2 times. Additionally, reduction in cost and power are also estimated by 10% and 34% respectively when upgraded from existing infrastructure to Kintex UltraScale+ device [32].

ZYNQ UltraSCALE+

Soon after the launch of 7 series FPGAs, Xilinx set an example by revealing the first device combining high bandwidth FPGA with a maximum of sixteen 28 Gbit/s and seventy-two 13.1 Gbit/s transceivers on a single chip of silicon, as Virex-7 HT – the industry's first heterogeneous FPGA [33]. This leads to the introduction of Zynq-7000 family, which integrates a complete ARM Cortex-A9 processor-based system on a 28 nm FPGA for system architects and embedded software developers. In December 2013, it announced an UltraScale SoC architecture, called Zynq UltraScale+, in TSMC 16 nm FinFET process. Today, the ZYNQ family provides an unrivaled level of system performance, flexibility, and scalability. The portfolio provides a wide range of devices categorized as SoC – System-on-chip, MPSOC – Multiprocessor system-on-chip, RFSoC – RF System-on-chip suitable for a various set of applications. The Figure 3 gives an overview of all the hybrid devices offered by Xilinx Inc. also depicting differences between them but, considering the limited scope of this report only the multiprocessor family is briefly discussed [34].

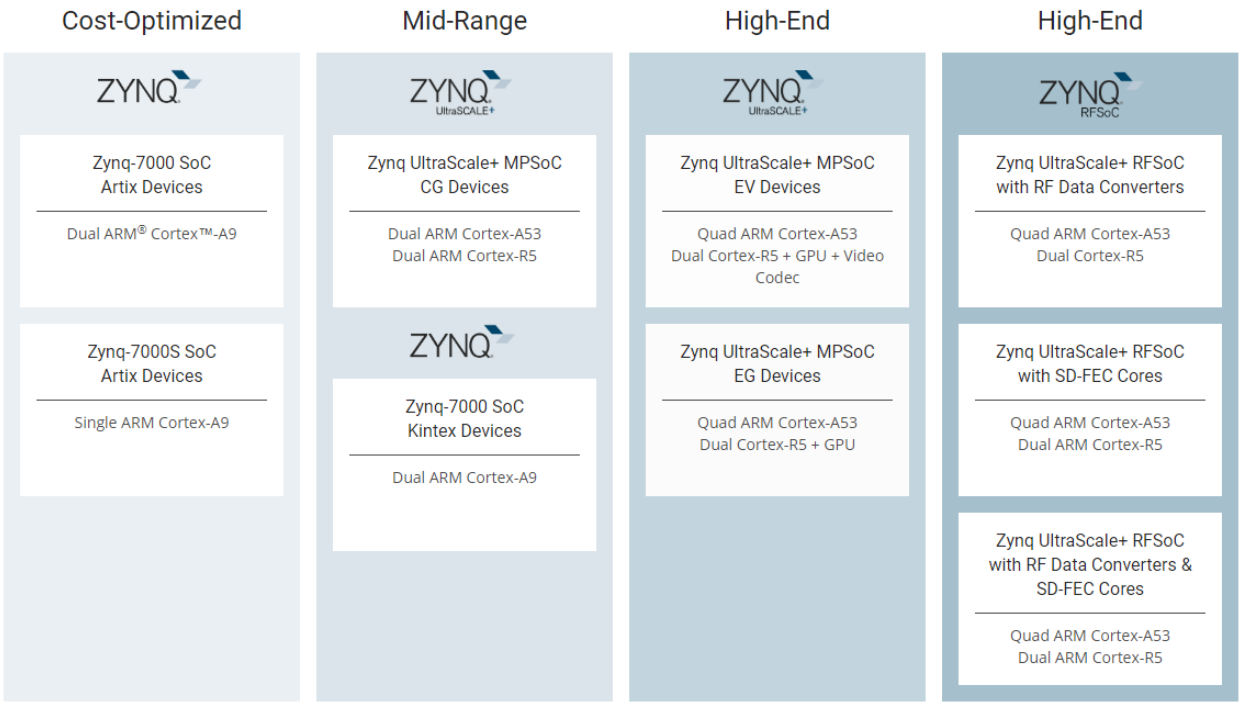

Figure 3: The complete portfolio of hybrid FPGAs offered by Xilinx Inc [34].

For the most compute-intensive applications UltraSCALE+ MPSoC provides 100 times better performance over conventional processor based systems. The Zynq UltraSCALE+ MPSoC family consists of three variants; Dual-core application processor equipped (CG) devices best fit for industrial motor control and sensor fusion. Quad-core application processor equipped (EG) devices to be deployed in wired and wireless networks, data centre, and Aerospace and Defense

applications. Video codec equipped (EV) devices are ideal for multimedia, Automotive ADAS, and surveillance applications [35].

In a typical camera-based advanced driver assistance system (ADAS) application Zynq UltraScale+ MPSoC solution can reduce system integration from 3 Chips to 1 Chip, increased system performance up to 3X, reducing the cost and power by 10 and 25 percent respectively when compared with existing systems based on previous Zynq-7000 hybrid FPGAs [35].

SPARTAN 7 series

In May 2017, Xilinx expanded the 7 Series with the production of the Spartan-7 family. The device is designed to offer low cost, low power and IO optimized applications for connectivity in industry. The Spartan-7 family offers 50 percent higher embedded performance than the previous generation, equipped with Xilinx 32-bit MicroBlaze soft processor IP. Spartan-7 devices also offer a layered security solution with AES-256 bitstream decryption, SHA-256 bitstream authentication, and on-chip eFUSE key storage. Coming to the software enhancements, now for the first time, Spartan FPGA-based designs can take advantage of the Vivado Design Suite [36].

The device is equipped with up to 400 I/Os and 100K logic cells, 800Mb/s DDR3 integrated with analog mixed signal blocks. The only 28 nm FPGA available in 8x8mm packages and also optimized for 2 PCB layers. It is the lowest priced device of 7 series family, and in comparison to the other devices in the series, it lacks in high-bandwidth transceivers availability. Spartan 7 delivers the highest value of performance/watt optimized for I/O connectivity in applications like any-to-any connectivity, sensor fusion, precision control, safety and security, and may go up to image processing too [37].

Altera – now part of Intel

Altera Corporation was an American manufacturer for programmable logic devices founded in 1984. Since then Altera has been the biggest competitor of the FPGA inventor, Xilinx and shares the second largest market share. Xilinx and Altera together has occupied over 90% of the market since 2015. Whereas later in 2015, Altera was acquired by Intel and is now part of it [8].

Altera shipped their first FPGA with full hard implementation of ARM processor in December 2012 [38] and named them as SoC FPGA. Considering the scope of this report, only selected products of the company are discussed in detail: SoC FPGAs and simple FPGAs which are further classified into high-end Stratix series, mid-range Arria series, low-end Cyclone and MAX series for PLDs. The Stratix 10 are the company largest, highest bandwidth, best performance hybrid FPGA devices. Arria 10 provides balanced performance, power, and cost suitable of mid-range applications. The Cyclone 10 are conventional FPGAs launched last year. Whereas, MAX series mostly comprises PLDs and CPLDs but, the latest product launched in the family is MAX 10 FPGAs. Below is a detailed overview of all four Intel products which cover both FPGAs and SoC FPGAs:

Intel® Stratix® 10

The challenges of today's industry include performance, capacity and throughput. Conforming to the requirements of artificial intelligence, 5G wireless networks, advanced search engines and high-performance computing, Intel announced their Stratix 10 capable of performing 10 trillion floating point operations per second (TFLOPS). The chipmaker has declared it as "the fastest chip of its kind in the world" [39]. Being a SoC FPGA, the chip is integrated with quad-core ARM Cortex A53 application processor which gives the user application class 2x high performance and 70% power efficiency. Intel has combined the product to processor architecture using hyperflex technology. The hyperflex architecture is a very different approach that delivers 2x performance over conventional FPGA products [40]. Intel Stratix 10 SoCs, manufactured on Intel's 14 nm process technology, includes a System Memory Management Unit which enables hardware virtualization across the processor and FPGA domains.

The challenges in communication systems are fundamentally about supporting many different protocols in a single device. In addition to that, the need to support different modulation schemes are addressed by providing up to 144 transceivers with data rates up to 30 Gbps deliver 4X serial transceiver bandwidth from previous-generation FPGAs for high port count device [41].

Traditionally, security was severe issue in military expand to areas such as cloud, data center, the internet of things. Stratix 10 has a new feature, a Secure Device Manager, that allows the user to

update their configuration codes to address the evolving threats. This is combined with advanced key management capabilities and a physically incredible function that gives FPGA designer the confidence that Stratix 10 can meet the security needs [41].

Typical applications of Startix 10 SoC FPGA are the usage in the data centre as accelerators, connectivity as well as storage controllers. They could implement typical functions such as Hadoop compassion, decompression, encryption, decryption that are implemented by other processing entities but at the tenth of a power.

Intel® Arria® 10

There is a rapidly growing demand for more information through a broad range of devices ranging from mobile phones to military handhelds. Such devices produce a huge amount of data which includes voice, images and videos as well, this caused an explosion of data in the wireline and wireless telecommunication and industrial sector. Keeping this in mind Altera has re-invented their mid-range SoC FPGA family Arria 10 enables higher performance than previous high-end FPGAs while simultaneously delivering lower power than today's mid-range FPGAs. The Intel Arria 10 SoC, based on 20 nm process technology offered by fabrication partner Taiwan Semiconductor Manufacturing Company (TSMC), combines a dual-core ARM Cortex A9 Hard Processor System that includes hardened floating-point digital signal processing blocks. The new generation equipped with 40% lower power and 60% better performance than previous mid-range FPGAs provided that 15% higher performance than previous high-end SoC. The four times better 96 high-speed serial transceivers are capable of supporting up to 28 gigabits per second that over 3.6 terabits seconds per worth of bandwidth. The high-speed transceiver also allows Arria 10 FPGAs SOCs to connect up to 16 serial memory interfaces or four links at data rates up to 15 gigabits per second offering a bandwidth of one terabit per seconds in hybrid memory cubes. The I/O structures are also designed to allow direct connection of high-performance external memory interfaces like DDR4 SD RAM, it also supports up to 4 x 72 DDR4 interfaces add data rates of 2.66 gigabits per second [42].

The Arria 10 vendors see its market mostly in telecommunication sector where the wireless infrastructure requires a bandwidth of 100Gbps to 200Gbps constraint by power and performance issues. There is also definitely nascent growing market of cloud computing where flash-assisted storage are implemented under incredible pressure, one of the most cost constraint markets is identified in broadcasting 4k Ultra-high definition videos.

Intel® Cyclone® 10

Things are continuously become more connected and sharing a huge amount of real-time data coming from sensors and cameras in factories, buildings, home and vehicles. In February 2017, to serve the growing demand for such smart and connected devices Intel introduced Cyclone 10 families optimized for high-bandwidth and low-cost applications. They have a variety of other uses, including for automotive, industrial automation, audio-visual systems. The Cyclone® 10 FPGAs – Cyclone® 10 GX and Cyclone® 10 LP both have a different variety of features to offer. The best part about these two sub-families of Cyclone 10 FPGA, they support software migration, means a user may start developing their product using any of them and can upgrade or downgrade later to boost design efficiency by tuning power and cost [43].

The set of features that make Cyclone 10 GX unique from other low-cost FPGAs are; hardened floating point DSP unit and transceivers up to 10G bandwidth which offers 2X higher performance than the previous generation. The architectural enhancements enable implementation of IEEE 754 compliant hardened floating-point unit which can operate in three modes; standard-precision fixed-point, high-precision fixed-point, and single precision fixed-point making computation possible up to 134 GFLOPs (Giga floating-point operations per second) [44]. This is important for engineers needing higher performance using the FPGA for applications such as motor control systems. Secondly, the Cyclone 10 GX offers maximum frequency of 12.5 Gbps per transceiver I/O for chip-to-chip communications provided by number of high-speed communicating protocols which includes GigE Vision, USB 3.1, CoaXPress, Camera Link, DisplayPort 1.3, HDMI and even, PCI Express which may give the power to connect to an external Intel processor [45]. The market for Intel Cyclone 10 GX includes those where high I/O performance and core speed are key requirements. Typical applications are industrial machine vision system, a smart city with surveillance in parking lots, road and/or bridges equipped with high-definition video streaming.

The LP family extends the Cyclone 10 FPGA to a broad spectrum for general logic applications where low-cost and high-volume are key requirements. These FPGAs have been built on 60-nm process technology and reduced the power consumption by 50% in comparison to the previous generation of Intel's Cyclone V FPGA. The LP series has significantly simplified the power distribution network of the system, needing just two core power supplies for operation, saving your board's cost, board space and design time [46]. With a range of IP blocks providing up to 500 I/Os including I2C, SPI, UART and parallel IO blocks, LP FPGAs are best suited for application where FPGAs accompany microprocessors for IO expansion. Cyclone 10 LP can be also used for automotive video processing and in sensor fusion.

Intel® MAX® 10

The MAX 10 FPGA family is a full-featured general purpose programmable logic family that combines a large number of FPGAs features along with all the ease to use features normally associated in non-volatile programmable logic devices. The device family offers densities up to 50,000 logic elements, integrated ADC and temperature sensor, internal SRAM, PLL's, dual image configuration capability, numerous IOs standards, design security and sleep mode features. The devices are non-volatile, enabling instant-on benefit and feature integrated voltage regulators and internal oscillators [47].

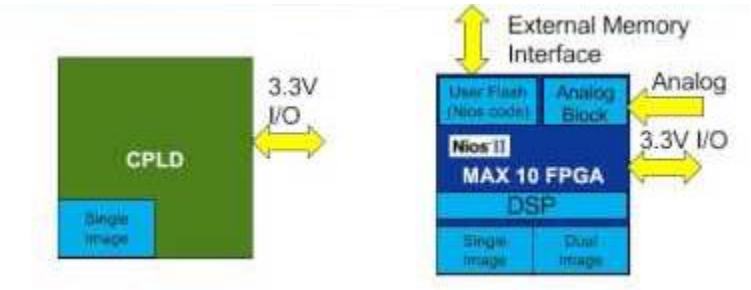

Figure 4: Block diagram comparison of conventional CPLDs and MAX10 FPGA

Coming back to the MAX series of Altera, before the launch of MAX10 all the devices in the series were CPLDs but, the launch of MAX10 later in 2014 has revolutionized non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor programmable logic device. Figure 4 depicts a comparison between a conventional CPLD with limited capabilities and the MAX10 FPGA. Unlike CPLDs, MAX 10 FPGAs includes full-featured FPGA capabilities, such as Nios® II soft core embedded processor support, digital signal processing (DSP) blocks, and soft DDR3 memory controllers. Nios II is fully equipped 32-bit soft-core processor which gives the user the flexibility of despite selecting the best suitable processor for the application select MAX10 to create your own, just up to your specifications. A MAX10 based circuit can potentially be used in a data centre as Power Management Integrated Circuit, and other applications due to their right combination of instant on, analog inputs, and digital control. Additionally, it can be used in numerous automotive, industrial and other board management application.

Conclusion

The prospect of FPGA-powered supercomputing has never looked brighter than this, neither there couldn't any better time for FPGA enthusiasts. The largest FPGA deployments in data centres after recent acquisitions indicate that the biggest FPGA players Xilinx and Altera (now Intel) are pushing their ware fares towards server computers. Furthermore, the constraint that held back massive adoption of these programmable devices, were ease of programmability that relied on low-level languages. The involvement of Intel and Microsoft with latest products deployed in high-performance computing and hardware accelerators will undoubtedly devote considerable resources to a more complete developer toolset and system software stack for these devices which will open doors for high-level application programmers as well. This study concludes that all the products mentioned are serving their purpose at best and it always depends upon the application the design engineer is looking to implement on the device which will make an FPGA more suitable. Once the reader selects the manufacturer and product family of interest the next step is to refer to the official documentation available online to dig more into the technical specifications. Lastly, it is always a good idea to look for related application notes by the manufacturer before selecting the programming device.

References

[1] "XC2064/XC2018 logic cell array product specification," Xilinx Inc..

[2] "Intel® Stratix® 10 GX/SX Product Table," Intel Corporation, [Online]. Available: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pt/stratix-10-product-table.pdf.

[3] "Xilinx, Arm, Cadence, and TSMC Announce World's First CCIX Silicon Demonstration Vehicle in 7nm Process Technology," Xilinx Inc., 11 09 2017. [Online]. Available: https://www.xilinx.com/news/press/2017/xilinx-arm-cadence-and-tsmc-announce-world-s-first-ccix-silicon-demonstration-vehicle-in-7nm-process-technology.html. [Accessed 11 09 2018].

[4] P. . Dillien, "And the Winner of Best FPGA of 2016 is...," , . [Online]. Available: http://www.eetimes.com/author.asp?doc_id=1331443. [Accessed 9 9 2018].

[5] "FPGA Market Size, Share, Growth, Industry Analysis Report ...," GrandView Research, 2015.

[6] K. Morris, "Lattice Acquires SiliconBlue," Silicon Symbiosis, 13 12 2011. [Online]. Available: http://www.eejournal.com/article/20111213-lattice/. [Accessed 11 09 2018].

[7] "MICROCHIP TECHNOLOGY TO ACQUIRE MICROSEMI," Microchip Technology Inc., 12 03 2018. [Online]. Available: https://investor.microsemi.com/2018-03-01-MICROCHIP-TECHNOLOGY-TO-ACQUIRE-MICROSEMI. [Accessed 11 09 2018].

[8] L. Mann and L. B. Baker, "Intel to buy Altera for $16.7 billion in its biggest deal ever," BUSINESS NEWS, 01 06 2015. [Online]. Available: https://www.reuters.com/article/us-altera-m-a-intel/intel-to-buy-altera-for-16-7-billion-in-its-biggest-deal-ever-idUSKBN0OH2E020150601. [Accessed 11 09 2018].

[9] L. Hopperton, "Xilinx introduces 'industry's first' extensible processing platform," embedded world, 01 03 2011. [Online]. Available: http://www.newelectronics.co.uk/electronics-news/embedded-world-xilinx-introduces-industrys-first-extensible-processing-platform/31861/. [Accessed 12 09 2018].

[10] Microsoft, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter ServicesMicrosoft," [Online]. Available: https://www.cc.gatech.edu/~hadi/doc/paper/2014-isca-catapult.pdf.

[11] L. Latif, "FPGA manufacturer claims to beat Moore's Law," Incisive Business Media Limited, 27 10 2010. [Online]. Available: https://www.theinquirer.net/inquirer/news/1811460/fpga-manufacturer-claims-beat-moores-law. [Accessed 12 09 2018].

[12] C. Maxfield, "Xilinx ships the world’s first heterogeneous 3D FPGA," EE Times, 5 30 2012. [Online]. Available: https://www.eetimes.com/document.asp?doc_id=1317249. [Accessed 12 09 2018].

[13] "FPGA Start-Up Tabula Exits Stealth Mode, Unveils “3-D” Architecture and First Devices," Berkeley Design Technology, Inc., 18 03 2010. [Online]. Available: https://www.bdti.com/InsideDSP/2010/03/18/Tabula. [Accessed 11 09 2018].

[14] "Field Programmable Gate Array Market|Opportunity Analysis|Industry Size|Segment Forecast 2015-2024," Variant Market Research, 2015.

[15] "FPGA Market Size, Share, Analysis, Research Report, 2020 - Radiant Insights," Radiantinsights.com.

[16] "Transceiver - Protocols," [Online]. Available: https://www.intel.com/content/www/us/en/programmable/solutions/technology/transceiver/protocols.html. [Accessed 9 9 2018].

[17] J. Happich, "Heterogeneous 3D FPGA with 28 Gbps transceivers claims world first," 5 6 2012. [Online]. Available: http://www.mwee.com/news/heterogeneous-3d-fpga-28-gbps-transceivers-claims-world-first. [Accessed 9 9 2018].

[18] J. Keller, "Today's FPGA trends in aerospace and defense applications involve security, tools, and specialization," 14 1 2011. [Online]. Available: https://www.militaryaerospace.com/articles/2011/01/today-s-fpga-trends.html. [Accessed 9 9 2018].

[19] "25+ Continuous Years Supporting Aerospace and Defense," Xilinx Inc., [Online]. Available: https://www.xilinx.com/applications/aerospace-and-defense.html. [Accessed 9 9 2018].

[20] "Radiation-Hardened, Space-Grade Virtex-5QV FPGA Data Sheet," [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds692_V5QV_Data_Sheet.pdf.

[21] "Intel Introduces Versatile New FPGA for Industrial and Automotive Markets," 13 02 2017. [Online]. Available: https://newsroom.intel.com/news/intel-introduces-versatile-new-fpga/. [Accessed 10 09 2018].

[22] "FPGAs, Virtex UltraScale+," Xilinx Inc., [Online]. Available: https://www.xilinx.com/support/documentation/product-briefs/virtex-ultrascale-plus-product-brief.pdf.

[23] "Heterogeneous MPSoC," Xilinx Inc., [Online]. Available: https://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html#productTable.

[24] "FPGA Market worth 9.50 Billion USD by 2023," MarketsandMarkets™, Seattle, WA, 2017.

[25] I. Kuon and J. Rose, "Measuring the Gap Between FPGAs and ASICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 26, no. 2, pp. 203-215, 2007.

[26] "ASIC Design Starts 2017: Consumer and Industrial Lead the Way," Semico Research Corp, September 2017.

[27] "Xilinx Ships 16nm Virtex UltraScale+ Devices; Industry's First High-End FinFET FPGAs," Xilinx Inc., 28 01 2016. [Online]. Available: https://www.xilinx.com/news/press/2016/xilinx-ships-16nm-virtex-ultrascale-devices-industry-s-first-high-end-finfet-fpgas.html. [Accessed 14 09 2018].

[28] "Virtex UltraScale+," Xilinx Inc., [Online]. Available: https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html. [Accessed 14 09 2018].

[29] X. Inc., "Virtex UltraScale+ Product Brief," [Online]. Available: https://www.xilinx.com/support/documentation/product-briefs/virtex-ultrascale-plus-product-brief.pdf. [Accessed 14 09 2018].

[30] K. Freund, "Amazon's Xilinx FPGA Cloud," Forbes, 13 12 2016. [Online]. Available: https://www.forbes.com/sites/moorinsights/2016/12/13/amazons-xilinx-fpga-cloud-why-this-may-be-a-significant-milestone/#3b0ba4dc370d. [Accessed 14 09 2018].

[31] N. Mehta, "Pushing Performance and Integration, Xilinx Inc.," 24 11 2015. [Online]. Available: https://www.xilinx.com/support/documentation/white_papers/wp471-ultrascale-plus-perf.pdf. [Accessed 15 09 2018].

[32] "Key UltraScale+™ Portfolio Benefits: 1 GHz eBand Modem," Xilinx Inc., [Online]. Available: https://www.xilinx.com/applications/wireless-communications/wireless-backhaul/eband-modem.html. [Accessed 15 09 2018].

[33] T. Ray, "Xilinx: 3-D Chip a Route to More Complex Semiconductors," BARRON'S TECH TRADER DAILY, 30 05 2012. [Online]. Available: https://www.barrons.com/articles/BL-TB-36664. [Accessed 15 09 2018].

[34] "SoCs, MPSoCs & RFSoCs - Expanding the SoC Portfolio," Xilinx Inc., [Online]. Available: https://www.xilinx.com/products/silicon-devices/soc.html. [Accessed 15 09 2018].

[35] "Zynq UltraScale+ MPSoC Product Brief," [Online]. Available: https://www.xilinx.com/support/documentation/product-briefs/zynq-ultrascale-plus-product-brief.pdf. [Accessed 15 09 2018].

[36] "Xilinx Spartan-7 FPGAs Now in Production," Xilinx Inc., 09 05 2017. [Online]. Available: https://www.xilinx.com/news/press/2017/xilinx-spartan-7-fpgas-now-in-production.html. [Accessed 15 09 2018].

[37] Xilinx, "Cost-Optimized Portfolio," [Online]. Available: https://www.xilinx.com/support/documentation/product-briefs/cost-optimized-product-brief.pdf. [Accessed 15 09 2018].

[38] C. Maxfield, "Altera's shipping its first SoC FPGAs," EE Times, 12 12 2012. [Online]. Available: https://www.eetimes.com/document.asp?doc_id=1317554. [Accessed 13 09 2018].

[39] "Intel Chip Performs 10 Trillion Calculations per Second," Intel News Byte, 18 04 2018. [Online]. Available: https://newsroom.intel.com/news/intel-chip-performs-10-trillion-calculations-per-second/. [Accessed 13 09 2018].

[40] M. Hutton, "Understanding How the New Intel®HyperFlex™ FPGA Architecture Enables Next Generation High-Performance Systems," Intel WHITE PAPER FPGA, [Online]. Available: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/wp/wp-01231-understanding-how-hyperflex-architecture-enables-high-performance-systems.pdf. [Accessed 13 09 2018].

[41] "INTEL® STRATIX® 10 SOC FPGAS," Intel, [Online]. Available: https://www.intel.ca/content/www/ca/en/products/programmable/soc/stratix-10.html. [Accessed 13 09 2018].

[42] "INTEL® ARRIA® 10 SoC FPGAS Overview," Intel®, [Online]. Available: https://www.intel.com/content/www/us/en/products/programmable/soc/arria-10.html. [Accessed 13 09 2013].

[43] "INTEL® CYCLONE® 10 FPGAS," Intel®, [Online]. Available: https://www.intel.com/content/www/us/en/products/programmable/fpga/cyclone-10.html. [Accessed 09 13 2018].

[44] "INTEL® CYCLONE® 10 GX FPGA," Intel Inc., [Online]. Available: https://www.intel.com/content/www/us/en/products/programmable/fpga/cyclone-10/gx.html. [Accessed 09 13 2018].

[45] "INTEL® CYCLONE® 10 GX FPGA Features," Intel®, [Online]. Available: https://www.intel.com/content/www/us/en/products/programmable/fpga/cyclone-10/gx/features.html. [Accessed 14 09 2018].

[46] "INTEL® CYCLONE® 10 LP FPGA," Intel Inc., [Online]. Available: https://www.intel.com/content/www/us/en/products/programmable/fpga/cyclone-10/lp.html. [Accessed 13 09 2018].

[47] "INTEL® MAX® 10 FPGA," Intel ®, [Online]. Available: https://www.intel.com/content/www/us/en/products/programmable/fpga/max-10.html. [Accessed 14 09 2018].