Question

The circuit shown in Fig. 1 given below is a signature analyzer used for built in self test in digital systems. The timing characteristic of the gates and the flip-flops are listed below. The circuit operates at a supply voltage of 5V±10% in an ambient temperature range of 0 to 25 °C with a power dissipation 0f 1.5 W. The thermal resistance of the package is 40 °C/W and the process variation factor is ±30%. Determine:

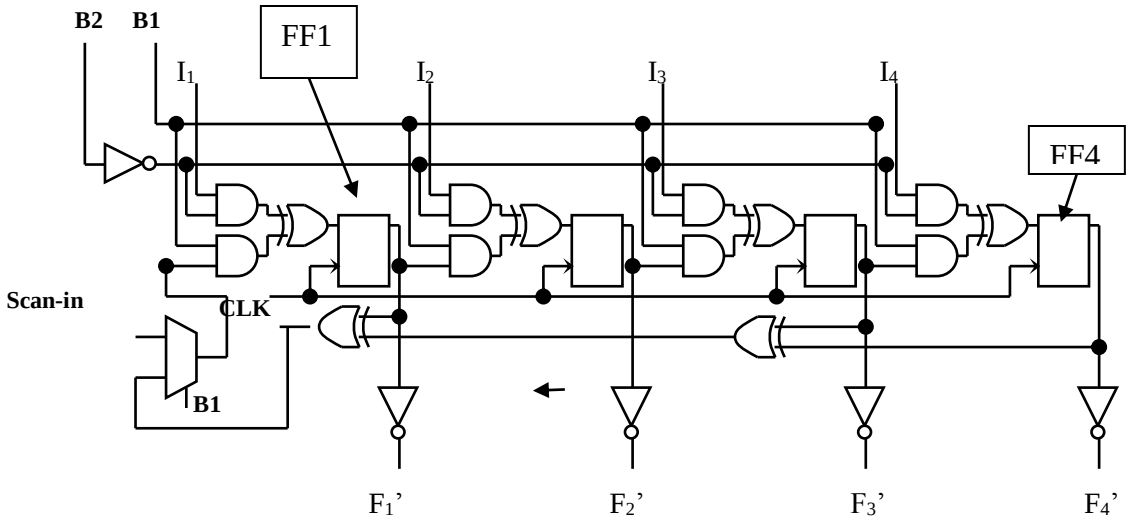
a) The critical path in the circuit. What will be the typical delay of the path?

b) Maximum speed of operation for the worst conditions.

Notes:

1. Arrival times of input signals B1, B2, Scan-in, is -∞
2. Signal I_1 to I_4 are registered inputs.
3. Temperature degrading factor M=1.5
4. K1, K2 are input and output degrading factors.

Component	Tp (ns)	Input Loading (UL)	K1 (ns/UL)	K2 (ns/fo)
Inverter	0.15	1	0.08	0.1
AND	0.15	2	0.08	0.1
XOR	0.3	2	0.12	0.15
2:1 MUX	0.4	1.5	0.12	0.15
D-FF (tsu=0.5, th=0.2ns)	0.7	2	0.10	0.2



Solution

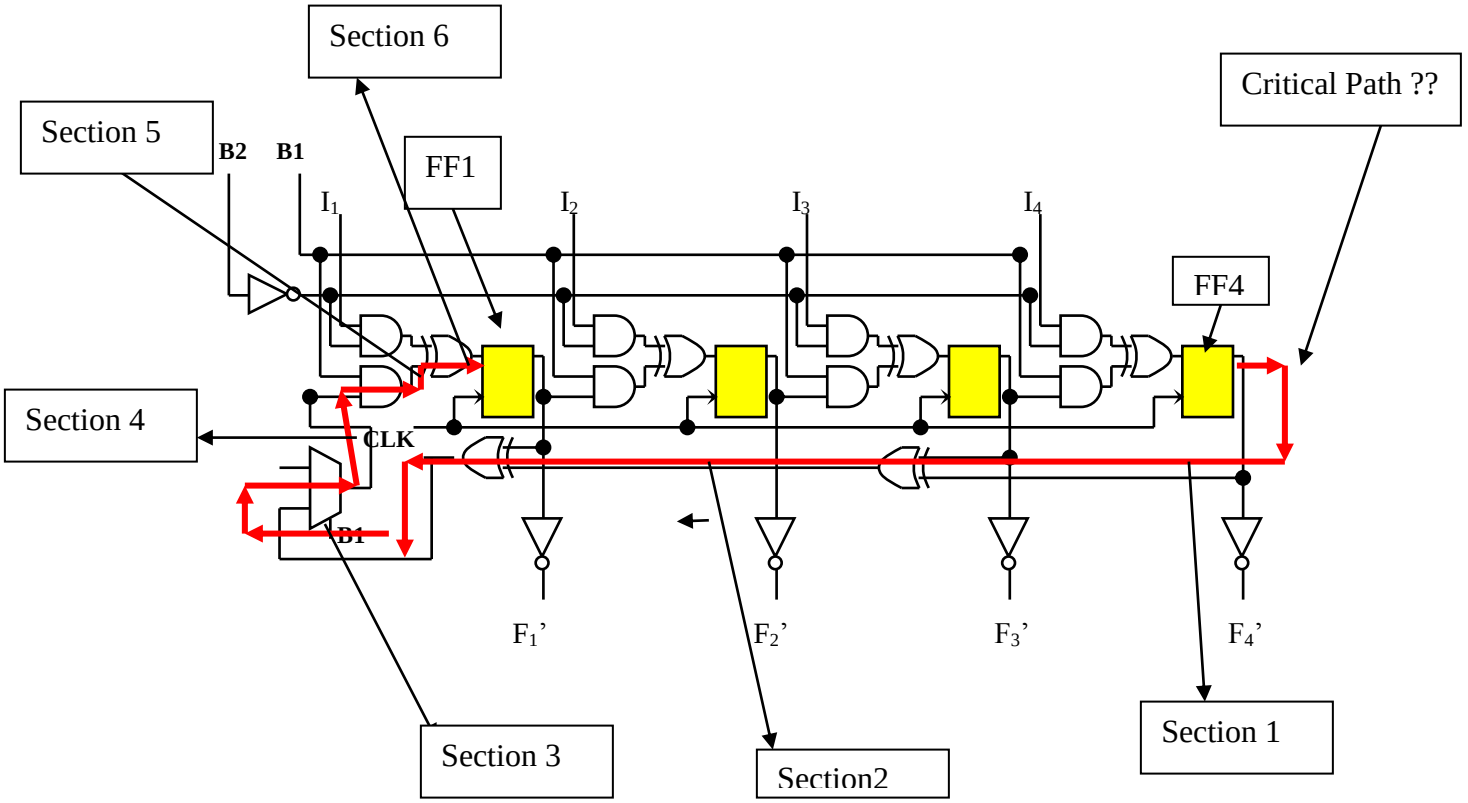
Usually all paths have to be investigated. In this case all paths in this circuit are almost of equal value except the feedback path(s). We will analyze only 2 paths for simplicity.

Part 1, Path 1

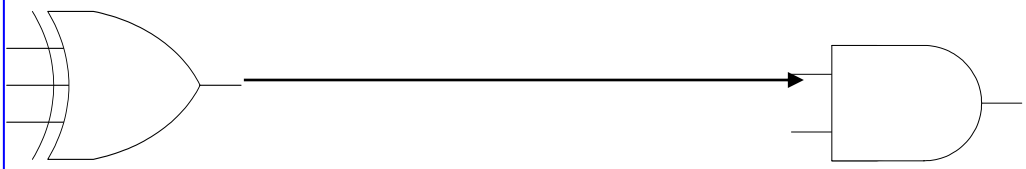
The selected path is the one outlined in heavy line, ie. the path from FF4 to FF1.

Let us assume initially that the Critical Path of the circuit is from Flip-Flop 4 to Flip-Flop 1

We will use the following model to calculate delay of each individual component



Model



Gate 1 **Gate 2**

Gate 1 is the driver,
Gate 2 is loading Gate 1.

Delay of Gate 1= Tp of Gate 1 + [K2 gate 1 * fo of G1] + [UL of Gate 2 * K1 of Gate 1]

Intrinsic	Fan out due to wiring LOAD	Fan out to input driven gate LOAD

t_{CL} = Delay of combinational block, is made up of 6 sections
= $3XOR_{delay}$ + MUX_{delay} + AND_{delay} + FF $_{load}$

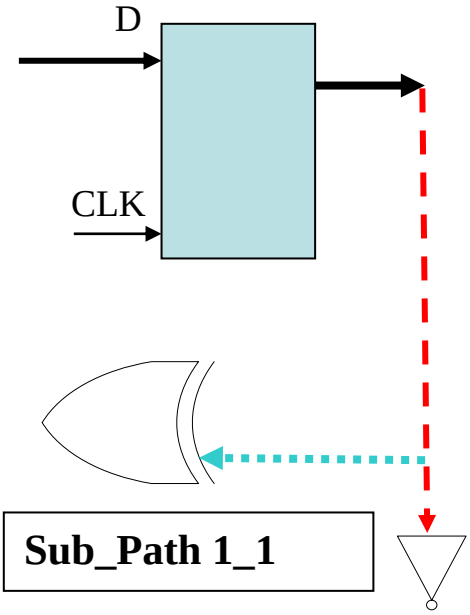
Critical Path delay = t_{CQ} + t_{CL} + t_{su}

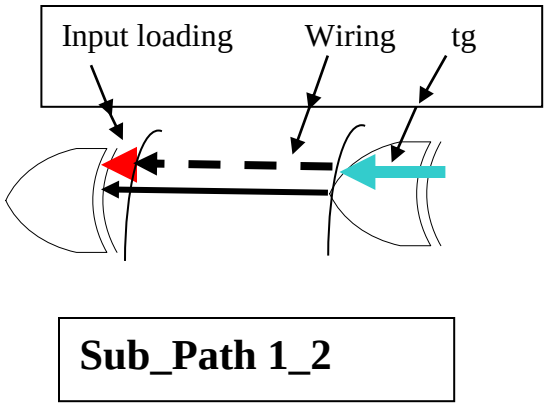
Delay of D4 (Clock to O/P)

Combinational logic delay

Setup time of D1

For example sub_path1_1 and sub_path1_2 calculation is shown below





Delay of FF K1 of FF UL (Inv + XOR) K2 of FF fo (Inv. +XOR)

Delay due FF= 0.7 + 0.1 * (1+2) + 0.2 * 2

Delay of FF will be added later (=0.7ns)
Calculating the combinational Logic Delay:

Section 1	=	----	+0.2 * 2	+ (2+1) * 0.1 =0.7
Section 2	=	0.30	+0.15 * 1	+ 0.12 * 2 =0.69
Section 3	=	0.30	+ 0.15 * 1	+ 0.12 * 1.5 =0.63
Section 4	=	0.40	+ 0.15 * 1	+ 0.12 * 2 =0.79
Section 5	=	0.15	+ 0.10 * 1	+ 0.08 * 2 =0.41
Section 6	=	0.30	+ 0.15 * 1	+ 0.12 * 2 =0.69

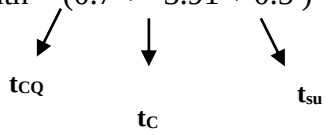
t_{int}

Fan out due wiring

Fan out due to input Capacitance loading

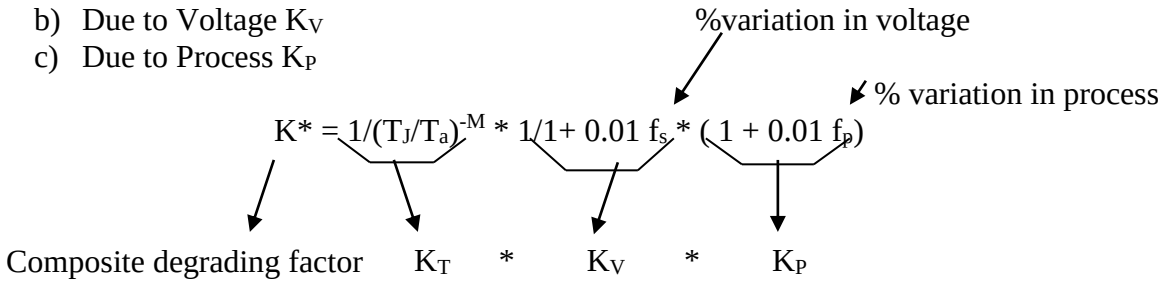
t_{CL} = Total of 6 sections =3.91ns

All units in are in ns
Delay of Critical Path = (0.7 + 3.91 + 0.5)



Typical Delay = 5.11 ns
Typical Frequency of operation < 200 MHz = 195MHz

b) De-rating factors
a) Due to Temperature K_T
b) Due to Voltage K_V
c) Due to Process K_P



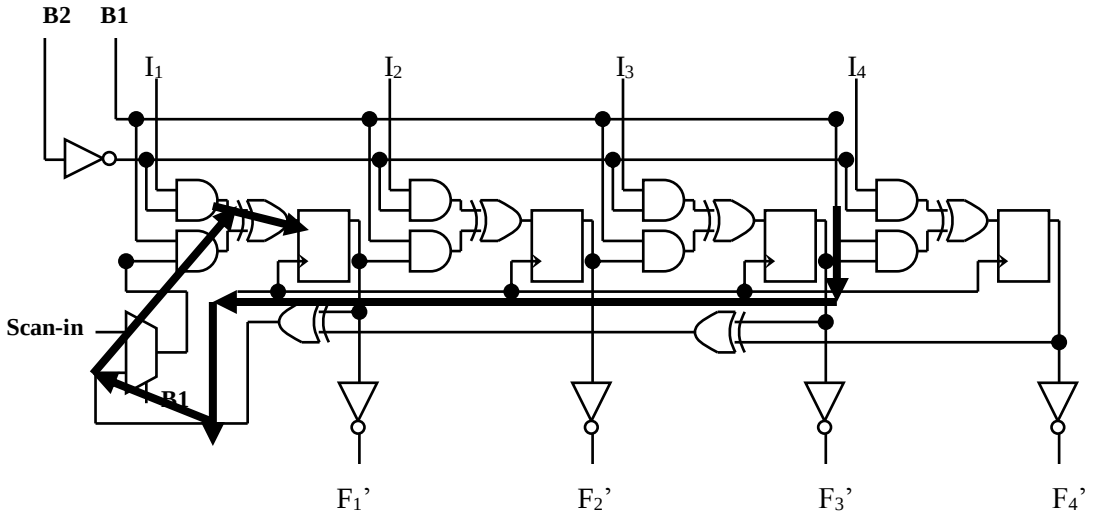
T_J = [(1.5*40) + 25] + 273
T_a = 273 + 25, M = -1.5
$K_T \cong 1.33$ = $(Tj/Ta)^{-1.5}$
$K_V \cong 1/(1-0.01f_s) = 1.11$
$K_P \cong 1 + 0.01\ f_p = 1.3$
$K^* = 1.33 * 1.11 * 1.3 \cong 1.919$

Maximum speed of operation is 195MHz/1.919 =101.6 ≅ 100 MHz

Part 2, path 2

(This Section shows how a misdiagnosis of the critical path can affect operation of the circuit)

Now we check one more time more closely, and we see that there is another path that could have delay greater than the selected path.

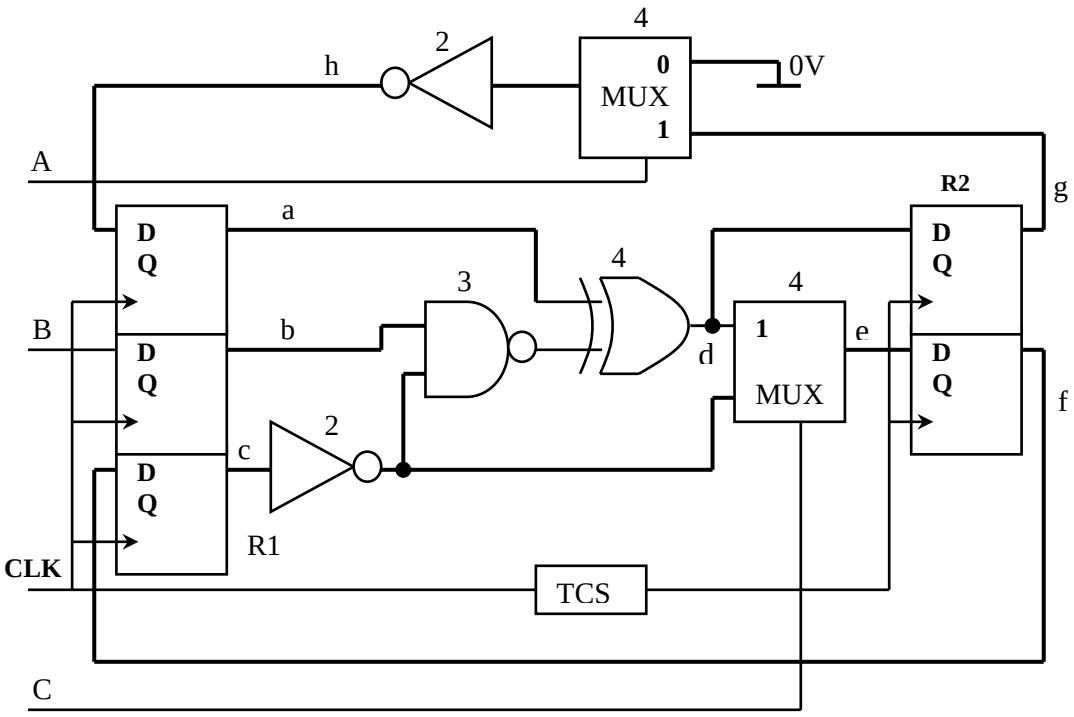


This path has one extra fanout and AND gate loading on Reg. 3 than Reg. 4. Therefore the combinational logic part will be increased by 0.1 * 2 + 0.2 * 1 = 0.4 or total delay is 5.51ns giving a frequency of
Frequency = 181.4 MHz
When the derating factors are taken into account then the frequency of the operation is reduced further to: 181.4/1.99 =91.2 MHz.
This example shows that even a little change in the loading of a path can affect the clock frequency a lot and renders our circuit incorrect..

Question

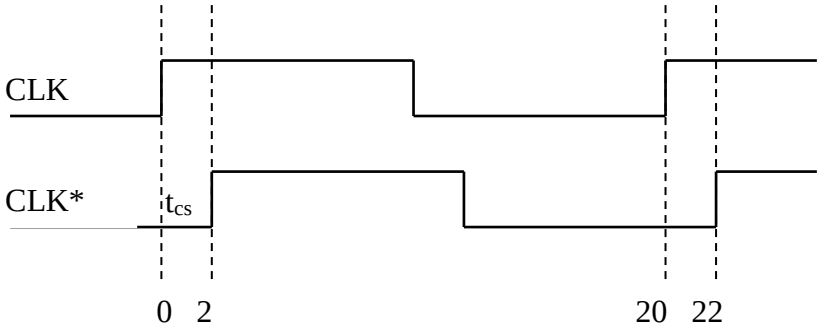
The circuit shown in the figure below has been initialized at t = -∞. The arrival time of inputs A, B, and C is -∞ sec. The first active edge of the clock of R1 register arrive at t = 0 sec. The signal skew (t_{cs}) in the clock path is 2 ns. Each F/F has:
Register switching time, t_{cq} = 6 ns, set up time, t_{su} = 4 ns, hold time, t_h = 2 ns.

a) Determine the arrival times, required times and the slack times for all nodes identified in the figure. Assume a clock rate of 50 MHz.
   Do you anticipate any timing problem?
b) Determine the maximum speed of operation.
c) What happens if the clock skew t_{cs} = -7 ns.



Solution

a)



a)

For the arrival time start at the output of R1 reg. and follow the signal as it goes through the logic. For the required time start backward with the clock period, clock skew and the setup time to see when it is required to be stable at the input of the registers. For the feedback loops consider where the signal is feeding and when it has to be there. The table below is the results.

Nodes	Arrival		Required		Slack
a	t_{cq}	6	e-$t_{mux\text{-}txor}$	10	4
b	t_{cq}	6	e-t_{mux}-$t_{AND\text{-}txor}$	7	1

Violations

c	t_{cq}	6	$e-t_{mux}-t_{AND}-t_{inv}$	5	* -1
d	$t_{cq} + t_{xor}$ $t_{cq} + t_{xor} \_ t_{AND}$ $t_{cq} + t_{xor} \_ t_{AND} + t_{inv}$	10 13 15✓	e- t_{mux} $T+t_{cs}-t_{su}$	14 ✓	***-1**
e	d + 4	19	$T+t_{cs}-t_{su}$	18	***-1**
f	$t_{cq} + t_{cs}$	8	$T-t_{su}$	16	8
g	$t_{cq} + t_{cs}$	8	$h-t_{inv}-t_{mux}$	10	2
h	$t_{mux} + t_{inv}$ $g + t_{mux} + t_{inv}$	6 14✓	$T-t_{su}$	16	2

There is a problem in **nodes "c" and "e " and "d" each have –1 slack time**. To overcome this problem, the circuit has to be redesigned or the clock frequency reduced.

b) The maximum speed then is $T \geq 20$ + (slack violation)
or $T \geq t_{cq} + t_{CL+} t_{su} - t_{cs} = 21$ $T \geq 21$
f = 1/21 ns ≅ 47.6 MHz or 45 Mhz. could be used

c) If the circuit has –ve clock skew, since the circuit has feedback then the negative clock skew will be helpful to the FB path but will be worse for the path where data and clock have the same direction. For proper operation then T has to be adjusted to
T =has to increase
$t_{cq} + t_{logic} + t_{su} + t_{cs} = 30$ ns

6 + 13 + 4 + 7 **Problem**

Nodes	Arrival		Required		Slack
a	t_{cq}	6	$e-t_{mux-txor}$	10	4
b	t_{cq}	6	$e-t_{mux}-t_{AND-txor}$	7	1
c	t_{cq}	6	$e-t_{mux}-t_{AND}-t_{inv}$	5	-1
d	$t_{cq} + t_{xor}$ $t_{cq} + t_{xor} \_ t_{AND}$ $t_{cq} + t_{xor} \_ t_{AND} + t_{inv}$	10 13 15✓	e- t_{mux} $T+t_{cs}-t_{su}$	14 ✓ 18	***-1**
e	d + 4	19	$T+t_{cs}-t_{su}$	18	***-1**

Violations

f	$t_{cq} + t_{cs}$	8	$T-t_{su}$	16	8
g	$t_{cq} + t_{cs}$	8	$h-t_{inv}-t_{mux}$	10	2
h	$t_{mux} + t_{inv}$ $g + t_{mux} + t_{inv}$	6 14√	$T-t_{su}$	16	2