ECE 4170

Quiz II
March 28th, 2007

1. The Georgia Tech Honor Code governs this examination. Please note you are not to discuss this examination with anyone. Your signature below attests to the same.
2. There are 3 questions. Make sure you have all of them.
3. Please write/draw **legibly**.
4. State any assumptions you feel you have to make or ask for clarification
5. Keep in mind it is difficult to give partial credit without written material. Please make sure you document any partial solutions.
6. **The points are shown next to each problem. Plan your work!**
7. I will be available in person Wednesday until 4:30 pm and electronically thereafter. Thursday AM I will be available electronically until 10:00 and then in person from 10:30 AM . Contact me if you have any questions or just come by**.**
8. Turn in your exam as follows.
    a. The answers to questions 2 & 3 should be in a single directory.
    b. One text (e.g., Word) file with answers to each question
    c. One zip file of all of the directory and answer document
    d. Email time stamped by 12 noon Thursday, March 29th.
    e. No late submissions will be accepted.

Problem	Max Points	Graded
1	10	
2	30	
3	10	
Total	50	

Student Name: _____

Student Number: _____

I have neither received nor given assistance on this examination.

_____

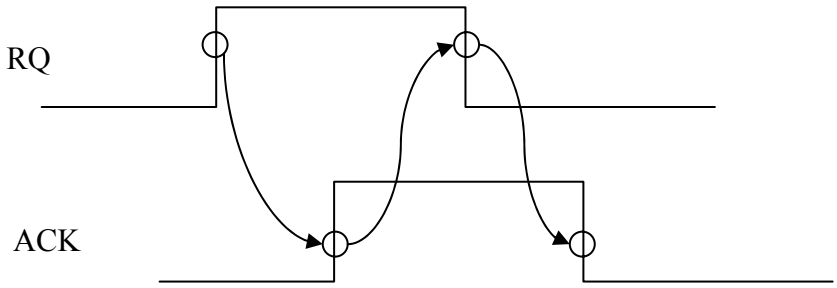
Signature

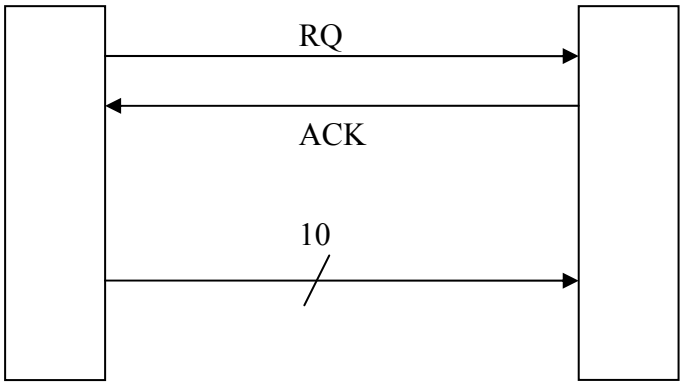
Question 1

1. In the synthesis of a process, identify three consequences of using signals vs. variables.
2. Can I synthesize a function that accepts an unconstrained array type as an argument? Explain your answer.

Question 2

Implement a synthesizable VHDL model of a unidirectional communication channel where a single data transfer is implemented using the four phase request-acknowledge handshake as shown in the figure below. The assertion of RQ causes the receiver to read the value on the channel and assert ACK. The transmitter then drops RQ which causes the receiver to drop ACK. The channel is 8 bits wide and one handshake sequence will transfer one byte. Implement, synthesize & demonstrate a channel model that will transmit 4 bytes, i.e., we need 4 handshakes. You may choose the store/receive these four bytes in any way you wish, but the four bytes must be received and stored. You may add additional control signals if you wish.





a. Construct three VHDL modules: transmitter, receiver and a top level that couples the transmitter and receiver.

Use the Xilinx ISE tool chain to synthesize your design to a XCV50, BG256 -4 part FPGA. Optimize the design for speed and report your maximum frequency value. What is the bandwidth you can achieve across this channel in Mbytes/sec? Offer some suggestions for speeding up this transfer (based on your design). Include a printout of a suitably annotated trace to demonstrate the functionality of the channel logic.

Question 3

Implement and synthesize model of an encoder that computes the checksum for a 4 byte message and appends the checksum to the message. The checksum is computed as the modulo 256 sum of the four bytes of the message. Thus you will compute the sum of the four bytes, take the remainder modulo 256 and attach this byte to the message now making it a 5 byte message. Checksums are used to detect classes of errors introduced by noisy channels by re-computing the checksum at the receiver and comparing it to the checksum received across the channel.

You **do not have to integrate** this checksum circuit with the transmitter and receiver but you **do have to synthesize** and produce the 5 byte packet that the transmitter/receiver pairs use.